Optimized Interleaver for NG-EPON Upstream

IEEE 802.3ca Meeting, Spokane, WA

12-14 Sept 2018

Zheng Liu, Jun Shan Wey (ZTE)

Chuanchuan Yang, Lei Zhang, Chun Yang (Beijing University)

Outline

This contribution presents an optimized interleaver for NG-EPON upstream transmission

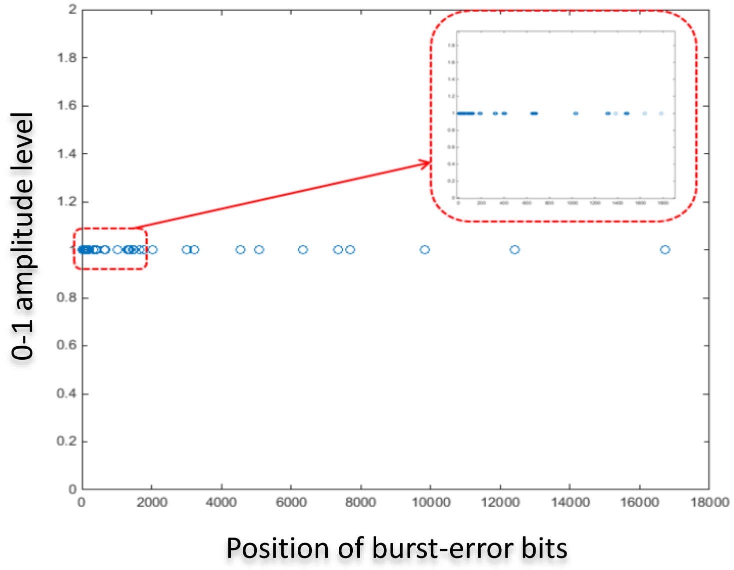
- Introduction
- Simulation Channel Model
- Optimized Interleaver Design Concept & Performance
- Summary

Introduction

- In the July 2018 meeting, the 802.3ca Task Force adopted the Omega network 256*256 interleaver for upstream (draft_3ca_D1_2_clean). However, in real cases, the length of burst-error in the upstream channel is always larger than 256 bits, which makes the Omega network interleaver not effective
- To approximate the real case burst-error condition, the upstream Gilbert channel parameters should be adjusted
- In this contribution, we present an optimized interleaver to better handle burst-error longer than 256 bits

Burst-error location affects the FEC performance

- Channel characteristics of 10G PON upstream burst error were described in [1][2]
- Highest error counts usually occur at the start-of-burst, within the first ~150 ns window
  - Equivalent to 1500 bits for 10G PON and 2500 bits for 25G PON
- They are due to transient effects in optically amplified PONs and in burst-mode Tx/Rx
- Longer preamble could mitigate the issue at the expense of lower throughput
- BER is correlated to the burst errors and distributed non-uniformly

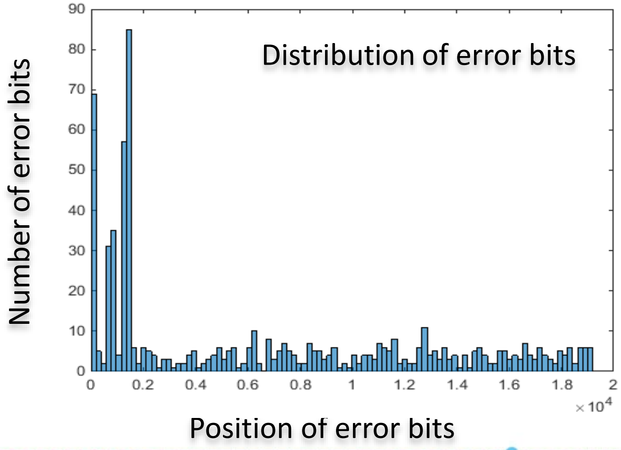


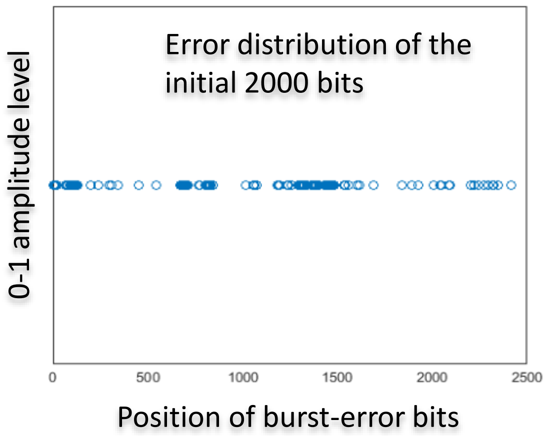
[1] D. Brunina, et al. “Analysis of forward error correction in the upstream channel of 10Gb/s optically amplified TDM-PONs,” Th4H.3, OFC 2015
[2] N. Brandonisio, et al. “Forward Error Correction Analysis for 10Gb/s Burst-Mode Transmission in TDM-DWDM PONs.” Th2A.28, OFC 2017

Description of the simulation channel model

- Built on Gilbert+AWGN channel according to real PON uplink channel characteristics
- Gilbert channel is a two-state Markov-chain, containing Good (G) state and Bad (B) state
- Prob(Good→Bad) should be smaller than Prob(Bad→Good), so that Markov-chain will converge to Good state
- Consecutive burst errors concentrate on the head of LDPC codeword, simulating the real situation
- Bit-error positions $\mathbf{L_1}$ and interleaving bit-length p_0 are obtained from channel model

- With Prob(Good→Bad) = 0.0032, Prob(Bad→Good) = 0.037, EbN0 = 3.0dB, bit-error distribution is as follows:



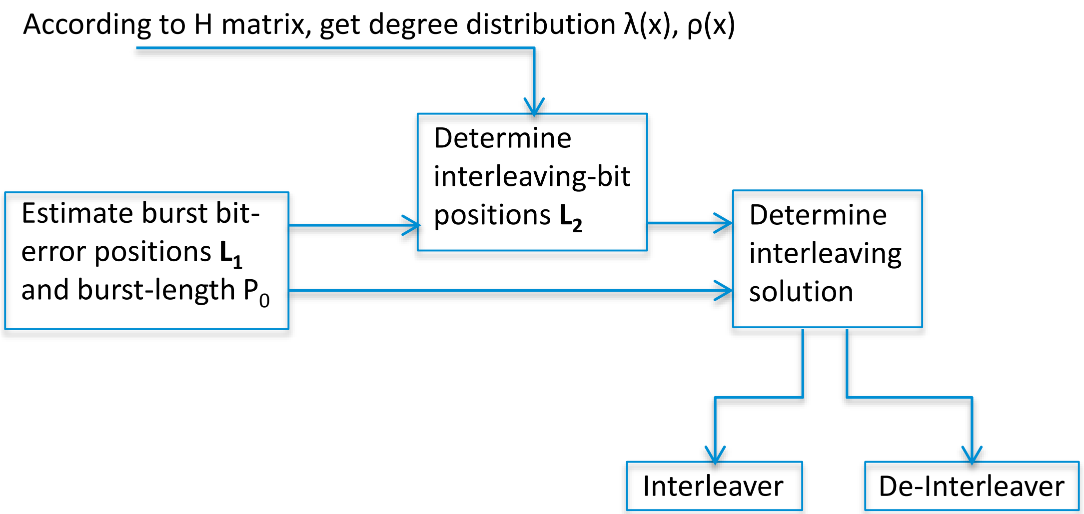


ZTE

Optimized interleaver design concept

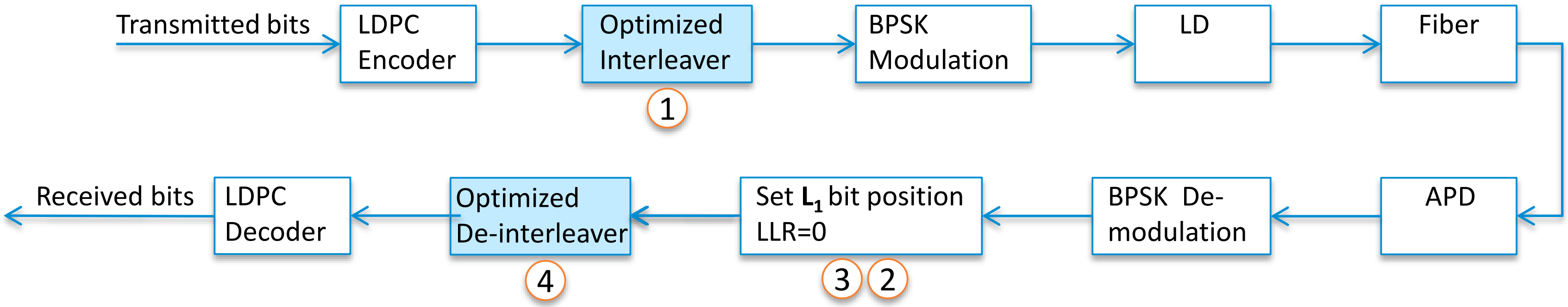
Design concept:

1. Estimate consecutive burst bit-error positions $\mathbf{L_1}=\{l_{11}, l_{12}, ..., l_{1p}\}$ and burst-length p_0. l_{1i} (i=1,2,...) denotes the position of the i-th flipped-bit error
2. According to H matrix, determine interleaving bit-positions $\mathbf{L_2}=\{l_{21}, l_{22}, ..., l_{2p}\}$. l_{2i} (i=1,2,...) denotes the position of the i-th interleaving bit
3. Determine interleaving solution. After getting $\mathbf{L_1}$ and $\mathbf{L_2}$, interleaver will map bits from $\mathbf{L_1}$ position to $\mathbf{L_2}$ position randomly, while de-interleaver will recover bits from $\mathbf{L_2}$ position to $\mathbf{L_1}$ position



ZTE

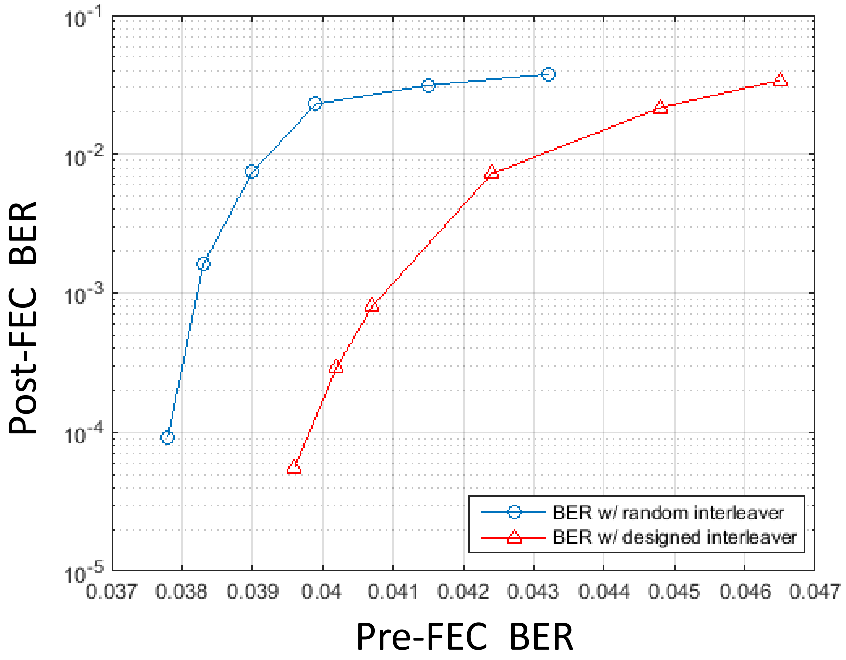
Simulation model of optimized interleaver



Flow introduction:

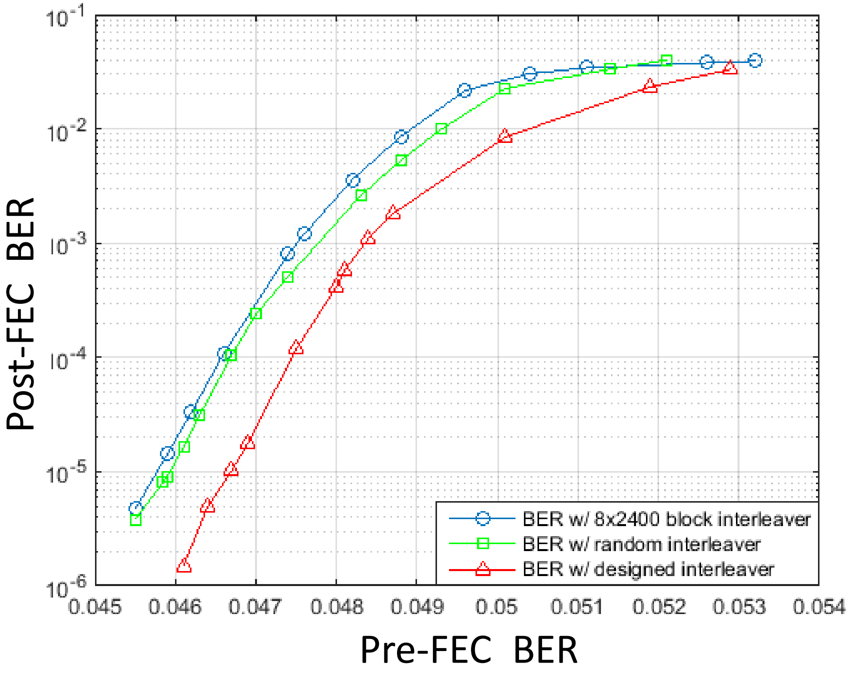
1) Transmitted bits pass through the optimal interleaver, where burst bits located at the head of LDPC codeword (L_1) are mapped to the *best interleaving bit-positions*
2) Get initial LLR (log likelihood ratio) of each received bit after soft-demodulation of BPSK
3) Set the *best interleaving bit-positions* LLR=0
4) De-interleaver is the same of the interleaver operating in reverse

Performance of optimized interleaver: example 1



- Prob(G->B)=0.0032, Prob(B->G)=0.037
- Random interleaver generates a set of random numbers as interleaving bit-positions, such as the Omega network 256*256 interleaver
- Optimized (designed) interleaver generates the best interleaving bit-positions according to a density evolution algorithm

Performance of optimized interleaver: example 2



- Prob(G->B)=0.001, Prob(B->G)=0.037
- Random interleaver generates a set of random numbers as interleaving bit-positions, such as the Omega network 256*256 interleaver
- Optimized (designed) interleaver generates the best interleaving bit-positions according to density evolution algorithm

Summary

- Location of burst-error greatly affects the FEC performance
- Highest error counts occur at the start-of-burst, within the first ~150 ns window → longer than 256 bits
- Omega network 256*256 interleaver is not sufficient to handle long error counts
- Parameters of Gilbert channel model need to be modified to meet the real situation
  - Prob(Good→ Bad): determine how sparsely the error bits are distributed
    - Smaller value ∝ more sparsely distributed
  - Prob(Bad→Good): inversely proportional to the burst error length
    - Smaller value ∝ longer burst error length
- We propose to consider the optimized interleaver for upstream transmission

Thank You!

Leading 5G Innovations