Cl 45 Introduction

Basics

- Cl 45 provides for the MDIO which allows management entities access to PHY control registers
- Control registers are split into various areas (see next slide), 3ca most concerned with:
  - PMA/PMD
  - PCA
  - PHY XS (possibly)

MMDs

- Table 45-1 MDIO Manageable Device addresses
  - Register area that require changes
    - PMA/PMD
    - PCS
  - Areas that might need changes
    - PHY XS (unlikely)

Red = touch

Black = maybe

Gray = possibly of interest to Nx25G-EPON

Register Address	MMD Name	Clause
0	Reserved	
1	PMA/PMD	45.2.1
2	WIS	45.2.2
3	PCS	45.2.3
4	PHY XS	45.2.4
5	DTE XS	45.2.5
6	TC	45.2.6
7	Auto-Negotiation	45.2.7
8	Separated PMA (1)	
9	Separated PMA (2)	
10	Separated PMA (3)	
11	Separated PMA (4)	
12	OFDM PMA/PMD	45.2.8
13	Power Unit	45.2.9
14 to 27	Reserved	
28	PLCA	45.2.13
29	Clause 22 extension	45.2.10
30	Vendor specific 1	45.2.11
31	Vendor specific 2	45.2.12

PMA/PMD changes and additions

Table 45-3

Register Address	Title	Clause	Table	Notes
1.0	PMA/PMD control 1	45.2.1.1	Table 45–4	25 & 50 Gb/s operation
1.4	PMA/PMD speed ability	45.2.1.4	Table 45–6	25 & 50 Gb/s speed select
1.7	PMA/PMD control 2	45.2.1.6	Table 45–7	Add Nx25G-EPON PMDs *
1.9	PMA/PMD transmit disable	45.2.1.8	Table 45–11	PMD Tx Disable by lane
1.10	PMD receive signal detect	45.2.1.9	Table 45–13	PMD Rx Sig Det by lane
1.11	PMA/PMD extended ability	45.2.1.10	Table 45–14	P2MP, 25G
1.12	10G-EPON PMA/PMD ability	45.2.1.11	Table 45–15	Need something similar for each PMD in Nx25G-EPON
1.14, 1.15	PMA/PMD package identifier	45.2.1.13	----	specified in 22.2.4.3.1.
1.19	25G PMA/PMD extended ability	45.2.1.17	Table 45–20	8 slots left, probably not desirable for Nx25G-EPON
1.20	50G PMA/PMD extended ability	45.2.1.17a	Table 45–20a	bits 5-14 available
1.25	PMA/PMD extended ability 2	45.2.1.21a	Table 45–24a	bits 1-15 unused
1.26	Reserved			PMA/PMD control 3?
1.110 to 1.128	Reserved			Nx25G-EPON extended ability?
1.600	PMA precoder control Tx output	45.2.1.132a	Table 45–102a	precoder control for 4 lanes
1.601	PMA precoder control Rx input	45.2.1.132b	Table 45–102b	precoder control for 4 lanes
1.2309 to 1.32767	Reserved			Sync Pattern?
New	Nx25G-EPON PMD Ext ability register			1 bit per PMD type (40 bits needed)
New	Sync Pattern			1 set for Discovery & 1 set for Normal or 3 sets each? Either way >100 registers needed

* - Limited space, may need to add a new register

PMA/PMD suggestions

- Add new register for PMA/PMD control 3
  - Register 26

Table 45–20b—PMA/PMD control 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.26.15:7	Reserved	Value always 0	RO
1.26.6:0	PMA/PMD type selection	0101000 = 50GBASE-PQX-U3 0100111 = 50GBASE-PQX-U2 0100110 = 50GBASE-PQX-D3 0100101 = 50GBASE-PQX-D2 0100100 = 50GBASE-PQG-U3 0100011 = 50GBASE-PQG-U2 0100010 = 50GBASE-PQG-D3 0100001 = 50GBASE-PQG-D2 0100000 = 50/25GBASE-PQX-U3 0011111 = 50/25GBASE-PQX-U2 0011110 = 50/25GBASE-PQX-D3 0011101 = 50/25GBASE-PQX-D2 0011100 = 50/25GBASE-PQG-U3 0011011 = 50/25GBASE-PQG-U2 0011010 = 50/25GBASE-PQG-D3 0011001 = 50/25GBASE-PQG-D2 0011000 = 50/10GBASE-PQX-U3 0010111 = 50/10GBASE-PQX-U2 0010110 = 50/10GBASE-PQX-D3 0010101 = 50/10GBASE-PQX-D2 0010100 = 50/10GBASE-PQG-U3 0010011 = 50/10GBASE-PQG-U2 0010010 = 50/10GBASE-PQG-D3 0010001 = 50/10GBASE-PQG-D2 0010000 = 25GBASE-PQX-U3 0001111 = 25GBASE-PQX-U2 0001110 = 25GBASE-PQX-D3 0001101 = 25GBASE-PQX-D2 0001100 = 25GBASE-PQG-U3 0001011 = 25GBASE-PQG-U2 0001010 = 25GBASE-PQG-D3 0001001 = 25GBASE-PQG-D2 0001000 = 25/10GBASE-PQX-U3 0000111 = 25/10GBASE-PQX-U2 0000110 = 25/10GBASE-PQX-D3 0000101 = 25/10GBASE-PQX-D2 0000100 = 25/10GBASE-PQG-U3 0000011 = 25/10GBASE-PQG-U2 0000010 = 25/10GBASE-PQG-D3 0000001 = 25/10GBASE-PQG-D2 0000000 = Reserved	R/W

[a]R/W = Read/Write, RO = Read only

PMA/PMD suggestions

- Add Nx25G-EPON PMA/PMD extended ability register
  - Address 1000-1002

Table 45–103b—Nx25G-EPON PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1002.8:15	Reserved	Value always 0	RO
1.1002.7	50GBASE-PQX-U3	1 = PMA/PMD is able to perform 50GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50GBASE-PQX-U3	RO
1.1002.6	50GBASE-PQX-U2	1 = PMA/PMD is able to perform 50GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50GBASE-PQX-U2	RO
1.1002.5	50GBASE-PQX-D3	1 = PMA/PMD is able to perform 50GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50GBASE-PQX-D3	RO
1.1002.4	50GBASE-PQX-D2	1 = PMA/PMD is able to perform 50GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50GBASE-PQX-D2	RO
1.1002.3	50GBASE-PQG-U3	1 = PMA/PMD is able to perform 50GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50GBASE-PQG-U3	RO
1.1002.2	50GBASE-PQG-U2	1 = PMA/PMD is able to perform 50GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50GBASE-PQG-U2	RO
1.1002.1	50GBASE-PQG-D3	1 = PMA/PMD is able to perform 50GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50GBASE-PQG-D3	RO
1.1002.0	50GBASE-PQG-D2	1 = PMA/PMD is able to perform 50GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50GBASE-PQG-D2	RO
1.1001.15	50/25GBASE-PQX-U3	1 = PMA/PMD is able to perform 50/25GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-U3	RO
1.1001.14	50/25GBASE-PQX-U2	1 = PMA/PMD is able to perform 50/25GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-U2	RO
1.1001.13	50/25GBASE-PQX-D3	1 = PMA/PMD is able to perform 50/25GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-D3	RO
1.1001.12	50/25GBASE-PQX-D2	1 = PMA/PMD is able to perform 50/25GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50/25GBASE-PQX-D2	RO
1.1001.11	50/25GBASE-PQG-U3	1 = PMA/PMD is able to perform 50/25GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-U3	RO
1.1001.10	50/25GBASE-PQG-U2	1 = PMA/PMD is able to perform 50/25GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-U2	RO
1.1001.9	50/25GBASE-PQG-D3	1 = PMA/PMD is able to perform 50/25GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-D3	RO
1.1001.8	50/25GBASE-PQG-D2	1 = PMA/PMD is able to perform 50/25GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50/25GBASE-PQG-D2	RO
1.1001.7	50/10GBASE-PQX-U3	1 = PMA/PMD is able to perform 50/10GBASE-PQX-U3 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-U3	RO
1.1001.6	50/10GBASE-PQX-U2	1 = PMA/PMD is able to perform 50/10GBASE-PQX-U2 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-U2	RO
1.1001.5	50/10GBASE-PQX-D3	1 = PMA/PMD is able to perform 50/10GBASE-PQX-D3 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-D3	RO
1.1001.4	50/10GBASE-PQX-D2	1 = PMA/PMD is able to perform 50/10GBASE-PQX-D2 0 = PMA/PMD is not able to perform 50/10GBASE-PQX-D2	RO
1.1001.3	50/10GBASE-PQG-U3	1 = PMA/PMD is able to perform 50/10GBASE-PQG-U3 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-U3	RO
1.1001.2	50/10GBASE-PQG-U2	1 = PMA/PMD is able to perform 50/10GBASE-PQG-U2 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-U2	RO
1.1001.1	50/10GBASE-PQG-D3	1 = PMA/PMD is able to perform 50/10GBASE-PQG-D3 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-D3	RO
1.1001.0	50/10GBASE-PQG-D2	1 = PMA/PMD is able to perform 50/10GBASE-PQG-D2 0 = PMA/PMD is not able to perform 50/10GBASE-PQG-D2	RO
1.1000.15	25GBASE-PQX-U3	1 = PMA/PMD is able to perform 25GBASE-PQX-U3 0 = PMA/PMD is not able to perform 25GBASE-PQX-U3	RO
1.1000.14	25GBASE-PQX-U2	1 = PMA/PMD is able to perform 25GBASE-PQX-U2 0 = PMA/PMD is not able to perform 25GBASE-PQX-U2	RO
1.1000.13	25GBASE-PQX-D3	1 = PMA/PMD is able to perform 25GBASE-PQX-D3 0 = PMA/PMD is not able to perform 25GBASE-PQX-D3	RO
1.1000.12	25GBASE-PQX-D2	1 = PMA/PMD is able to perform 25GBASE-PQX-D2 0 = PMA/PMD is not able to perform 25GBASE-PQX-D2	RO
1.1000.11	25GBASE-PQG-U3	1 = PMA/PMD is able to perform 25GBASE-PQG-U3 0 = PMA/PMD is not able to perform 25GBASE-PQG-U3	RO
1.1000.10	25GBASE-PQG-U2	1 = PMA/PMD is able to perform 25GBASE-PQG-U2 0 = PMA/PMD is not able to perform 25GBASE-PQG-U2	RO
1.1000.9	25GBASE-PQG-D3	1 = PMA/PMD is able to perform 25GBASE-PQG-D3 0 = PMA/PMD is not able to perform 25GBASE-PQG-D3	RO
1.1000.8	25GBASE-PQG-D2	1 = PMA/PMD is able to perform 25GBASE-PQG-D2 0 = PMA/PMD is not able to perform 25GBASE-PQG-D2	RO
1.1000.7	25/10GBASE-PQX-U3	1 = PMA/PMD is able to perform 25/10GBASE-PQX-U3 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-U3	RO
1.1000.6	25/10GBASE-PQX-U2	1 = PMA/PMD is able to perform 25/10GBASE-PQX-U2 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-U2	RO
1.1000.5	25/10GBASE-PQX-D3	1 = PMA/PMD is able to perform 25/10GBASE-PQX-D3 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-D3	RO
1.1000.4	25/10GBASE-PQX-D2	1 = PMA/PMD is able to perform 25/10GBASE-PQX-D2 0 = PMA/PMD is not able to perform 25/10GBASE-PQX-D2	RO
1.1000.3	25/10GBASE-PQG-U3	1 = PMA/PMD is able to perform 25/10GBASE-PQG-U3 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-U3	RO
1.1000.2	25/10GBASE-PQG-U2	1 = PMA/PMD is able to perform 25/10GBASE-PQG-U2 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-U2	RO
1.1000.1	25/10GBASE-PQG-D3	1 = PMA/PMD is able to perform 25/10GBASE-PQG-D3 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-D3	RO
1.1000.0	25/10GBASE-PQG-D2	1 = PMA/PMD is able to perform 25/10GBASE-PQG-D2 0 = PMA/PMD is not able to perform 25/10GBASE-PQG-D2	RO

[a]RO = Read only

PMA/PMD sugge

- Add Nx25G-EPON Synchronization Pattern register
  - Address 1.2400-1.2534

Table 45–103b—Nx25G-EPON Synchronization Pattern register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2534.7:8	SP Register Count	The number of SPx (x = 1, 2, or 3) to be used for responses to GATE messages	R/W
1.2534.5:6	SP Discovery Count	The number of SPx (x = 1, 2, or 3) to be used for Discovery	R/W
1.2534.3	SP3 Register Balanced	Balance setting for SP3 to be used for responses to GATE messages	R/W
1.2534.2	SP3 Discovery Balanced	Balance setting for SP3 to be used for Discovery	R/W
1.2534.1	SP3 Register bit 257	The MSB of the 257-bit SP3 to be used for responses to GATE messages	R/W
1.2534.0	SP3 Discovery bit 257	The MSB of the 257-bit SP3 to be used for Discovery	R/W
1.2533.0 through 1.2533.15	SP3 Register Length	The number of times SP3 is to be repeated for responses to GATE messages	R/W
1.2517.0 through 1.2532.15	SP3 Register	The lower 256 bits of SP3 to be used for responses to GATE messages	R/W
1.2516.0 through 1.2516.15	SP3 Discovery Length	The number of times SP3 is to be repeated for the Register Req	R/W
1.2500.0 through 1.2515.15	SP3 Discovery	The lower 256 bits of SP3 to be used for Discovery	R/W
1.2485 through 1.2499	Reserved	Value always 0	RO
1.2484.4:15	Reserved	Value always 0	RO
1.2484.3	SP2 Register Balanced	Balance setting for SP2 to be used for responses to GATE messages	R/W
1.2484.2	SP2 Discovery Balanced	Balance setting for SP2 to be used for Discovery	R/W
1.2484.1	SP2 Register bit 257	The MSB of the 257-bit SP2 to be used for responses to GATE messages	R/W
1.2484.0	SP2 Discovery bit 257	The MSB of the 257-bit SP2 to be used for Discovery	R/W
1.2483.0 through 1.2483.15	SP2 Register Length	The number of times SP2 is to be repeated for responses to GATE messages	R/W
1.2467.0 through 1.2482.15	SP2 Register	The lower 256 bits of SP2 to be used for responses to GATE messages	R/W
1.2466.0 through 1.2466.15	SP2 Discovery Length	The number of times SP2 is to be repeated for the Register Req	R/W
1.2450.0 through 1.2465.15	SP2 Discovery	The lower 256 bits of SP2 to be used for Discovery	R/W
1.2435 through 1.2449	Reserved	Value always 0	RO
1.2434.4:15	Reserved	Value always 0	RO
1.2434.3	SP1 Register Balanced	Balance setting for SP1 to be used for responses to GATE messages	R/W
1.2434.2	SP1 Discovery Balanced	Balance setting for SP1 to be used for Discovery	R/W
1.2434.1	SP1 Register bit 257	The MSB of the 257-bit SP1 to be used for responses to GATE messages	R/W
1.2434.0	SP1 Discovery bit 257	The MSB of the 257-bit SP1 to be used for Discovery	R/W
1.2433.0:15	SP1 Register Length	The number of times SP1 is to be repeated for responses to GATE messages	R/W
1.2417.0 through 1.2432.15	SP1 Register	The lower 256 bits of SP1 to be used for responses to GATE messages	R/W
1.2416.0:15	SP1 Discovery Length	The number of times SP1 is to be repeated for the Register Req	R/W
1.2400.0 through 1.2415.15	SP1 Discovery	The lower 256 bits of SP1 to be used for Discovery	R/W

[a]R/W = Read/Write, RO = Read only

PMA/PMD changes and additions

Table 45-3

- PMA/PMD Control registers (1.0 & 1.7) provide speed (e.g., 50G, 25G, 10G) and PMD Type (e.g., 10/1GBASE-PRX-D3) selection, among other things.
  - Both 50G and 25G speeds are included (50G from P802.3cd).
  - We will need a new register to select from the number of PMD types being added.
- PMA/PMD Speed Ability registers (1.4) lists all PMDs speeds a device is capable of supporting (one speed/bit). No change needed.
  - To indicate 25/10, 50/10 and 50/25 two points could indicate capability.
  - If we want to explicitly indicate asymmetric rate (as was done for 10/1) we need to add another register.
- PMA/PMD Nx25G-EPON extended ability register (new register set)
  - 1-bit per PMD type
- PMA/PMD register group(s) to indicate Sync Pattern settings (new register set)
  - Do we prefer one register for all (SP1, SP2 & SP3) or
  - One register per pattern (1 for SP1, 1 for SP2 and 1 for SP3)?
- Can possibly use register 1.600 to address pre-coder control.
  - Is this per PHY (1 bit) or per PMA (4 bits)?

PCS changes and additions

Table 45-176

Register Address	Title	Clause	Table	Notes
3.0	PCS control 1	45.2.3.1	Table 45–177	Add 25/10, 50/10, and 50/25
3.4	PCS speed ability	45.2.3.4	Table 45–179	50G added in 802.3cd
3.7	PCS control 2	45.2.3.6	Table 45-180	Add 10 & 25GBASE-Q type PCS
3.9	PCS status 3	45.2.3.8	Table 45–182	Add 10 & 25GBASE-Q type PCS
3.32	BASE-R and MultiGBASE-T PCS status 1 *(mostly test patterns)*	45.2.3.15	Table 45–187	Extend to BASE-Q?
3.33	BASE-R and MultiGBASE-T PCS status 2 *(low order BER & Err blocks)*	45.2.3.16	Table 45–188	mandatory for Nx25G-EPON?
3.44	BER high order counter	45.2.3.21	Table 45–193	mandatory for Nx25G-EPON?
3.74	10GBASE-PR and 10/1GBASE-PRX FEC ability	45.2.3.39	Table 45–211	Extent to 10BASE-Q?
3.75	10GBASE-PR and 10/1GBASE-PRX FEC control	45.2.3.40	Table 45–212	Extent to 10BASE-Q?
3.76, 3.77	10/1GBASE-PRX and 10GBASE-PR corrected FEC codewords counter	45.2.3.41	Table 45–213	Extent to 10BASE-Q?
3.78, 3.79	10/1GBASE-PRX and 10GBASE-PR uncorrected FEC codewords counter	45.2.3.42	Table 45–214	Extent to 10BASE-Q?
3.80	10GBASE-PR and 10/1GBASE-PRX BER monitor timer control	45.2.3.43	Table 45–215	Extent to BASE-Q?
3.81	10GBASE-PR and 10/1GBASE-PRX BER monitor status *(T/F high BER)*	45.2.3.44	Table 45–216	Extent to BASE-Q?
3.82	10GBASE-PR and 10/1GBASE-PRX BER monitor threshold control	45.2.3.45	Table 45–217	Extent to BASE-Q?
3.812 to 3.1799	Reserved			BASE-Q FEC Counters @ 3.900-3.935?
new	PCS FEC corrected codewords counter ch1			32 bits
new	PCS FEC corrected codewords counter ch2			32 bits
new	PCS FEC uncorrected codewords counter ch 1			32 bits
new	PCS FEC uncorrected codewords counter ch 2			32 bits
new	reserved for Nx25G-EPON FEC counters			Allow for additional channels (8/16?)

PCS changes and additions

Table 45-176

- Slightly more complicated as we have at least two PCS channels with associated control and reporting.

- PCS Control registers (3.0 & 3.7) provide speed (e.g., 50G, 25G, 10G) and PCS Type (e.g., 10GBASE-X) selection, among other things.
  - Both 50G and 25G speeds are included (50G from P802.3cd).
  - We will need a control point for PCS type 25GBASE-Q and 10GBASE-Q.
    - Structure only allows selection of a single speed / PCS Type.
    - How to address multiple channels?

PCS changes and additions

Table 45-176

- PCS Status registers (3.1, 3.8, & 3.9) include PCS Type capability
  - Status points needed for PCS type 25GBASE-Q & 10GBASE-Q.
    - Previous PON generations did not change these registers.
    - How to address multiple channels?
- PCS Speed Ability register (3.4) lists all PCS speeds a device is capable of supporting (one speed/bit).
  - Bits 15:10 still open
    - How to address multiple channels?
- BASE-R and MultiGBASE-T PCS (3.32 & 3.33) provide link status, test pattern abilities and BER counter. Extend to Nx25G?
- PCS BER High order counter (3.44) 16-bit BER count. Extend to Nx25G?

PCS changes and additions

Table 45-176

- Multi-lane BASE-R PCS alignment status (3.50-3.53) provide block lock status. Extend to Nx25G?
- 10/1GBASE-PRX & 10GBASE-PR FEC codeword counters (3.76-3.79) uncorrected & corrected FEC blocks. Extend to 10GBASE-Q?
- 10/1GBASE-PRX & 10GBASE-PR BER monitor (3.80-3.82) timer control, status & threshold control. Extend to 10GBASE-Q?

- New registers needed for
  - Nx25G-EPON PCS Control, Status, and Speed ability registers?
  - Nx25G-EPON PCS FEC codeword counters;
    - 32-bit counters for each channel / corrected FEC CW's / uncorrected FEC CW's.
    - Reserve space for additional channel counters ?

PMA suggestions

- Change Table 45-177 as shown

Table 45–177—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.0.5:2	Speed selection	5432 ~~11xx~~ 1110 = reserved 1101 = 50/25 Gb/s 1100 = 50/10 Gb/s 1011 = 25/10 Gb/s 1010 = 400 Gb/s 1001 = 200 Gb/s 1000 = 5 Gb/s 0111 = 2.5 Gb/s 0110 = 50 Gb/s 0101 = 25 Gb/s 0100 = 100 Gb/s 0011 = 40 Gb/s 0010 = 10/1 Gb/s 0001 = 10PASS-TS/2BASE-TL 0000 = 10 Gb/s	R/W

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

PMA suggestions

- Change Table 45-180 as shown

Table 45–180—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
~~3.7.15:4~~ 3.7.15:5	Reserved	Value always 0	RO
~~3.7.3:0~~ 3.7.4:0	PCS type selection	~~3210~~ 43210 10100 = Select 50GBASE-Q PCS type 10011 = Select 50/25GBASE-Q PCS type 10010 = Select 50/10GBASE-Q PCS type 10001 = Select 25GBASE-Q PCS type 10000 = Select 25/10GBASE-Q PCS type 0111x = reserved 01101 = Select 400GBASE-R PCS type 01100 = Select 200GBASE-R PCS type 01011 = Select 5GBASE-T PCS type 01010 = Select 2.5GBASE-T PCS type 01001 = Select 25GBASE-T PCS type 01000 = Select 50GBASE-R PCS type 00111 = Select 25GBASE-R PCS type 00110 = Select 40GBASE-T PCS type 00101 = Select 100GBASE-R PCS type 00100 = Select 40GBASE-R PCS type 00011 = Select 10GBASE-T PCS type 00010 = Select 10GBASE-W PCS type 00001 = Select 10GBASE-X PCS type 00000 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

PMA suggestions

- Change Table 45-182 as shown

Table 45–182—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
~~3.9.15:2~~ 3.9.15:5	Reserved	Value always 0	RO
3.9.4	2x25GBASE-Q capable	1 = PCS is able to support 2x25GBASE-Q PCS type 0 = PCS is not able to support 2x25GBASE-Q PCS type	RO
3.9.3	25GBASE-Q capable	1 = PCS is able to support 25GBASE-Q PCS type 0 = PCS is not able to support 25GBASE-Q PCS type	RO
3.9.2	10GBASE-Q capable	1 = PCS is able to support10GBASE-Q PCS type 0 = PCS is not able to support 10GBASE-Q PCS type	RO
3.9.1	400GBASE-R capable	1 = PCS is able to support 400GBASE-R PCS type 0 = PCS is not able to support 400GBASE-R PCS type	RO
3.9.0	200GBASE-R capable	1 = PCS is able to support 200GBASE-R PCS type 0 = PCS is not able to support 200GBASE-R PCS type	RO

aRO = Read only

PMA suggestions

- Add Table 45-237a as shown

Table 45–237a—BASE-Q PCS FEC corrected codewrds counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.812 though ~~3.1799~~ 3.899	reserved	Value always 0	RO
3.900.15:0	FEC corrected codewords lower	PCS FEC corrected codewords counter ch1 (15:0)	RO, NR
3.901.15:0	FEC corrected codewords upper	PCS FEC corrected codewords counter ch1 (31:16)	RO, NR
3.902.15:0	FEC corrected codewords lower	PCS FEC corrected codewords counter ch2 (15:0)	RO, NR
3.903.15:0	FEC corrected codewords upper	PCS FEC corrected codewords counter ch3 (31:16)	RO, NR

aRO = Read only, NR = Non Roll-over

PMA suggestions

- Add Table 45-237b as shown

Table 45–237b—BASE-Q PCS FEC uncorrected codewrds counter register bit definitions

3.904 through 3.931	reserved	Value always 0	RO
3.932.15:0	FEC uncorrected codewords lower	PCS FEC corrected codewords counter ch1 (15:0)	RO, NR
3.933.15:0	FEC uncorrected codewords upper	PCS FEC corrected codewords counter ch1 (31:16)	RO, NR
3.934.15:1	FEC uncorrected codewords lower	PCS FEC corrected codewords counter ch2 (15:0)	RO, NR
3.935.15:1	FEC uncorrected codewords upper	PCS FEC corrected codewords counter ch3 (31:16)	RO, NR
3.936 through 3.1799	reserved	Value always 0	RO

aRO = Read only, NR = Non Roll-over

PHY XS

- Table 45-245 (FYI only)

Register Address	Title	Clause
4.0	PHY XS control 1	45.2.4.1
4.1	PHY XS status 1	45.2.4.2
4.2, 4.3	PHY XS device identifier	45.2.4.3
4.4	PHY XS speed ability	45.2.4.4
4.5, 4.6	PHY XS devices in package	45.2.4.5
4.8	PHY XS status 2	45.2.4.6
4.14, 4.15	PHY XS package identifier	45.2.4.7
4.20	EEE capability	45.2.4.8
4.22	EEE wake error counter	45.2.4.9
4.24	10G PHY XGXS lane status	45.2.4.10
4.25	10G PHY XGXS test control	45.2.4.11
4.32	BASE-R PHY XS status 1	45.2.4.12
4.42	BASE-R PHY XS test pattern control	45.2.4.13
4.50	Multi-lane BASE-R PHY XS alignment status 1	45.2.4.14
4.52	Multi-lane BASE-R PHY XS alignment status 3	45.2.4.15
4.53	Multi-lane BASE-R PHY XS alignment status 4	45.2.4.16
4.400 to 4.415	PHY XS lane mapping, lane 0 through 15	45.2.4.17, 45.2.4.18
4.600 to 4.631	PHY XS FEC symbol error counter, lane 0 to 15	45.2.4.19, 45.2.4.20
4.800	PHY XS FEC control	45.2.4.21
4.801	PHY XS FEC status	45.2.4.22
4.802, 4.803	PHY XS FEC corrected codewords counter	45.2.4.23
4.804, 4.805	PHY XS FEC uncorrected codewords counter	45.2.4.24
4.806, 4.807	PHY XS FEC degraded SER activate threshold	45.2.4.25
4.808, 4.809	PHY XS FEC degraded SER deactivate threshold	45.2.4.26
4.810, 4.811	PHY XS FEC degraded SER interval	45.2.4.27
4.1800	TimeSync PHY XS capability	45.2.4.28
4.1801 to 4.1804	TimeSync PHY XS transmit path data delay	45.2.4.29
4.1805 to 4.1808	TimeSync PHY XS receive path data delay	45.2.4.30

Call for Volunteers

Nx25G-EPON wants

YOU

to step up and contribute!

"YOU"s who have already contributed significantly are exempt from this Call

To be Resolved

- How to address multiple PCS channels for
  - PCS Control - Type & Speed selection
  - PCS Speed capability

- Missing anything?
  - PMA/PMD
  - PCS
  - Elsewhere

Thank You

Especially if you answer the call on slide 7

☺

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:10	Reserved	Value always 0	RO
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W
1.7.7	Reserved	Value always 0	RO
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 1 1 x x x x x = reserved 1 0 1 1 1 1 x = reserved 1 0 1 1 1 0 1 = reserved 1 0 1 1 1 0 0 = 400GBASE-LR8 PMA/PMD 1 0 1 1 0 1 1 = 400GBASE-FR8 PMA/PMD 1 0 1 1 0 1 0 = 400GBASE-DR4 PMA/PMD 1 0 1 1 0 0 1 = 400GBASE-SR16 PMA/PMD 1 0 1 1 0 0 0 = reserved 1 0 1 0 1 1 x = reserved 1 0 1 0 1 0 1 = 200GBASE-LR4 PMA/PMD 1 0 1 0 1 0 0 = 200GBASE-FR4 PMA/PMD 1 0 1 0 0 1 1 = 200GBASE-DR4 PMA/PMD 1 0 1 0 0 1 0 = reserved 1 0 1 0 0 0 x = reserved 1 0 0 x x x x = reserved 0 1 1 1 1 1 x = reserved	R/W

Table 45-14--PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/Wa
1.11.15	BASE-H extended abilities	1 = PMA/PMD has BASE-H extended abilities listed in register 1.22 0 = PMA/PMD does not have BASE-H extended abilities	RO
1.11.14	2.5G/5G extended abilities	1 = PMA/PMD has 2.5G/5G extended abilities listed in register 1.21 0 = PMA/PMD does not have 2.5G/5G extended abilities	RO
1.11.13	200G/400G extended abilities	1 = PMA/PMD has 200G/400G extended abilities listed in register 1.23 or register 1.24 0 = PMA/PMD does not have 200G/400G extended abilities	RO
1.11.12	25G extended abilities	1 = PMA/PMD has 25G extended abilities listed in register 1.19 0 = PMA/PMD does not have 25G extended abilities	RO
1.11.11	BASE-T1 extended abilities	1 = PMA/PMD has BASE-T1 extended abilities listed in register 1.18 0 = PMA/PMD does not have BASE-T1 extended abilities	RO
1.11.10	40G/100G extended abilities	1 = PMA/PMD has 40G/100G extended abilities listed in register 1.13 0 = PMA/PMD does not have 40G/100G extended abilities	RO
1.11.9	P2MP ability	1 = PMA/PMD has P2MP abilities listed in register 1.12 0 = PMA/PMD does not have P2MP abilities	RO
1.11.8	10BASE-T ability	1 = PMA/PMD is able to perform 10BASE-T 0 = PMA/PMD is not able to perform 10BASE-T	RO
1.11.7	100BASE-TX ability	1 = PMA/PMD is able to perform 100BASE-TX 0 = PMA/PMD is not able to perform 100BASE-TX	RO
1.11.6	1000BASE-KX ability	1 = PMA/PMD is able to perform 1000BASE-KX 0 = PMA/PMD is not able to perform 1000BASE-KX	RO
1.11.5	1000BASE-T ability	1 = PMA/PMD is able to perform 1000BASE-T 0 = PMA/PMD is not able to perform 1000BASE-T	RO
1.11.4	10GBASE-KR ability	1 = PMA/PMD is able to perform 10GBASE-KR 0 = PMA/PMD is not able to perform 10GBASE-KR	RO
1.11.3	10GBASE-KX4 ability	1 = PMA/PMD is able to perform 10GBASE-KX4 0 = PMA/PMD is not able to perform 10GBASE-KX4	RO
1.11.2	10GBASE-T ability	1 = PMA/PMD is able to perform 10GBASE-T 0 = PMA/PMD is not able to perform 10GBASE-T	RO
1.11.1	10GBASE-LRM ability	1 = PMA/PMD is able to perform 10GBASE-LRM 0 = PMA/PMD is not able to perform 10GBASE-LRM	RO
1.11.0	10GBASE-CX4 ability	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO

Table 45–180—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.7.15:4	Reserved	Value always 0	RO
3.7.3:0	PCS type selection	3 2 1 0 1 1 1 x = reserved 1 1 0 1 = Select 400GBASE-R PCS type 1 1 0 0 = Select 200GBASE-R PCS type 1 0 1 1 = Select 5GBASE-T PCS type 1 0 1 0 = Select 2.5GBASE-T PCS type 1 0 0 1 = Select 25GBASE-T PCS type 1 0 0 0 = reserved 0 1 1 1 = Select 25GBASE-R PCS type 0 1 1 0 = Select 40GBASE-T PCS type 0 1 0 1 = Select 100GBASE-R PCS type 0 1 0 0 = Select 40GBASE-R PCS type 0 0 1 1 = Select 10GBASE-T PCS type 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 = Select 10GBASE-R PCS type	R/W

[a]RO = Read only, R/W = Read/Write

Table 45–181—PCS status 2 register bit definitions

Bit(s)	Name	Description	R/Wa
3.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
3.8.13	5GBASE-T capable	1 = PCS is able to support 2.5GBASE-T PCS type 0 = PCS is not able to support 2.5GBASE-T PCS type	RO
3.8.12	2.5GBASE-T capable	1 = PCS is able to support 5GBASE-T PCS type 0 = PCS is not able to support 5GBASE-T PCS type	RO
3.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO
3.8.10	Receive fault	1 = Fault condition on the receive path 0 = No fault condition on the receive path	RO
3.8.9	25GBASE-T capable	1 = PCS is able to support 25GBASE-T PCS type 0 = PCS is not able to support 25GBASE-T PCS type Value always 0	RO
3.8.8	Reserved	Value always 0	RO
3.8.7	25GBASE-R capable	1 = PCS is able to support 25GBASE-R PCS type 0 = PCS is not able to support 25GBASE-R PCS type	RO
3.8.6	40GBASE-T capable	1 = PCS is able to support 40GBASE-T PCS type 0 = PCS is not able to support 40GBASE-T PCS type	RO
3.8.5	100GBASE-R capable	1 = PCS is able to support 100GBASE-R PCS type 0 = PCS is not able to support 100GBASE-R PCS type	RO
3.8.4	40GBASE-R capable	1 = PCS is able to support 40GBASE-R PCS type 0 = PCS is not able to support 40GBASE-R PCS type	RO
3.8.3	10GBASE-T capable	1 = PCS is able to support 10GBASE-T PCS type 0 = PCS is not able to support 10GBASE-T PCS type	RO
3.8.2	10GBASE-W capable	1 = PCS is able to support 10GBASE-W PCS type 0 = PCS is not able to support 10GBASE-W PCS type	RO
3.8.1	10GBASE-X capable	1 = PCS is able to support 10GBASE-X PCS type 0 = PCS is not able to support 10GBASE-X PCS type	RO
3.8.0	10GBASE-R capable	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types	RO

Table 45–182—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.9.15:2	Reserved	Value always 0	RO
3.9.1	400GBASE-R capable	1 = PCS is able to support 400GBASE-R PCS type 0 = PCS is not able to support 400GBASE-R PCS type	RO
3.9.0	200GBASE-R capable	1 = PCS is able to support 200GBASE-R PCS type 0 = PCS is not able to support 200GBASE-R PCS type	RO

[a]RO = Read only

Table 45–187—BASE-R and MultiGBASE-T PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.32.15:13	Reserved	Value always 0	RO
3.32.12	BASE-R and MultiGBASE-T receive link status	1 = BASE-R or any MultiGBASE-T PCS receive link up 0 = BASE-R or any MultiGBASE-T PCS receive link down	RO
3.32.11:4	Reserved	Value always 0	RO
3.32.3	10GBASE-R PRBS9 pattern testing ability	1 = PCS is able to support PRBS9 pattern testing 0 = PCS is not able to support PRBS9 pattern testing	RO
3.32.2	10GBASE-R PRBS31 pattern testing ability	1 = PCS is able to 0 = PCS is not ab	
3.32.1	BASE-R and MultiGBASE-T PCS high BER	1 = BASE-R or a 0 = BASE-R or a BER	
3.32.0	BASE-R and MultiGBASE-T PCS block lock	1 = BASE-R or a blocks 0 = BASE-R or a blocks	

[a]RO = Read only

Table 45–188—BASE-R and MultiGBASE-T PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.33.15	Latched block lock	1 = BASE-R or any MultiGBASE-T PCS has block lock 0 = BASE-R or any MultiGBASE-T PCS does not have block lock	RO/LL
3.33.14	Latched high BER	1 = BASE-R or any MultiGBASE-T PCS has reported a high BER 0 = BASE-R or any MultiGBASE-T PCS has not reported a high BER	RO/LH
3.33.13:8	BER	BER counter	RO/NR
3.33.7:0	Errored blocks	Errored blocks counter	RO/NR

[a]RO = Read only, LL = Latching low, LH = Latching high, NR = Non Roll-over

Table 45–193—BER high order counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.44.15:0	BER high order	Bits 21:6 of BER counter	

[a]RO = Read only

Table 45–194—Errored blocks high order counter regis

Bit(s)	Name	Description
3.45.15	High order counter present	Always reads as one if this register
3.45.14	Reserved	Value always 0
3.45.13:0	Errored blocks high order	Bits 21:8 of errored blocks counter

[a]RO = Read only

Table 45–195—Multi-lane BASE-R PCS alignment status 1 register bit definitions

Bit(s)	Name	Description	R/Wa
3.50.15:13	Reserved	Value always 0	RO
3.50.12	PCS lane alignment status	1 = PCS receive lanes locked and aligned 0 = PCS receive lanes not locked and aligned	RO
3.50.11:8	Reserved	Value always 0	RO
3.50.7	Block lock 7	1 = Lane 7 is locked 0 = Lane 7 is not locked	RO
3.50.6	Block lock 6	1 = Lane 6 is locked 0 = Lane 6 is not locked	RO
3.50.5	Block lock 5	1 = Lane 5 is locked 0 = Lane 5 is not locked	RO
3.50.4	Block lock 4	1 = Lane 4 is locked 0 = Lane 4 is not locked	RO
3.50.3	Block lock 3	1 = Lane 3 is locked 0 = Lane 3 is not locked	RO
3.50.2	Block lock 2	1 = Lane 2 is locked 0 = Lane 2 is not locked	RO
3.50.1	Block lock 1	1 = Lane 1 is locked 0 = Lane 1 is not locked	RO
3.50.0	Block lock 0	1 = Lane 0 is locked 0 = Lane 0 is not locked	RO

Table 45–213—10GBASE-PR corrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.76.15:0	corrected FEC codewords lower	corrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.77.15:0	corrected FEC codewords upper	corrected_FEC_codewords_counter[31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word. NR = Non Roll-over

Table 45–214—10GBASE-PR uncorrected FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.78.15:0	uncorrected FEC codewords lower	uncorrected_FEC_codewords_counter[15:0]	RO, MW, NR
3.79.15:0	uncorrected FEC codewords lower	uncorrected_FEC_codewords_counter[32:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word. NR = Non Roll-over

Table 45–215—10GBASE-PR and 10/1GBASE-PRX BER monitor timer control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.80.15:8	Reserved	Value always 0	RO
3.80.7:0	10G-EPON BER monitor timer	Duration (in units of 5 microseconds) of the timer used by the 10G-EPON BER monitor function. Default value is 25 (i.e., 125 microseconds). A value of zero indicates that the BER monitor function is disabled.	R/W

[a]RO = Read only, R/W = Read/Write

Table 45–216—10GBASE-PR and 10/1GBASE-PRX BER monitor status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.81.15:2	Reserved	Value always 0	RO
3.81.1	Latched high BER	1 = 10GBASE-PR or 10/1GBASE-PRX PCS reported a high BER. 0 = 10GBASE-PR or 10/1GBASE-PRX PCS did not report a high BER.	RO, LH
3.81.0	high BER	1 = 10GBASE-PR or 10/1GBASE-PRX PCS reporting a high BER. 0 = 10GBASE-PR or 10/1GBASE-PRX PCS not reporting a high BER.	RO

[a]RO Read only, LH = Latching high

Table 45–217—10GBASE-PR and 10/1GBASE-PRX BER monitor threshold control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.82.15:0	10G-EPON BER monitor threshold	Number of sync header errors within a timer interval that triggers a high BER condition for the 10G-EPON BER monitor function. Default value is 1600. A value of zero indicates that the BER monitor function is disabled.	R/W

[a]R/W = Read/Write

Intended Straw Polls

Straw Poll

Do you prefer one register group for SP1, SP2 & SP3 (1 group of Discover & another for normal operation) or

One register per pattern (2 for SP1, 2 for SP2 and 2 for SP3)?

One group register for SP1, SP2 & SP3 with
2 groups; one for Discovery and
one for Normal operation _____

One register for SP1 Discovery, another for SP1

Normal, another for SP2 Discovery, … _____

Vote for one

Straw Poll

Pre-coder control should be per PHY (1 bit for all PMAs).

Agree _____

Disagree _____

Don’t know _____

Vote for one

Straw Poll

For PCS registers do we Extend existing registers where possible or define a complete new set (i.e., n channels for Control, Speed Ability, Status, etc.

Extend where possible _____

Complete new set _____

No opinion _____

Vote for one

Straw Poll

How many channels to we target for PCS Registers?

Only 2 _____

4 (2 + 2 reserved) _____

8 (2 + 6 reserved) _____

> 8 _____

Vote for one

Motion

Move to adopt the tables shown on remein_3ca_2a.pdf slides 5-7 and 13-17 and include in Draft 1.4.

Moved:

Second:

For: _____

Against: _____

Abstain: _____

Motion Technical (> 75%) Motion Passed/Failed