45. Management Data Input/Output (MDIO) Interface

45.2.1 PMA/PMD registers

Change rows in Table 45–3 (as modified by IEEE Std 802.3cb-2018 and IEEE Std 802.cd-2018) as shown below:

Table 45–3—PCS registers

Register address	Register name	Subclause
...	...	....
3.80	10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor timer control	45.2.3.43
3.81	10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor status	45.2.3.44
3.82	10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor threshold control	45.2.3.45
...	...	...

Update 45.2.3.43, 45.2.3.44, and 45.2.3.45 as shown below:

45.2.3.43 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor interval ~~timer~~ control register (Register 3.80)

The assignment of bits in the 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor interval ~~timer~~ control register is shown in Table 45–215. This register is defined only when 10GBASE-PR ~~or~~, 10/1GBASE-PRX, or Nx25G EPON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G EPON LDPC BER monitor is described in 142.3.5.6.

Table 45–215—10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor interval ~~timer~~ control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.80.15:8	Reserved	Value always 0	RO
3.80.7:0	~~10G~~-EPON BER monitor ~~timer~~ interval	For 10GBASE-PR and 10/1GBASE-PRX: Duration (in units of 5 micro-seconds) of the timer used by the ~~10G-EPON~~ BER monitor function. Default value is 25 (i.e., 125 micro seconds). A value of zero indicates that the BER monitor function is disabled. For Nx25G EPON: LDPC codeword count (in units of 16 codewords) of the monitoring interval used by the BER monitor function. Default value is 12 (i.e., 192 codewords).	R/W

[a]RO = Read only, R/W = Read/Write

45.2.3.44 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor status (Register 3.81)

The assignment of bits in the 10GBASE-PR ~~and~~, 10/1GBASE-PRX BER, and Nx25G EPON monitor status register is shown in Table 45–216. This register is defined only when 10GBASE-PR ~~or~~, 10/1GBASE-PRX, or Nx25G EPON ONU capability is supported.

Table 45–216—10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor status register bit definitions

Bit(s)	Name	Description	R/W[a]
3.81.15:2	Reserved	Value always 0	RO
3.81.1	Latched high BER	10GBASE-PR, 10/1GBASE-PRX, or Nx25G EPON PCS: 1 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ reported a high BER. 0 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ did not report a high BER.	RO, LH
3.81.0	high BER	10GBASE-PR, 10/1GBASE-PRX, or Nx25G EPON PCS: 1 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ reporting a high BER. 0 = 10GBASE-PR or 10/1GBASE-PRX PCS not reporting a high BER.	RO

[a]RO Read only, LH = Latching high

45.2.3.44.1 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON PCS high BER (3.81.0)

In the 10GBASE-PR ~~and~~,10/1GBASE-PRX BER, and Nx25G EPON PCS, when read as a one, bit 3.81.0 indicates that the receiver is detecting a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.0 indicates that the receiver is detecting a BER lower than the configurable threshold (low BER state). This bit mirrors the state of the hi_ber variable, defined in 76.3.3.4 for 10GBASE-PR and, 10/1GBASE-PRX, and the HiBer variable in 142.3.5.2 for Nx25G EPON.

45.2.3.44.2 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON PCS latched high BER (3.81.1)

In the 10GBASE-PR ~~and~~, 10/1GBASE-PRX BER, and Nx25G EPON, when read as a one, bit 3.81.1 indicates that the receiver detected a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.1 indicates that the receiver detected BER lower than the configurable threshold (low BER state).

This bit is a latching high version of the 10GBASE-PR ~~and~~, 10/1GBASE-PRX BER, and Nx25G EPON high BER status bit (3.81.0).

45.2.3.45 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor threshold control (Register 3.82)

The assignment of bits in the 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor threshold control register is shown in Table 45–217. This register is defined only when 10GBASE-PR ~~or~~,

10/1GBASE-PRX, or Nx25G EPON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G EPON LDPC BER monitor is described in 142.3.5.6

Table 45–217—10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G EPON BER monitor threshold control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.82.15:0	~~10G-~~EPON BER monitor threshold	For 10G-EPON: n~~N~~umber of sync header errors within a timer interval that triggers a high BER condition for the ~~10G-EPON~~ BER monitor function. Default value is 1600. A value of zero indicates that the BER monitor function is disabled. For Nx25G EPON: number of invalid LDPC codeword parity checks within a BER monitor interval that triggers a high BER condition for the BER monitor function. Default value is 18. A value of zero indicates that the BER monitor function is disabled.	R/W

[a]R/W = Read/Write