Annex 128A

(normative)

2.5Gb/s Storage Enclosure Interface (2.5GSEI)

128A.1 Overview

This clause defines the functional and electrical characteristics for 2.5GSEI. This interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with pluggable storage drive module interfaces. Figure 128A–1 shows the test point locations associated with 2.5GSEI.

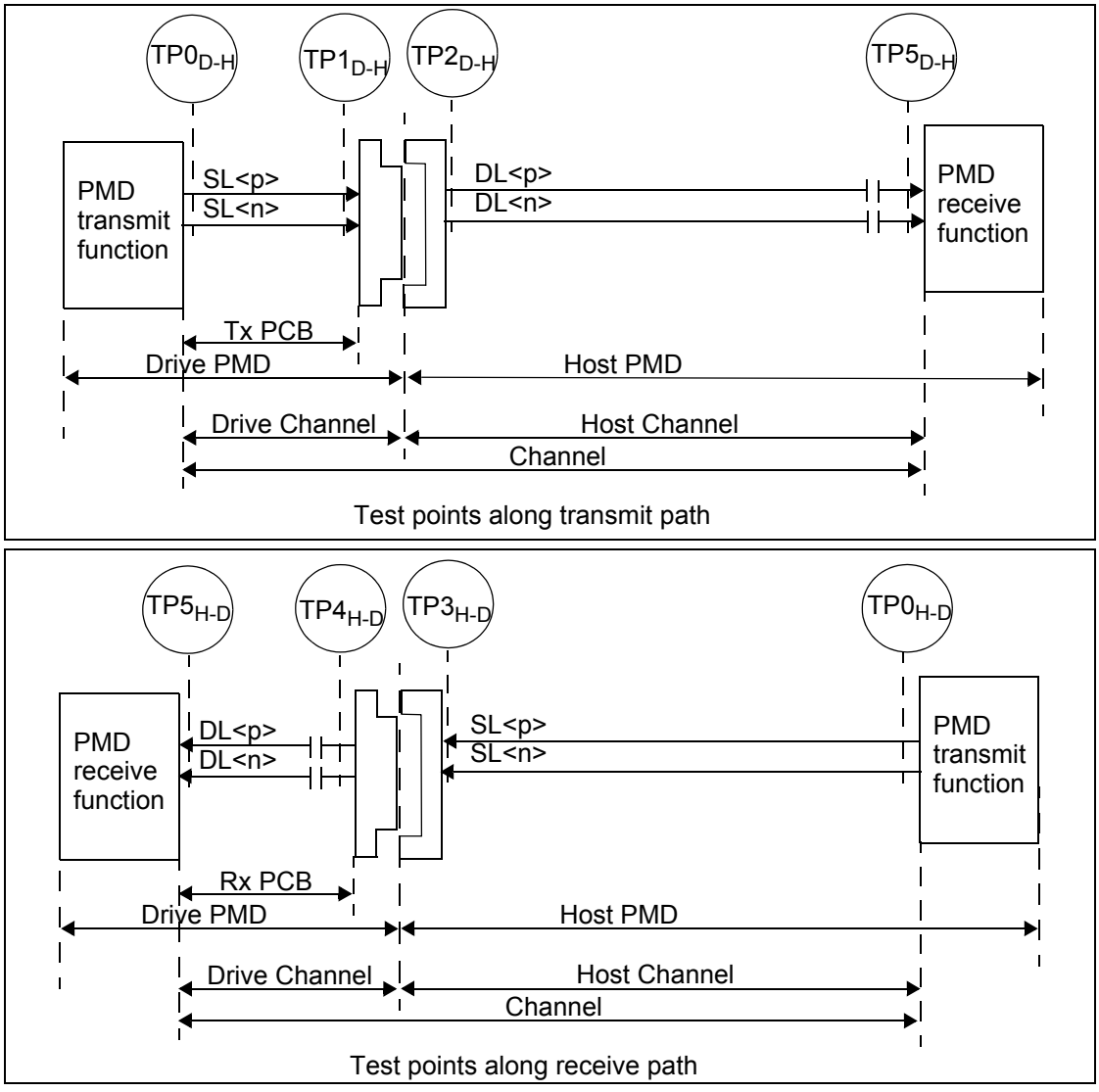
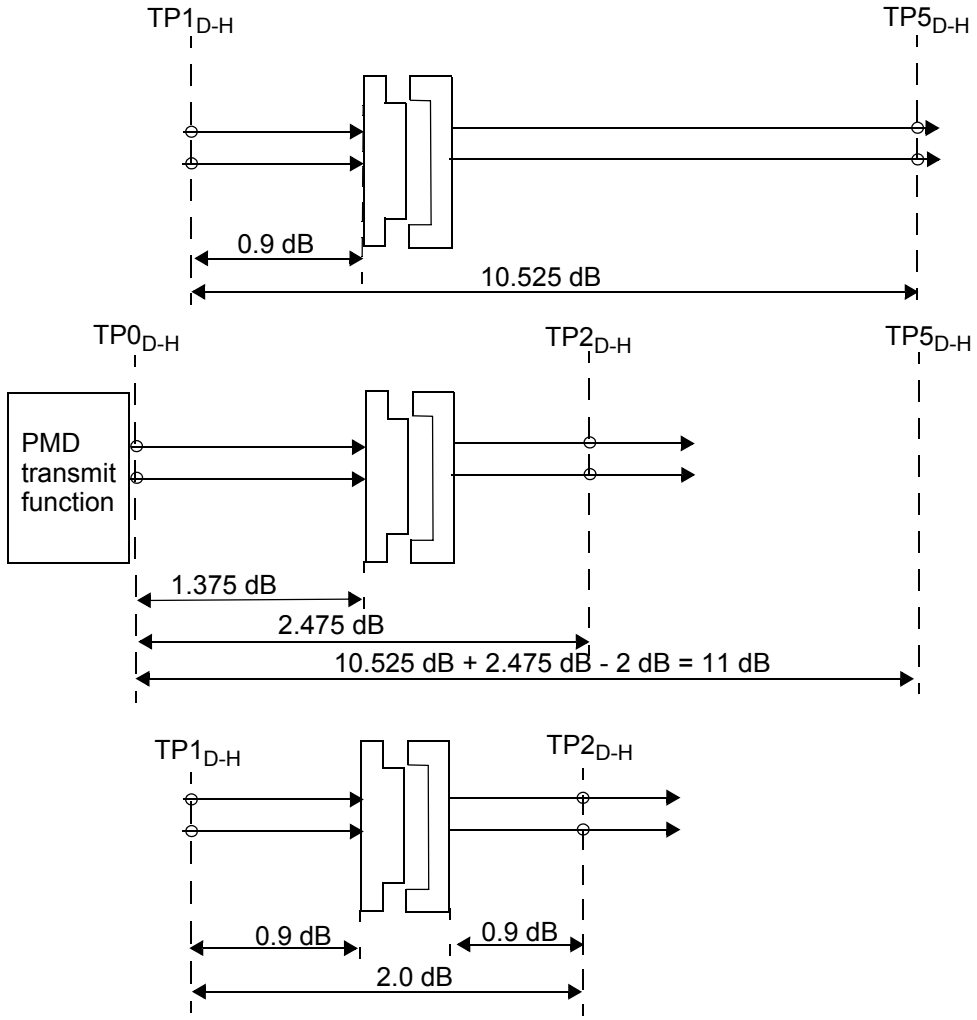


Figure 128A–1—Test points

The 2.5GSEI link is described in terms of a host 2.5GSEI component with associated insertion loss and a drive 2.5GSEI component. Figure 128A–2 (one direction shown) and Equation (128A–1) depict a typical 2.5GSEI application and summarize the informative differential insertion loss budget, which is shown in Figure 128A–3. The 2.5GSEI interface comprises of independent data paths in each direction. Each data path contains one differential lane, which is AC-coupled on the receiver side. The nominal signaling rate for each lane is 3.125 GBd.



NOTE-- The connector insertion loss is 0.2 dB for the mated test fixture.

Figure 128A–2—Insertion loss budget at 2.578125 GHz

$$Insertion\_loss(f) \le \left\{ \begin{array}{cc} 0.668 + 3.755\sqrt{f} + 3.608f & 0.05 \le f < 1.5625 \\ -23.753 + 22.242f & 1.5625 \le f < 2.34375 \end{array} \right\} \text{ (dB)} \qquad (128A–1)$$

where

f	is the frequency in GHz
Insertion_loss(f)	chip to chip (C2C) insertion loss

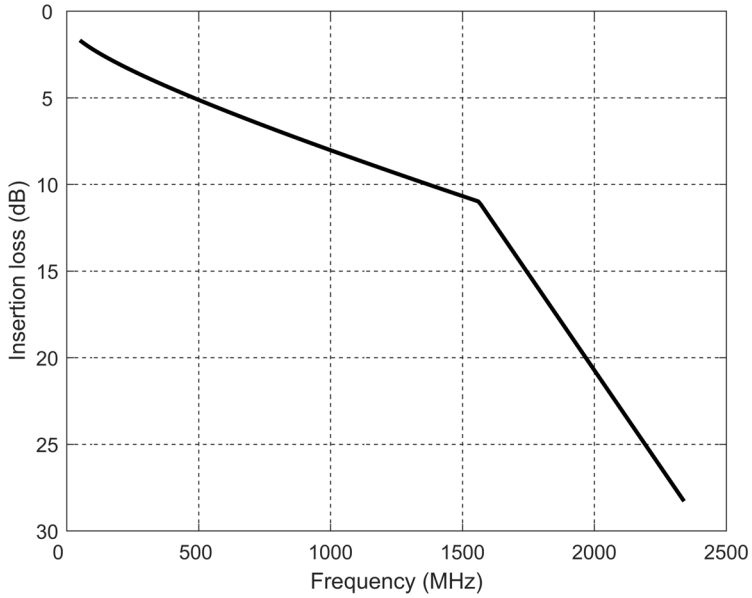


Figure 128A–3—Chip-to-chip insertion loss

128A.1.1 Bit error ratio

The bit error ratio (BER) shall be less than 10^{-12} with any errors sufficiently un-correlated to ensure an acceptably high mean time to false packet acceptance (MTTFPA) assuming 8B/10B coding.

128A.2 2.5GSEI compliance point definitions

The electrical characteristics for 2.5GSEI are defined at compliance points for the host and drive, respectively. Reference test fixtures, called compliance boards, are used to access the electrical specification parameters. Figure 128A–4 depicts the location of compliance points when measuring host 2.5GSEI compliance. The output of the Host Compliance Board (HCB) is used to verify the host electrical output signal at $TP4_{H\text{-}D}$. Similarly, the input of the HCB at $TP1_{D\text{-}H}$ is used to verify the host input compliance.

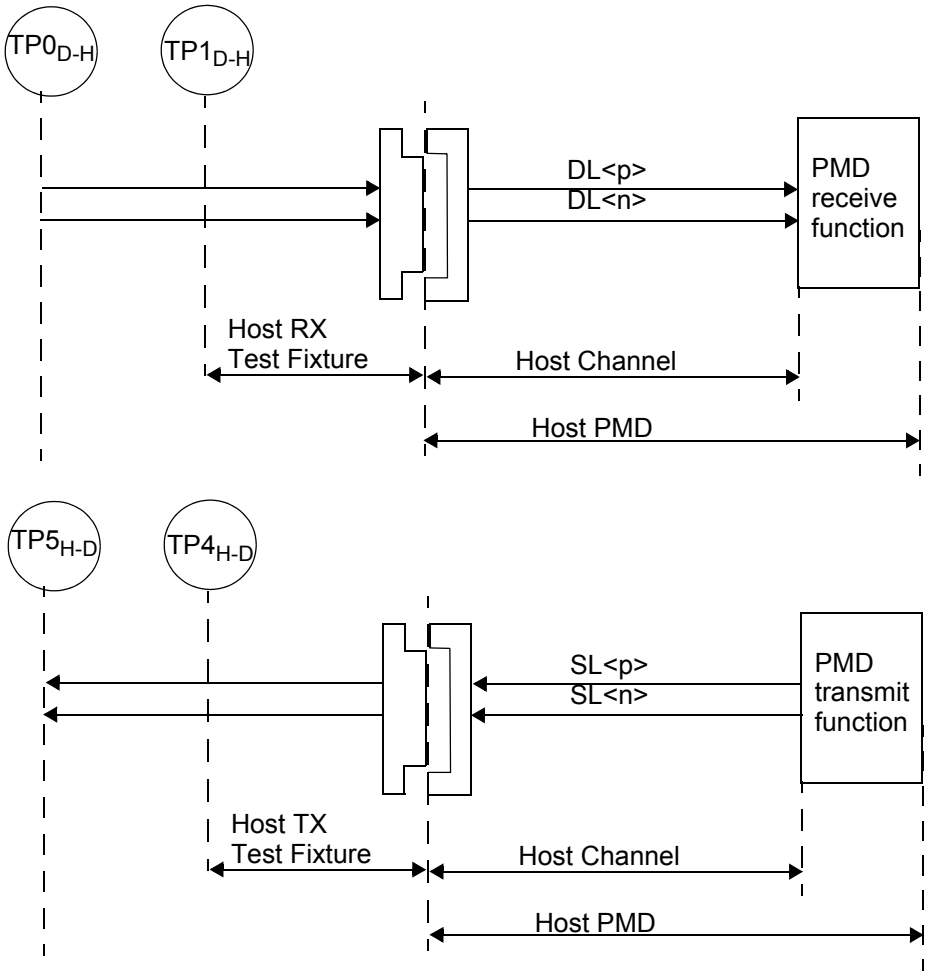


Figure 128A–4—Host compliance board

Figure 128A–5 depicts the location of compliance points when measuring drive 2.5GSEI compliance. The output of the Drive Compliance Board (DCB) is used to verify the host electrical output signal at $TP2_{D\text{-}H}$. Similarly, the input of the DCB at $TP3_{H\text{-}D}$ is used to verify the host input compliance. Additional details on the requirements for the HCB and DCB are given in Annex 128D.

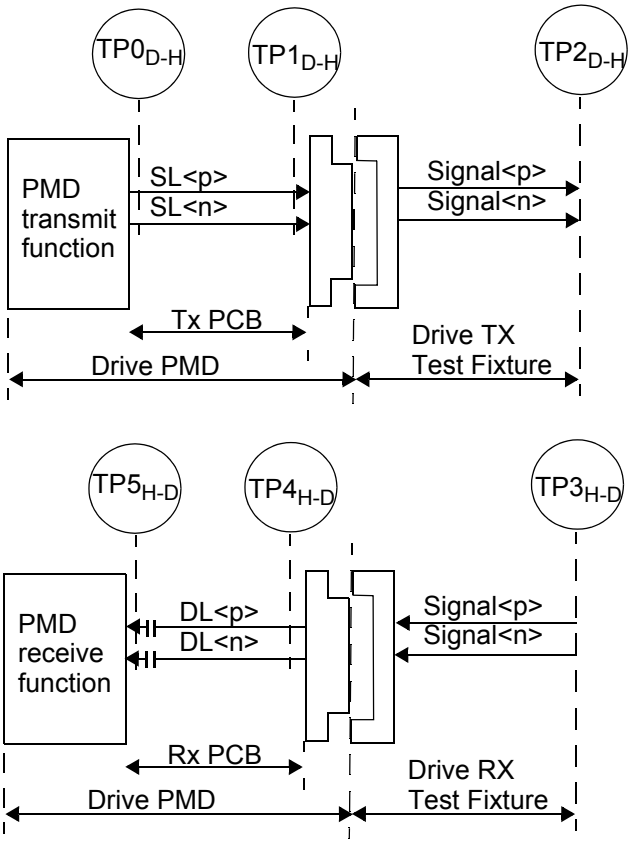


Figure 128A–5—Drive compliance board

128A.3 2.5GSEI electrical characteristics

128A.3.1 2.5GSEI host output characteristics

A 2.5GSEI host output shall meet the specifications defined in Table 128A–1 if measured at $TP4_{H\text{-}D}$.

Table 128A–1—2.5GSEI host output characteristics

Parameter	Subclause reference	Value	Units
Signaling rate	128A.3.1.1	3.125 ± 100 ppm	GBd
DC common-mode output voltage (max.)	128A.3.1.2	1.9	V
AC common-mode output voltage (max, RMS)	128A.3.1.2	30	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	128A.3.1.2	 35 1200	 mV mV
Differential output return loss (min.)	128A.3.1.3	See Equation (128A–1) and Equation (128A–2)	dB
Output waveform Transmitter steady-state voltage, vf (max.) Transmitter steady-state voltage, vf (min.) Linear fit pulse peak (min)	 128A.3.1.4.2 128A.3.1.4.2 128A.3.1.4.2	 600 400 0.42	 mV mV mV
Max output jitter (peak-to-peak) Random jitter Deterministic jitter Duty Cycle Distortion Total jitter	 128A.3.1.6	 0.20 0.12 0.035 0.35	 UI UI UI UI
Signal-to-noise-and-distortion ratio (min)	128A.3.1.7	5.6	dB

A test system with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

128A.3.1.1 Signaling rate and range

The 2.5GSEI signaling rate is 3.125 GBd ± 100 ppm. This translates to a nominal unit interval of 320 ps.

128A.3.1.2 Signaling levels

The differential output voltage V_d is defined to be the difference between the single-ended output voltages, *SL*<*p*> minus *SL*<*n*>. The common-mode voltage V_{cm} is defined to be one half of the sum of *SL*<*p*> and *SL*<*n*>. These definitions are illustrated by Figure 128A–6.

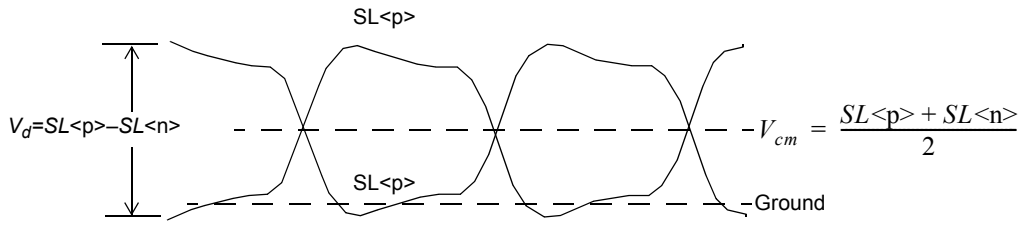


Figure 128A–6—Voltage definitions

The peak-to-peak differential output voltage is less than or equal to 1200 mV. The peak-to-peak differential output voltage is less than or equal to 35 mV when the transmitter is disabled. The DC common-mode output voltage and AC common-mode output voltage are defined with respect to signal ground.

128A.3.1.3 Output return loss

The differential output return loss, in dB, of the output is shown in Equation (128A–2) and illustrated in Figure 128A–7. This output requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$Return\_loss(f) \geq \begin{cases} Return\_loss_{min} = 12 & 50 \leq f < 275 \\ Return\_loss_{min} = 12 - 6.75\log_{10}\left(\frac{f}{275\,\text{MHz}}\right) & 275 \leq f < 2343.75 \end{cases} \text{(dB)} \qquad \text{(128A–2)}$$

where

f is the frequency in MHz

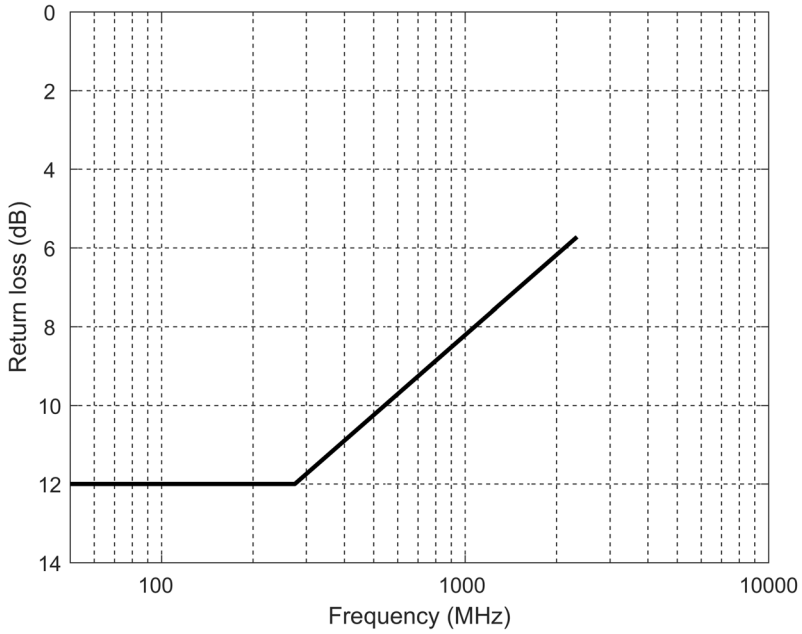


Figure 128A–7—Output differential return loss

128A.3.1.4 Transmitter output waveform

128A.3.1.4.1 Linear fit to the measured waveform

The linear fit pulse response is characterized using the procedure described in 94.3.12.5.2 with the exception that the measurement is performed at $TP4_{H\text{-}D}$ rather than TP2, Np =100, and pattern is PRBS13Q test pattern (see 120.5.10.2.3).

128A.3.1.4.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, *p(k)*, is determined according to 128A.3.1.4.1 The steady-state voltage *vf* is defined to be the sum of the linear fit pulse *p(k)* divided by M, determined in step 3 of the linear fit procedure. The steady-state voltage shall be greater than or equal to 400 mV and less than or equal to 600 mV. The peak value of *p(k)* shall be greater than 0.42× *vf*.

128A.3.1.5 Transmit jitter test requirements

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.3. For the purpose of jitter measurement, the effect of a single-pole high-pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements shall be a square wave as defined in 52.9.1.2 with 5 consecutive 1's and 0's. Crossing times are defined with respect to the mid-point (0 V) of the AC coupled differential signal.

128A.3.1.6 Transmit jitter

The transmitter shall have a maximum total jitter of 0.35 UI peak-to-peak, composed of a maximum deterministic component of 0.12 UI peak-to-peak and a maximum random component of 0.2 UI peak-to-peak.

Duty cycle distortion (DCD) is considered a component of deterministic jitter and shall not exceed 0.035 UI peak-to-peak. The peak-to-peak duty cycle distortion is defined as the absolute value of the difference in the mean pulse width of a 1 pulse or the mean pulse width of a 0 pulse (as measured at the mean of the high- and low-voltage levels in a clocklike repeating bit sequence) and the nominal pulse width. Jitter specifications are specified for BER 10^{-12}. Transmit jitter test requirements are specified in 128A.3.1.5.

128A.3.1.7 Transmitter output noise and distortion

Signal-to-noise-and-distortion ratio (SNDR) measured at the transmitter output using the method described in 92.8.3.7 shall be greater than 5.6 dB using Np=3 . A 2.5GSEI signal must be injected at $TP1_{D\text{-}H}$ to ensure connector crosstalk is accounted for in this measurement.

128A.3.2 2.5GSEI host input characteristics

A 2.5GSEI host input shall meet the specifications defined in Table 128A–2 if measured at the appropriate test point. The test transmitter then transmits any valid PCS output (such as scrambled idle).

Table 128A–2—2.5GSEI host input characteristics

Parameter	Subclause reference	Value	Units
Differential input return loss (min.)	128A.3.2.1	See Equation (128A–2)	dB
Interference tolerance	128A.3.2.1	Table 128A–3	
Jitter tolerance	128A.3.2.1	Table 128A–4	

128A.3.2.1 Input differential return loss

The host input differential return loss shall meet Equation (128A–2) measured at $TP1_{D\text{-}H}$.

128A.3.2.2 Receiver interference tolerance

The following considerations apply to the interference tolerance test. The pattern generator is calibrated at $TP2_{D\text{-}H}$ to produce the values in Table 128A–3. ~~A transmitter is applied to $TP3_{H\text{-}D}$ to inject representative crosstalk that will be present when the host receiver is being tested to ensure the crosstalk is measured when calibrating the broadband noise.~~The channel Noise source is a broadband noise generator capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from f_l in Table 128C–1 to 0.5 times the signaling speed for the port type under test with a crest factor of no less than 5. The noise shall be measured at the out-put of a filter connected to the output of the noise source. The filter for this measurement shall have no more than a 40 dB per decade roll-off and a 3 dB cut-off frequency at least 0.5 times the signaling speed. Figure 128A–9 illustrates the calibration and test configurations that are needed for the host interference tolerance test. The data pattern used for the receiver interference tolerance test shall be PRBS7. The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 3.125 GBd ± 100 ppm.

Calibration procedure is as follows:

1) Create a channel (ISI channel + HCB + DCB) with as close to 2.475 dB of loss at 1.5625 GHz as possible.
2) Measure signal through the ISI channel at $TP2_{D\text{-}H}$.

3) Adjust pattern generator output and ISI channel to meet the required linear fit pulse peak value.
4) Adjust pattern generator amplitude to meet the required steady-state voltage.
5) ~~Ensure signal is being injected at $TP3_{H-D}$ and a~~Adjust noise to meet the required SNDR.
6) Adjust pattern generator random jitter to the required value and then add sinusoidal jitter at 20 MHz to reach the total jitter requirement.

Table 128A–3—2.5GSEI host interference parameters

Parameter	Value	Units
Transmitter steady-state voltage, *vf*	400	mV
Linear fit pulse peak	0.84 × *vf*	mV
Total Jitter	0.35	UI
Random Jitter	0.2	UI
SDNR	25	dB

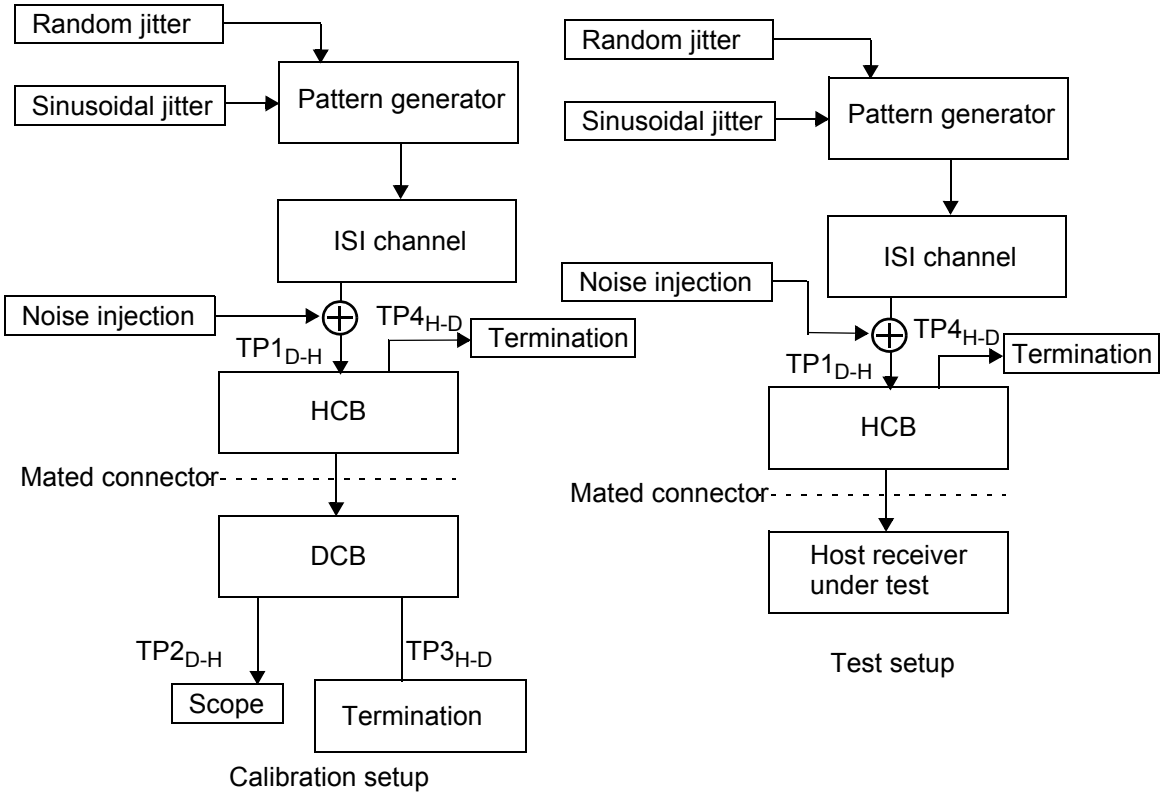


Figure 128A–8—Host interference calibration and test setup

128A.3.2.3 Receiver jitter tolerance

The following considerations apply to the jitter tolerance test. The transmitter is calibrated at $TP2_{D\text{-}H}$ to produce the values in Table 128A–4. Broadband noise is not injected during this test except for what is inherently present in the host. Table 128A–10 illustrates the calibration and test configurations that are needed for the host interference tolerance test. The data pattern used for the receiver jitter tolerance test shall be PRBS7. The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 3.125 GBd ± 100 ppm.

Calibration procedure is as follows:

1) Create a channel (ISI channel + HCB + DCB) with as close to 2.475 dB of loss at 1.5625 GHz as possible.
2) Measure signal through the ISI channel at $TP2_{D\text{-}H.}$
3) Adjust pattern generator output and ISI channel to meet the required linear fit pulse peak value.
4) Adjust pattern generator amplitude to meet the required steady-state voltage.
5) Adjust pattern generator random jitter to the required value.
6) Adjust sinusoidal jitter until the values in Table 128A–5 are met.

Table 128A–4—2.5GSEI host jitter tolerance parameters

Parameter	Value	Units
Transmitter steady-state voltage, *vf*	400	mV
Linear fit pulse peak	0.84 × *vf*	mV
Random Jitter	0.2	UI
Applied peak-to-peak sinusoidal jitter	Table 128A–5	

Table 128A–5—Applied peak-to-peak sinusoidal jitter

Parameter	Case 1	Case 2	Case 3	Units
Jitter frequency	0.02	1.875	20	MHz
Peak-to-peak jitter amplitude	5	0.15	0.15	UI

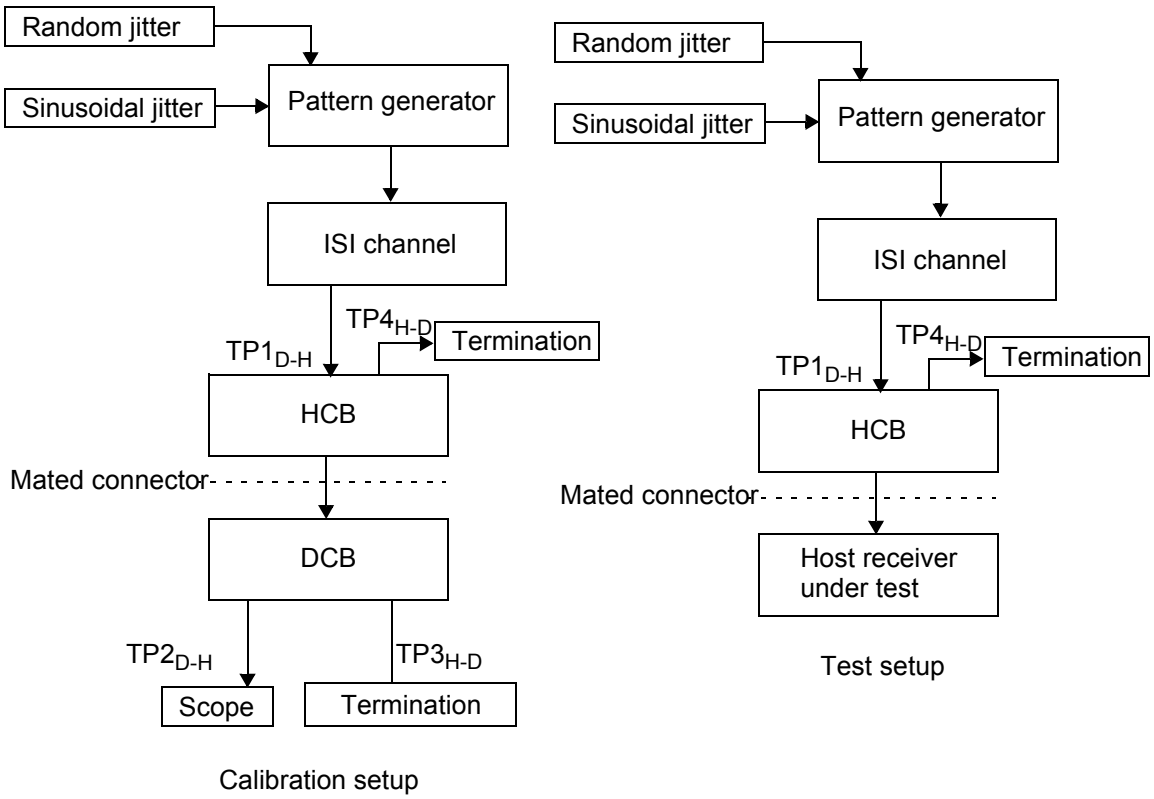


Figure 128A–9—Host ~~interference~~jitter tolerance calibration and test setup

128A.3.3 2.5GSEI drive output characteristics

A 2.5GSEI drive output shall meet the specifications defined in Table 128A–6 if measured at $TP2_{D-H}$.

Table 128A–6—2.5GSEI drive output characteristics

Parameter	Subclause reference	Value	Units
Signaling rate ~~per lane (range)~~	128A.3.1.1	3.125 ± 100 ppm	GBd
DC common-mode output voltage (max.)	128A.3.1.2	1.9	V
AC common-mode output voltage (max, RMS)	128A.3.1.2	30	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	128A.3.1.2	 35 1200	 mV mV
Differential output return loss (min.)	128A.3.1.3	See Equation (128A–2)	dB
Output waveform Transmitter steady-state voltage, vf (max.) Transmitter steady-state voltage, vf (min.) Linear fit pulse peak (min)	 128A.3.3.2 128A.3.3.2 128A.3.3.2	 600 400 0.84	 mV mV mV
Max output jitter (peak-to-peak) Random jitter Deterministic jitter Duty Cycle Distortion Total jitter	128A.3.1.6	 0.2 0.12 0.035 0.35	 UI UI UI UI
Signal-to-noise-and-distortion ratio (min)	128A.3.3.2	25	dB

A test system with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth is to be used for all output signal measurements, unless otherwise specified.

128A.3.3.1 Linear fit to the measured waveform

The linear fit pulse response and normalized transmitter coefficient values are characterized using the procedure described in 94.3.12.5.2 with the exception that the measurement is performed at $TP2_{D\text{-}H}$ rather than TP2, Np =100, and pattern is PRBS13Q test pattern (see 120.5.10.2.3).

128A.3.3.2 Steady-state voltage and linear fit pulse peak

The linear fit pulse, *p(k)*, is determined according to 128A.3.1.4.1. The steady-state voltage *vf* is defined to be the sum of the linear fit pulse *p(k)*) divided by *M*, determined in step 3 of the linear fit procedure. The steady-state voltage shall be greater than or equal to 400 mV and less than or equal to 600 mV. The peak value of *p(k)* shall be greater than 0.84 × *vf*.

128A.3.3.3 Transmitter output noise and distortion

Signal-to-noise-and-distortion ratio (SNDR) measured at the transmitter output using the method described in 92.8.3.7 shall be greater than 25 dB using NP=3 regardless of the transmit equalizer setting. A 2.5GSEI signal must be injected at $TP3_{H\text{-}D}$ to ensure connector crosstalk is accounted for in this measurement.

128A.3.4 2.5GSEI drive input characteristics

A 2.5GSEI drive input shall meet the specifications defined in Table 128A–7 if measured at the appropriate test point.

Table 128A–7—2.5GSEI drive input characteristics

Parameter	Subclause reference	Value	Units
Differential input return loss (min.)	128A.3.4.1	See Equation (128A–2)	dB
Interference tolerance	128A.3.4.2	Table 128A–8	
Jitter tolerance	128A.3.4.3	Table 128A–9	

128A.3.4.1 Input differential return loss

The drive input differential return loss shall meet Equation (128A–2) measured at $TP3_{H\text{-}D}$.

128A.3.4.2 Receiver interference tolerance

The following considerations apply to the interference tolerance test. The pattern generator is calibrated at $TP2_{D\text{-}H}$ to produce the values in Table 128A–8. ~~A transmitter is applied to $TP3_{H\text{-}D}$ to inject representative crosstalk that will be present when the drive receiver is being tested to ensure the crosstalk is measured when calibrating the broadband noise.~~ The channel Noise source is a broadband noise generator capable of producing white Gaussian noise with adjustable amplitude. The power spectral density shall be flat to ±3 dB from f_l in Table 128C–1 to 0.5 times the signaling speed for the port type under test with a crest factor of no less than 5. The noise shall be measured at the out-put of a filter connected to the output of the noise source. The filter for this measurement shall have no more than a 40 dB per decade roll-off and a 3 dB cut-off frequency at least 0.5 times the signaling speed. Figure 128A–10 illustrates the calibration and test configurations that are needed for the drive interference tolerance test. The data pattern used for the receiver interference tolerance test shall be PRBS7 (see 49.2.8). The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 3.125 ± 100 ppm.

Calibration procedure is as follows:

1) Create a channel (ISI channel + HCB + DCB) with as close to 10.525 dB of loss at 1.5625 GHz as possible.
2) Measure signal through the ISI channel at $TP4_{H\text{-}D}$.
3) Adjust pattern generator output and ISI channel to meet the required linear fit pulse peak value.
4) Adjust pattern generator amplitude to meet the required steady-state voltage.
5) ~~Ensure signal is being injected at $TP1_{D\text{-}H}$ and a~~Adjust noise to meet the required SNDR.

6) Adjust pattern generator random jitter to the required value and then add sinusoidal jitter at 20 MHz to reach the total jitter requirement.

Table 128A–8—2.5GSEI drive interference parameters

Parameter	Value	Units
Transmitter steady-state voltage, *vf*	400	mV
Linear fit pulse peak	0.42 × *vf*	mV
Total Jitter	0.35	UI
Random Jitter	0.2	UI
SDNR	5.6	dB

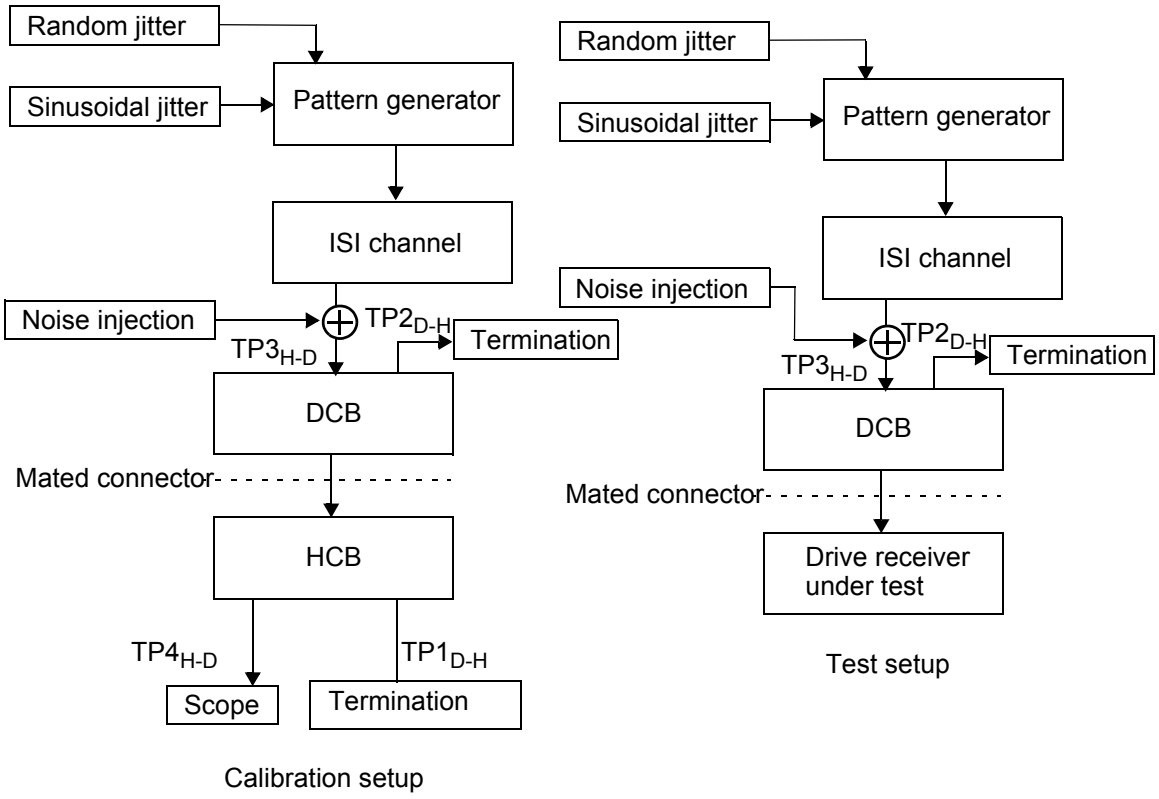


Figure 128A–10—Drive interference calibration and test setup

128A.3.4.3 Receiver jitter tolerance

The following considerations apply to the jitter tolerance test. The transmitter is calibrated at $TP2_{D\text{-}H}$ to produce the values in Table 128A–9. Broadband noise is not injected during this test except for what is inherently present in the drive. Figure 128A–10 illustrates the calibration and test configurations that are needed for the drive interference tolerance test. The data pattern used for the receiver jitter tolerance test shall be

PRBS7 (see 49.2.8). The BER shall be less than or equal to 10^{-12} for any signaling speed in the range of 3.125 GBd ± 100 ppm.

Calibration procedure is as follows:

1) Create a channel (ISI channel + HCB + DCB) with as close to 10.525 dB of loss at1.5625 GHz as possible.
2) Measure signal through the ISI channel at $TP4_{H\text{-}D}$.
3) Adjust pattern generator output and ISI channel to meet the required linear fit pulse peak value.
4) Adjust pattern generator amplitude to meet the required steady-state voltage.
5) Adjust pattern generator random jitter to the required value.
6) Adjust sinusoidal jitter until the values in Table 128A–10 are met.

Table 128A–9—2.5GSEI drive receiver jitter tolerance parameters

Parameter	Value	Units
Transmitter steady-state voltage, *vf*	400	mV
Linear fit pulse peak	0.42 × *vf*	mV
Random Jitter	0.2	UI
Applied peak-to-peak sinusoidal jitter	Table 128A–10	

Table 128A–10—Applied peak-to-peak sinusoidal jitter

Parameter	Case 1	Case 2	Case 3	Units
Jitter frequency	0.02	1.875	20	MHz
Peak-to-peak jitter amplitude	5	0.15	0.15	UI

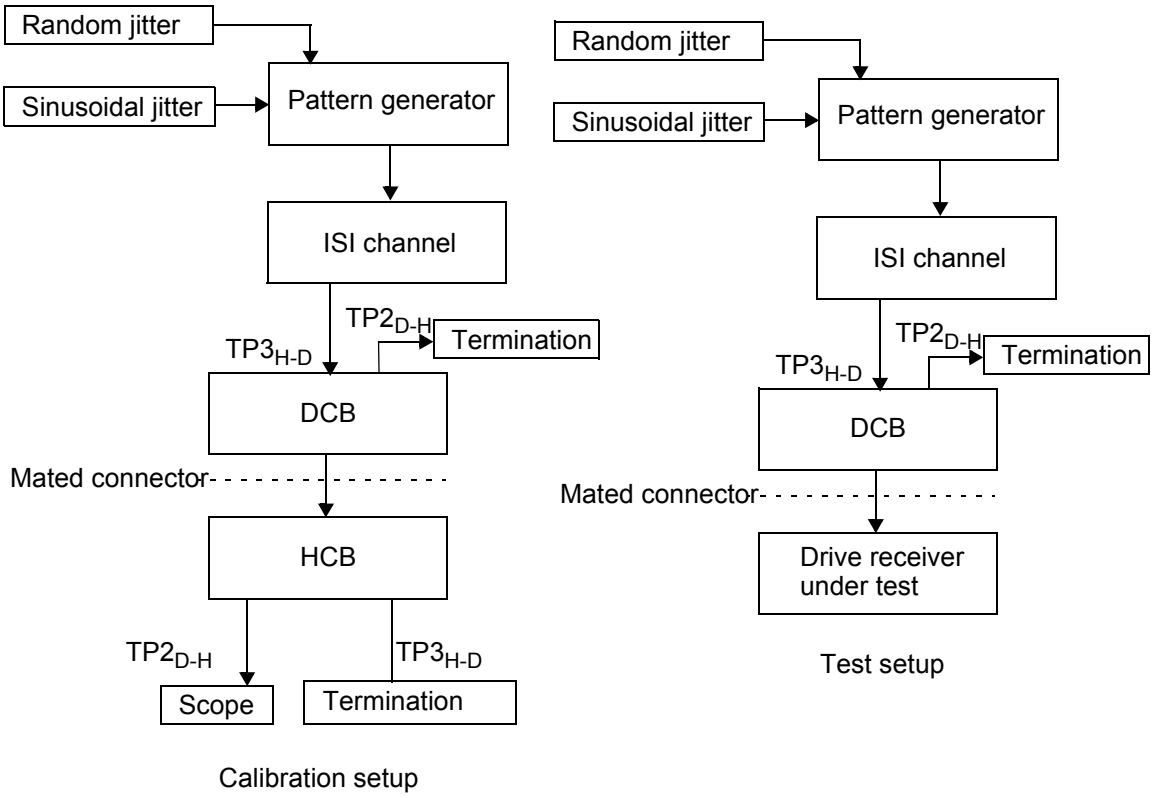


Figure 128A–11—Drive receiver jitter tolerance test setup

128A.4 Protocol implementation conformance statement (PICS) proforma for Annex 128A, 2.5Gb/s Storage Enclosure Interface (2.5GSEI)[1]

128A.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 128A, 2.5Gb/s Storage Enclosure Interface (2.5GSEI), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

128A.4.2 Identification

128A.4.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

128A.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cb-2016, Annex 128A, Annex title
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cb-2016.)	

Date of Statement	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

128A.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
2.5GSEI	2.5GSEI Host Enclosure Interface	128A		O	Yes [ ] No [ ]

128A.4.4 PICS proforma tables for 2.5Gb/s Storage Enclosure Interface (2.5GSEI)

Item	Feature	Subclause	Value/Comment	Status	Support
OV1	Bit Error Rate	128A.1.1	BER < 10E-12	M	Yes [ ]

128A.4.4.1 Host output functions

Item	Feature	Subclause	Value/Comment	Status	Support
HO1	2.5GSEI host output characteristics	128A.3.1	Table 128A–1, measured at $TP4_{H\text{-}D}$	M	Yes [ ]
HO2	Tx steady-state output	128A.3.1.4.2	≥ 400 mV, ≤ 600 mV	M	Yes [ ]
HO3	Tx peak output	128A.3.1.4.2	p(k) > 0.42 x v_f	M	Yes [ ]
HO4	Tx jitter test waveform	128A.3.1.5	Square wave defined in 52.9.1.2	M	Yes [ ]
HO5	Transmit jitter requirements	128A.3.1.6	Tj ≤ 0.35 UI pk-pk, with Dj ≤ 0.12 UI pk-pk and Rj ≤ 0.2 UI pk-pk	M	Yes [ ]
HO6	Tx DCD limit	128A.3.1.6	< 0.035 UI pk-pk	M	Yes [ ]
HO7	Tx SNDR limit	128A.3.1.7	> 5.6 dB using Np=3	M	Yes [ ]

128A.4.4.2 Host input functions

Item	Feature	Subclause	Value/Comment	Status	Support
HI1	2.5GSEI host input characteristics	128A.3.2	Table 128A–2, measured at $TP1_{D\text{-}H}$	M	Yes [ ]
HI2	Input differential return loss	128A.3.2.2	Shall meet Equation (128A–2) at $TP1_{D\text{-}H}$	M	Yes [ ]
HI3	Receiver interference tolerance test pattern	128A.3.2.2	PRBS7	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
HI4	Receiver interference tolerance BER	128A.3.2.2	BER ≤ 10E-12 for any signaling in range of 3.125 Gbps ± 100 ppm	M	Yes [ ]
HI5	Receiver jitter tolerance test pattern	128A.3.2.3	PRBS7	M	Yes [ ]
HI6	Receiver jitter tolerance BER	128A.3.2.3	BER ≤ 10E-12 for any signaling in range of 3.125 Gbps ± 100 ppm	M	Yes [ ]

128A.4.4.3 Drive output functions

Item	Feature	Subclause	Value/Comment	Status	Support
DO1	2.5GSEI host output characteristics	128A.3.3	Table 128A–6, measured at $TP2_{D\text{-}H}$	M	Yes [ ]
DO2	Tx Steady-State output	128A.3.3.2	≥ 400 mV, ≤ 600 mV	M	Yes [ ]
DO3	Tx peak output	128A.3.3.2	$p(k) > 0.84 \times v_f$	M	Yes [ ]
DO4	Tx SNDR limit	128A.3.3.3	> 25 dB using Np=3	M	Yes [ ]

128A.4.4.4 Drive input functions

Item	Feature	Subclause	Value/Comment	Status	Support
DI1	2.5GSEI drive input parameters	128A.3.4	Table 128A–7, measured at $TP3_{H\text{-}D}$	M	Yes [ ]
DI2	Input differential return loss	128A.3.4.2	Shall meet Equation (128A–2) at $TP3_{H\text{-}D}$	M	Yes [ ]
DI3	Receiver interference tolerance test pattern	128A.3.4.2	PRBS7	M	Yes [ ]
DI4	Receiver interference tolerance BER	128A.3.4.2	BER ≤ 10E-12 for any signaling in range of 3.125 Gbps ± 100 ppm	M	Yes [ ]
DI5	Receiver jitter tolerance test pattern	128A.3.4.3	PRBS7	M	Yes [ ]
DI6	Receiver jitter tolerance BER	128A.3.4.3	BER ≤ 10E-12 for any signaling in range of 3.125 Gbps ± 100 ppm	M	Yes [ ]