Response to comments #161, #164, #166

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Comment #161

Table 136–13—Interference tolerance test parameters

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Test pattern	Scrambled idle encoded by RS-FEC				
Total symbol error ratio required[a]	$< 10^{-3}$				
Test channel insertion loss at 13.28 GHz[b]	14.3	14.8	23.21	23.74	dB
Cable assembly insertion loss at 13.28 GHz	8	10	14.06	16.06	dB
COM		3		3	dB
$b_{max}(1)$ used in COM calculation	0.7				
DER_0 used in COM calculation	10^{-4}				

[a]See 136.9.4.2.5 for definition of total symbol error ratio.
[b]Insertion loss between the two test references (see Figure 110–3b).

136.9.4.3.2 (Jitter tolerance) Test procedure

Jitter may be applied either to one lane at a time or to all lanes in parallel. If jitter is applied to one lane at a time, multiple measurements have to be summed to yield the total symbol error ratio.

A PHY shall meet the total symbol error ratio requirement defined in Table 136–13 for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 120D–6.

136.9.4.2.5 (Interference tolerance) Test procedure

Symbol error ratio is measured using the per-lane RS-FEC symbol error counters (see 91.6) in the adjacent RS-FEC sublayer, or the per-lane PCS symbol error counters (see 119.3.1) in the adjacent PCS, as appropriate. The per-lane counters are summed together.

The total symbol error ratio is defined as the sum of symbol error ratios measured while adding broadband noise to each lane on the pattern generator (see 136.9.4.2.4). If noise is applied to one lane at a time, multiple measurements have to be summed to yield the total symbol error ratio.

A PHY shall meet the total symbol error ratio requirement in all tests defined in Table 136–13.

(Use “FEC” instead of “total” where highlighted)

Proposed response:

Total symbol error ratio is used in Table 136-13, and subclauses 136.9.4.2.5, 136.9.4.3.2.
Rename the parameter "Total symbol error ratio" to "FEC symbol error ratio".

Sum or average?

- Assume all lanes of the DUT are similar and have a small margin
- Denote the result (errors on all lanes divided by symbols on all lanes) with noise on a single lane by SER_1, the result with noise on all lanes by SER_n, and the result with no noise on any lane by SER_0
- Case 1: test setup has very high COM and requires significant additive noise
  - Unstressed lanes have zero errors and not contribute to SER
  - The sum of FEC SER measurements will be $n \cdot SER_1 = SER_n$
  - Average would be incorrect
- Case 2: test setup has COM close to the target and requires negligible additive noise
  - Unstressed lanes have the same SER as the "stressed" lane so SER_1=SER_n
  - The sum of FEC SER measurements will be incorrect: $n \cdot SER_1 \neq SER_n$
  - Using average would yield the correct result in this case
  - This can be corrected by measuring the FEC SER without stress on any lane (denoted SER_0) and deducting (n-1)*SER_0 from the sum:

$$n \cdot SER_1 - (n-1) \cdot SER_0 = SER_n$$

- Assuming case 1 is more realistic, it is suggested use sum in the definition
  - We can leave the decision on whether to correct or not to the test engineer

Comments #164 and #166

Proposed response: Change FROM

136.9.4.2.5 (Interference tolerance) Test procedure

Symbol error ratio is measured using the per-lane RS-FEC symbol error counters (see 91.6) in the adjacent RS-FEC sublayer, or the per-lane PCS symbol error counters (see 119.3.1) in the adjacent PCS, as appropriate. ~~The per-lane counters are summed together.~~

The ~~total~~ symbol error ratio is defined as the sum of symbol error ratios measured while adding broadband noise to each lane on the pattern generator (see 136.9.4.2.4). If noise is applied to one lane at a time, multiple measurements have to be summed to yield the ~~total~~ symbol error ratio.

A PHY shall meet the ~~total~~ symbol error ratio requirement in all tests defined in Table 136–13.

TO

136.9.4.2.5 (Interference tolerance) Test procedure

Symbol error ratio is measured using the per-lane RS-FEC symbol error counters (see 91.6) in the adjacent RS-FEC sublayer, or the per-lane PCS symbol error counters (see 119.3.1) in the adjacent PCS, as appropriate.

The FEC symbol error ratio is defined as the sum of the symbol error counters on all lanes divided by the number of symbols transmitted on all lanes, which may be estimated from the test time.

A PHY shall meet the FEC symbol error ratio requirement in all tests defined in Table 136–13 with broadband noise added to all lanes (see 136.9.4.2.4).

NOTE--If noise is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio.
The result may need to be corrected based on the FEC symbol error ratio with no noise added on any lane.

Comments #164 and #166 (cont.)

Change FROM

136.9.4.3.2 (Jitter tolerance) Test procedure
Jitter may be applied either to one lane at a time or to all lanes in parallel. If jitter is applied to one lane at a time, multiple measurements have to be summed to yield the total symbol error ratio.

A PHY shall meet the total symbol error ratio requirement defined in Table 136–13 for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 120D–6.

TO

136.9.4.3.2 (Jitter tolerance) Test procedure

A PHY shall meet the FEC symbol error ratio requirement defined in Table 136–13 for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 120D–6 with jitter added to all lanes (see 136.9.4.2.4).

NOTE-- If jitter is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio. The result may need to be corrected based on the FEC symbol error ratio with no jitter applied on any lane.