100GbE alignment markers

Pete Anslow, Ciena

IEEE P802.3cd Task Force, San Diego, July 2016

Introduction

nicholl_3cd_01_0716 proposes a similar alignment marker mapping to FEC lanes as is used in Clause 91.

If the scheme is adopted as for Clause 91, this gives:

FEC lane 0	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM4	BIP	$\overline{\text{AM4}}$	$\overline{\text{BIP}}$	AM8	BIP	$\overline{\text{AM8}}$	$\overline{\text{BIP}}$	AM12	BIP	$\overline{\text{AM12}}$	$\overline{\text{BIP}}$	AM16	BIP	$\overline{\text{AM16}}$	$\overline{\text{BIP}}$	Pad	Data
FEC lane 1	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM5	BIP	$\overline{\text{AM5}}$	$\overline{\text{BIP}}$	AM9	BIP	$\overline{\text{AM9}}$	$\overline{\text{BIP}}$	AM13	BIP	$\overline{\text{AM13}}$	$\overline{\text{BIP}}$	AM16	BIP	$\overline{\text{AM16}}$	$\overline{\text{BIP}}$	Data	
FEC lane 2	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM6	BIP	$\overline{\text{AM6}}$	$\overline{\text{BIP}}$	AM10	BIP	$\overline{\text{AM10}}$	$\overline{\text{BIP}}$	AM14	BIP	$\overline{\text{AM14}}$	$\overline{\text{BIP}}$	AM16	BIP	$\overline{\text{AM16}}$	$\overline{\text{BIP}}$	Data	
FEC lane 3	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM7	BIP	$\overline{\text{AM7}}$	$\overline{\text{BIP}}$	AM11	BIP	$\overline{\text{AM11}}$	$\overline{\text{BIP}}$	AM15	BIP	$\overline{\text{AM15}}$	$\overline{\text{BIP}}$	AM16	BIP	$\overline{\text{AM16}}$	$\overline{\text{BIP}}$	Data	

This contribution analyses the performance of this set of alignment markers for 100 Gb/s Ethernet.

Baseline wander

Previous NRZ contributions have used a “baseline wander” parameter

This was defined as:

Baseline wander is the instantaneous offset (in %) in the signal generated by AC coupling at the Baud rate / 10,000.

This analysis re-uses this definition unmodified, but it should be noted that for PAM4, the eye height is 1/3 that of NRZ so the effects of a given amount of baseline wander will be greater.

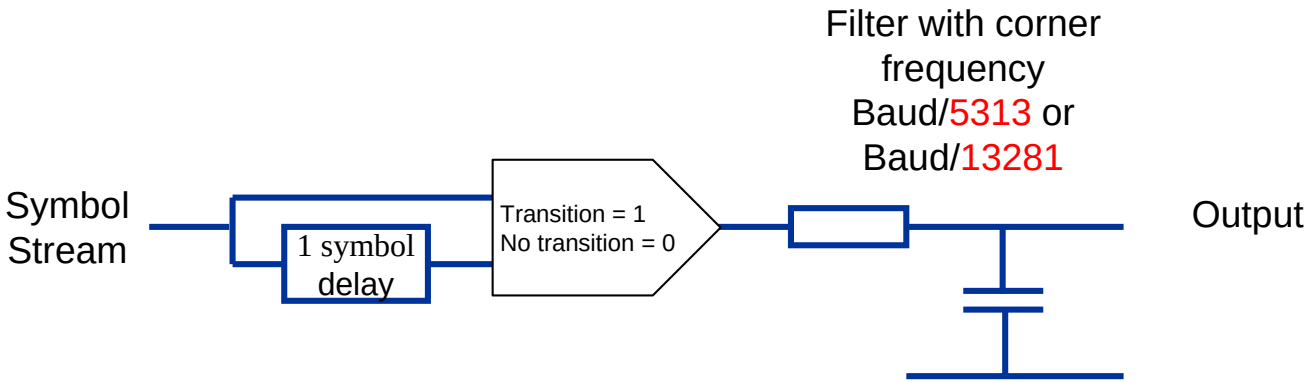
Clock content

The “clock content” parameter is defined here as:

Create a function which is a 1 for a transition and a 0 for no transition and then filter the resulting sequence with a corner frequency of Baud/5313 or Baud/13281.

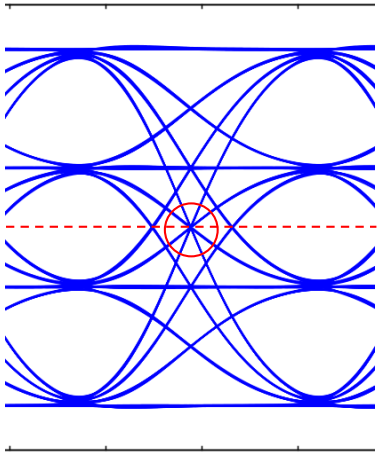
This analysis defines a transition as one of three possibilities (as per healey_3bs_01_1115):

- Symmetrical transitions through the signal average
- Transitions through the signal average
- All transitions

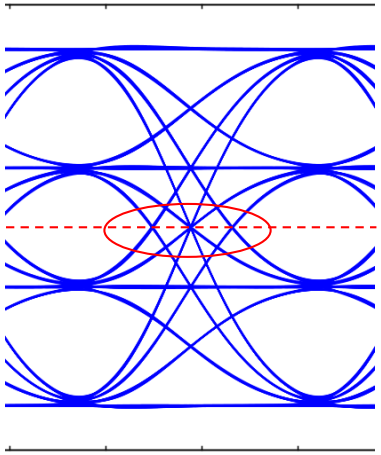


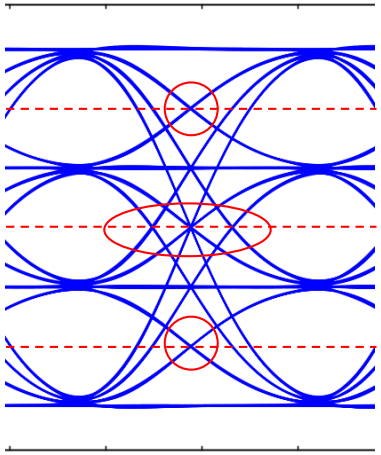
Clock content illustration

Symmetrical transitions through the signal average



Transitions through the signal average





All transitions

Simulations

Using these alignment codes, all possible combinations of FEC lanes for 4:1 bit interleaving for a 100 Gb/s lane were then analysed to find the worst cases for Baseline Wander (BW) and Clock Content (CC) after Gray coding to PAM4 symbols. These searches included lane delays of -40 to +40 UI.

The worst case FEC lane combinations and delays were then used to generate the worst case PDFs for 100 GbE scrambled idle over a single 100 Gb/s lane.

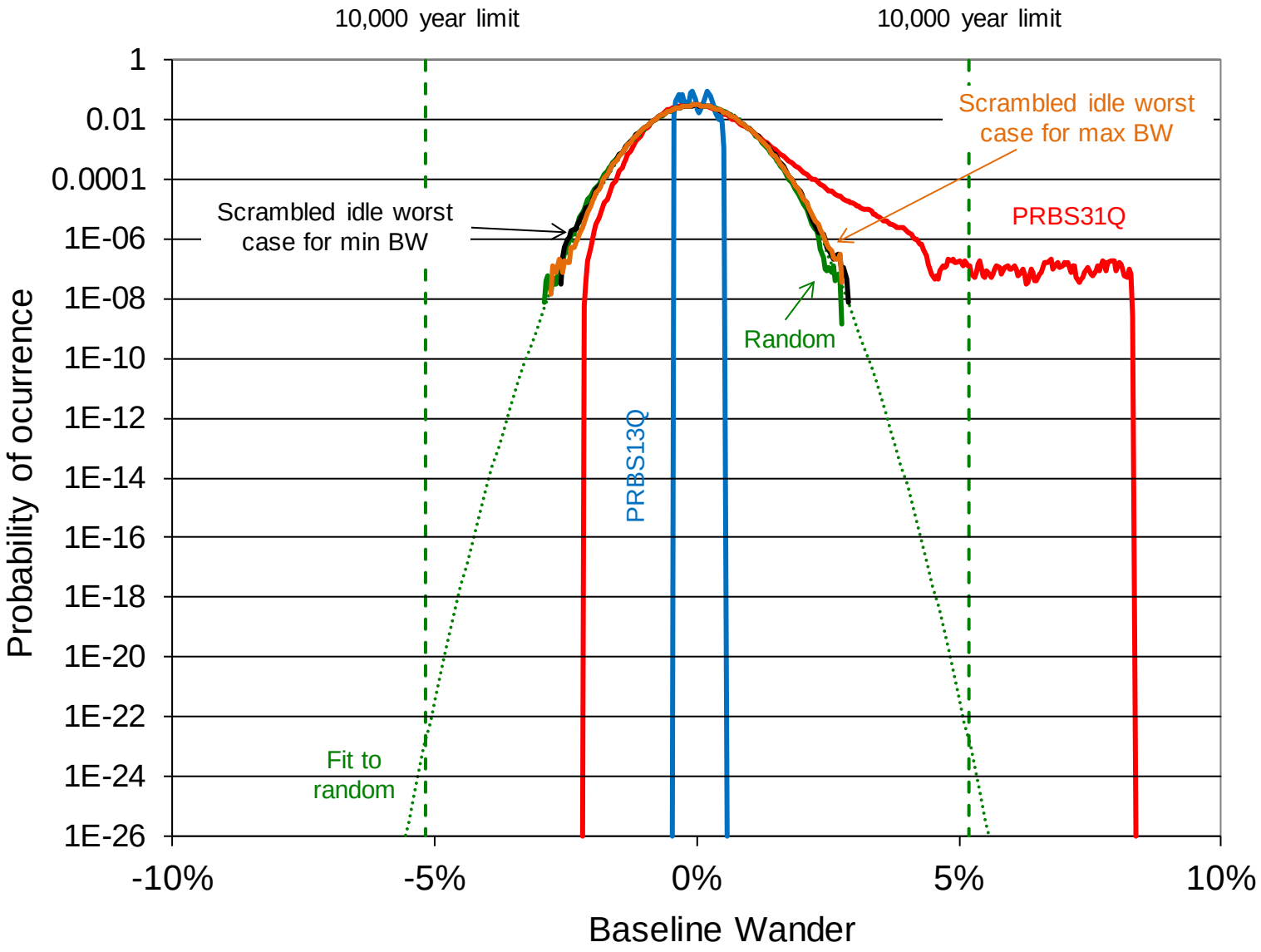
Scrambled idle construction

The scrambled idle symbol streams generated for this analysis were:

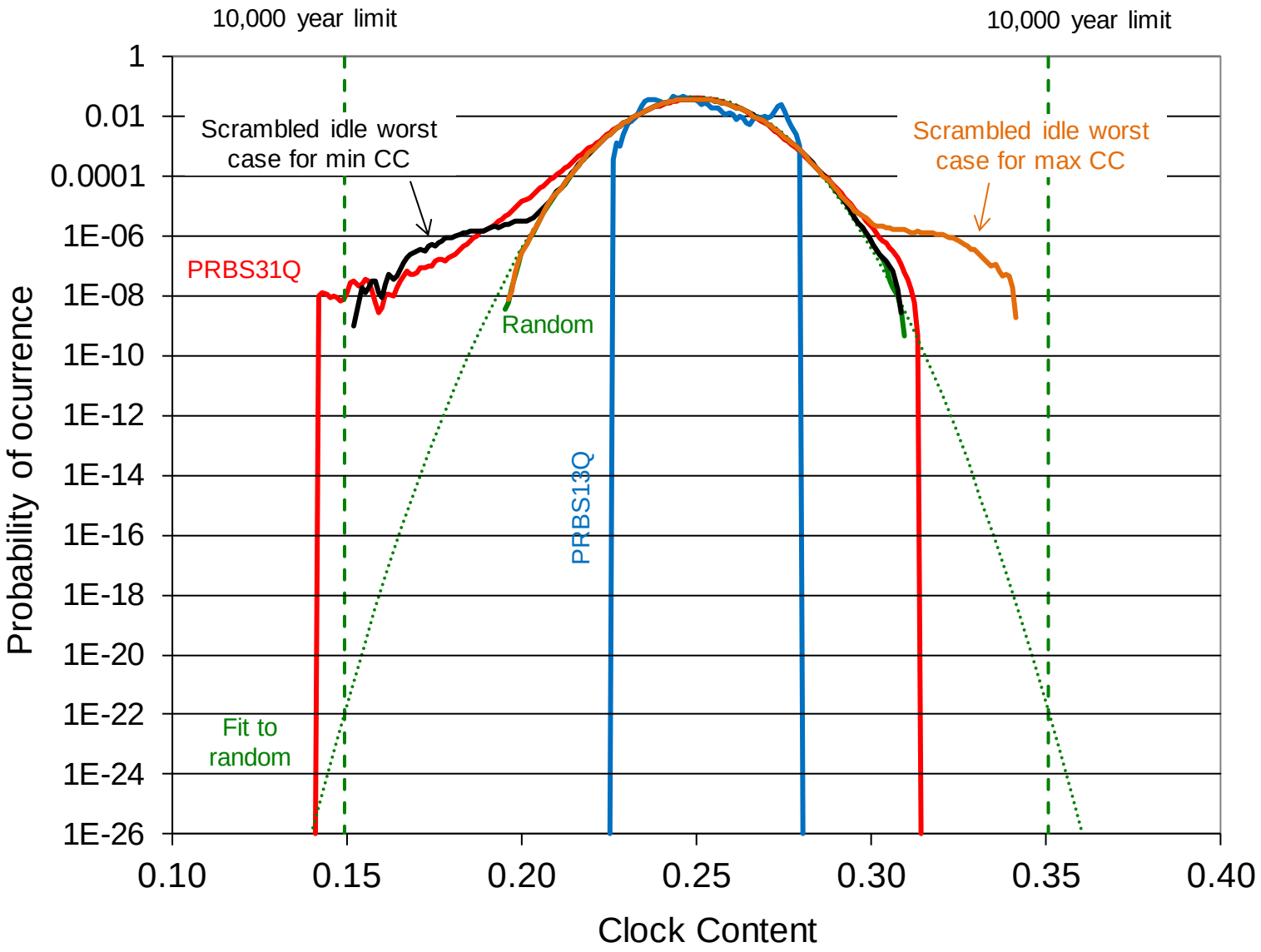
- Idle control characters
- Scrambled
- 256B/257B transcoded
- Used to fill FEC codewords which start with alignment markers followed by the 5 bit pad once in every 4096 codewords
- BIP bits taken as random
- 300 bits of RS(544,514) FEC parity added
- Interleaved 10 bits at a time to form FEC lanes
- Bit interleaved with worst case FEC lane combinations and delays

The results for baseline wander and clock content are in the following slides.

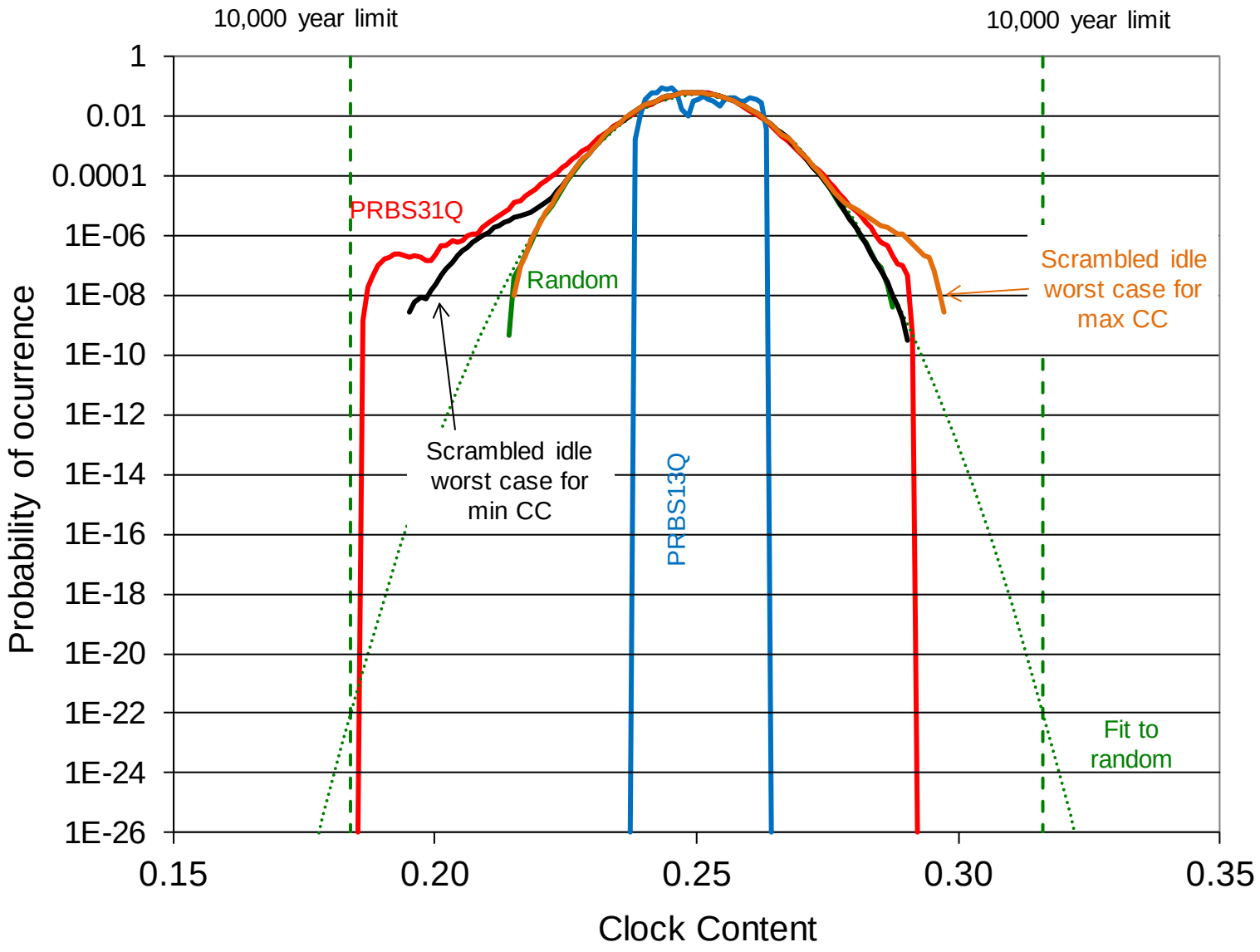
Baseline wander



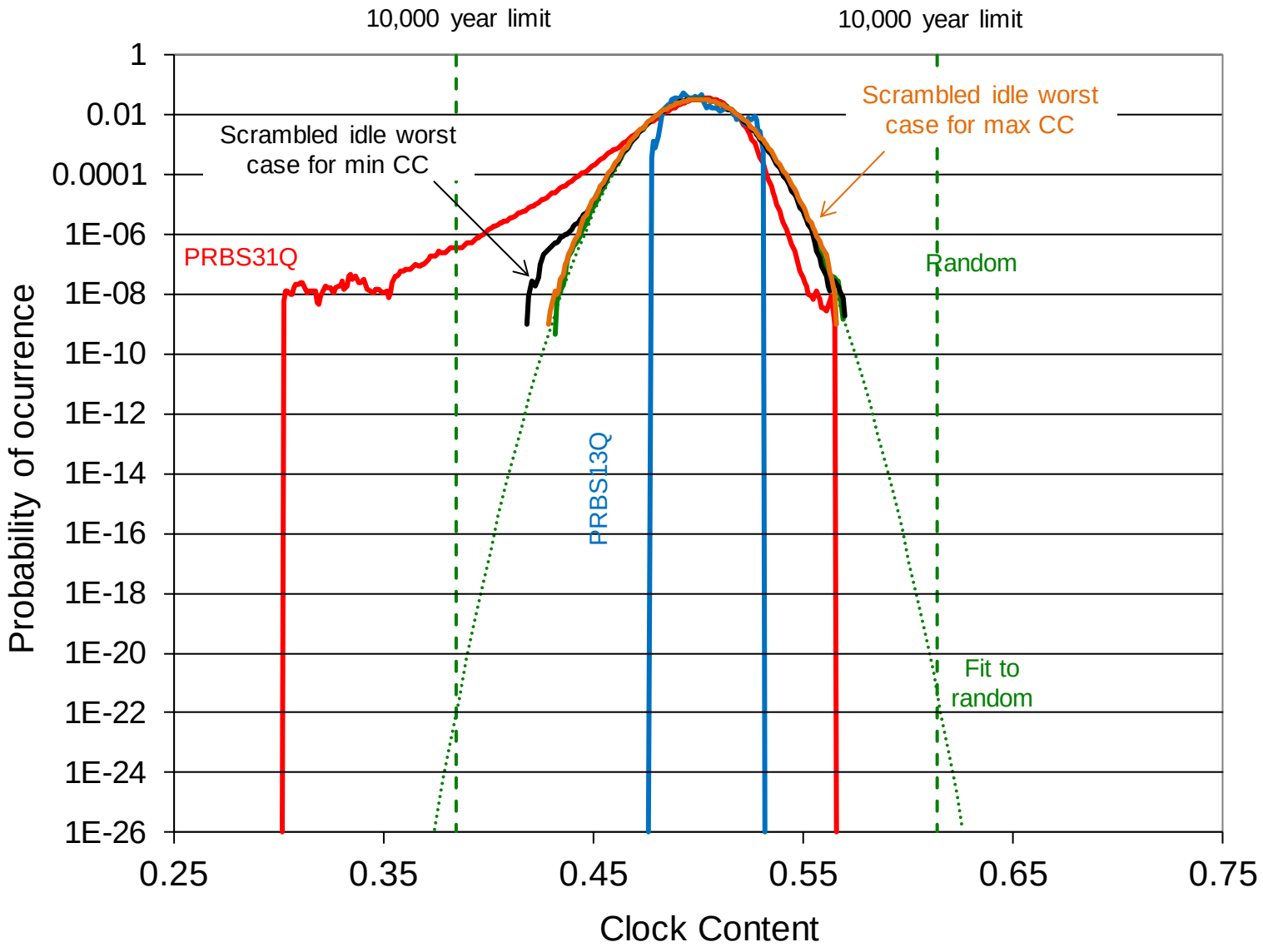
Clock, sym trans through ave, Bd/5313



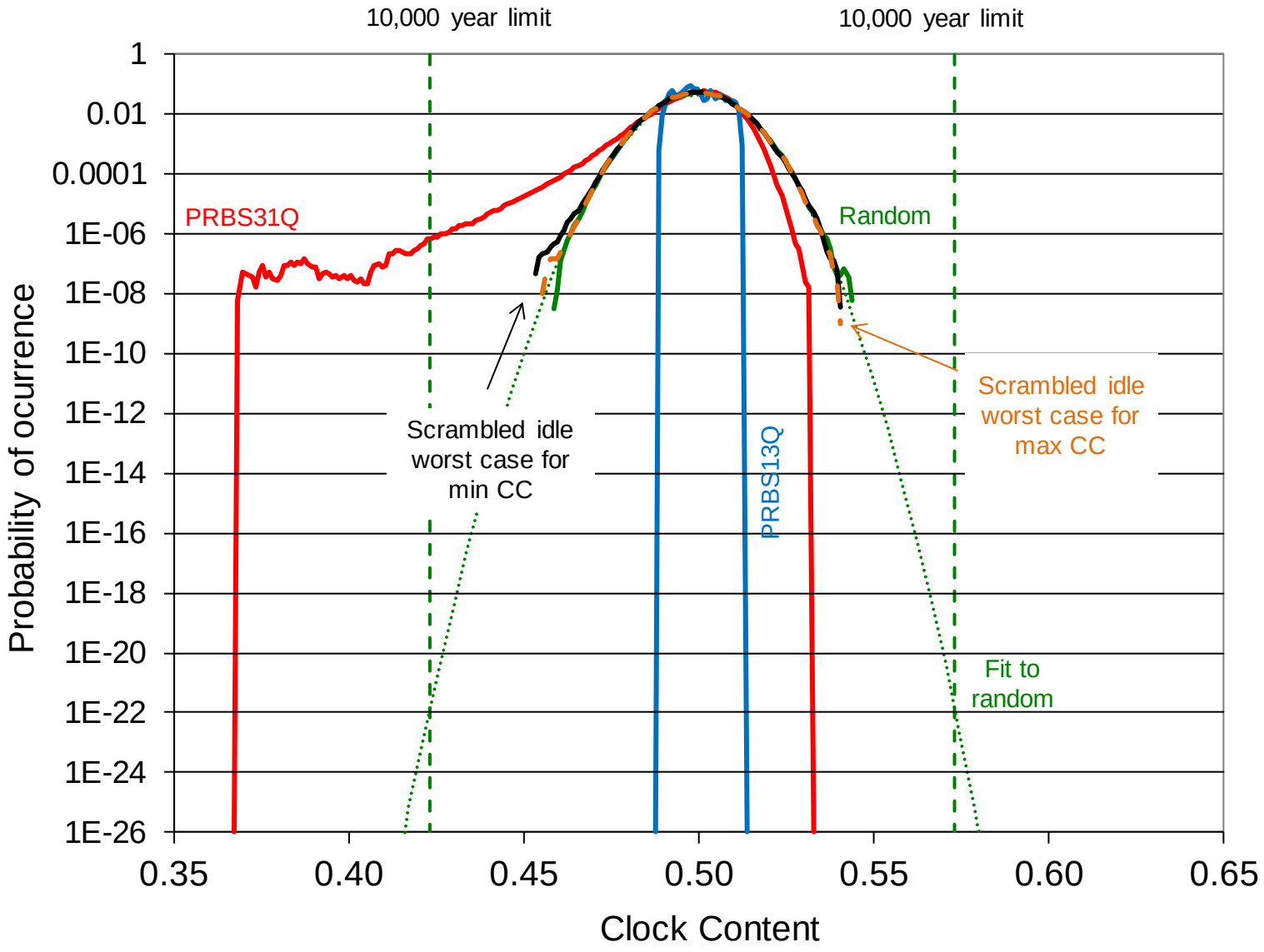
Clock, sym trans through ave, Bd/13281



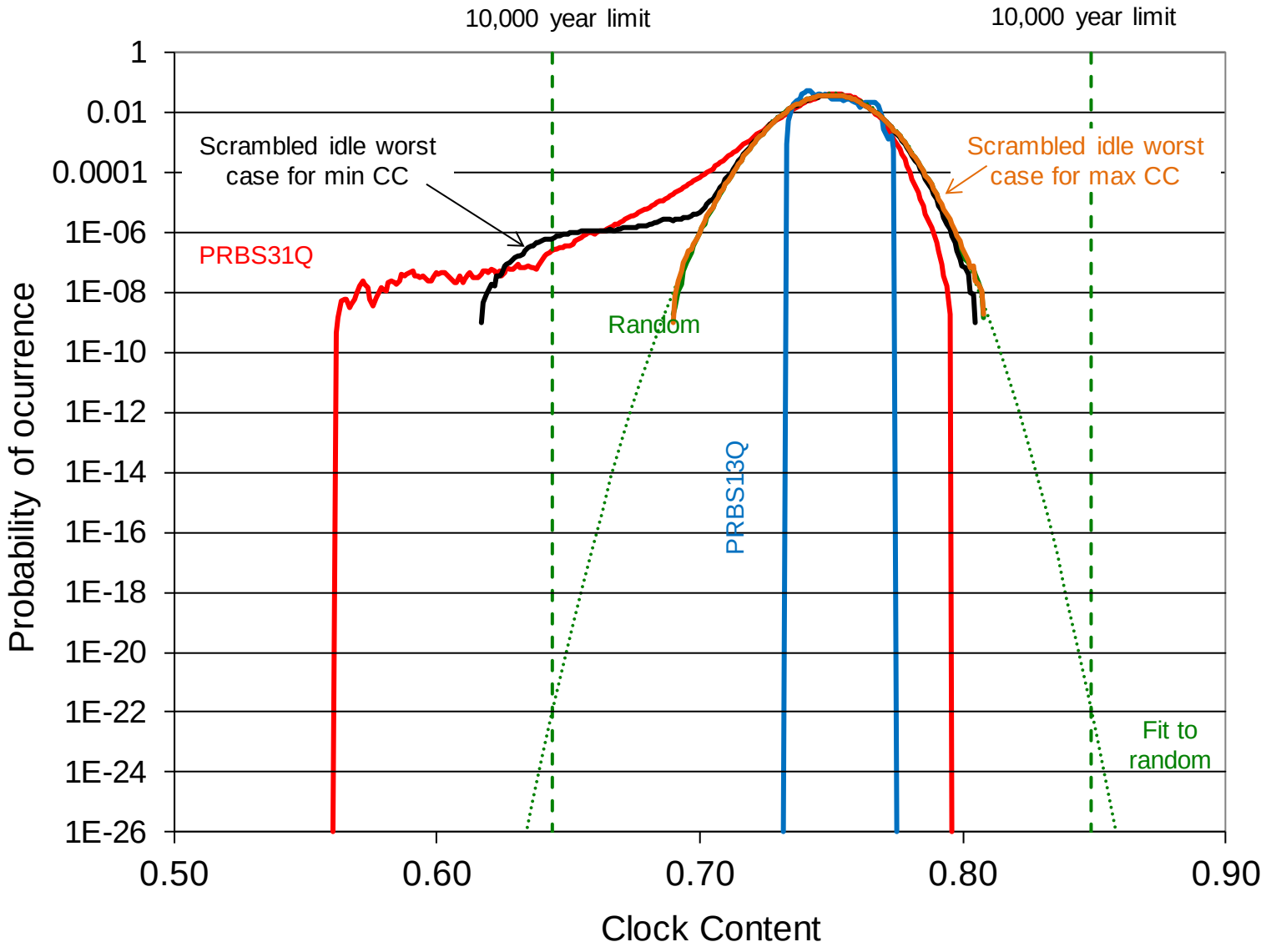
Clock, trans through ave, Bd/5313



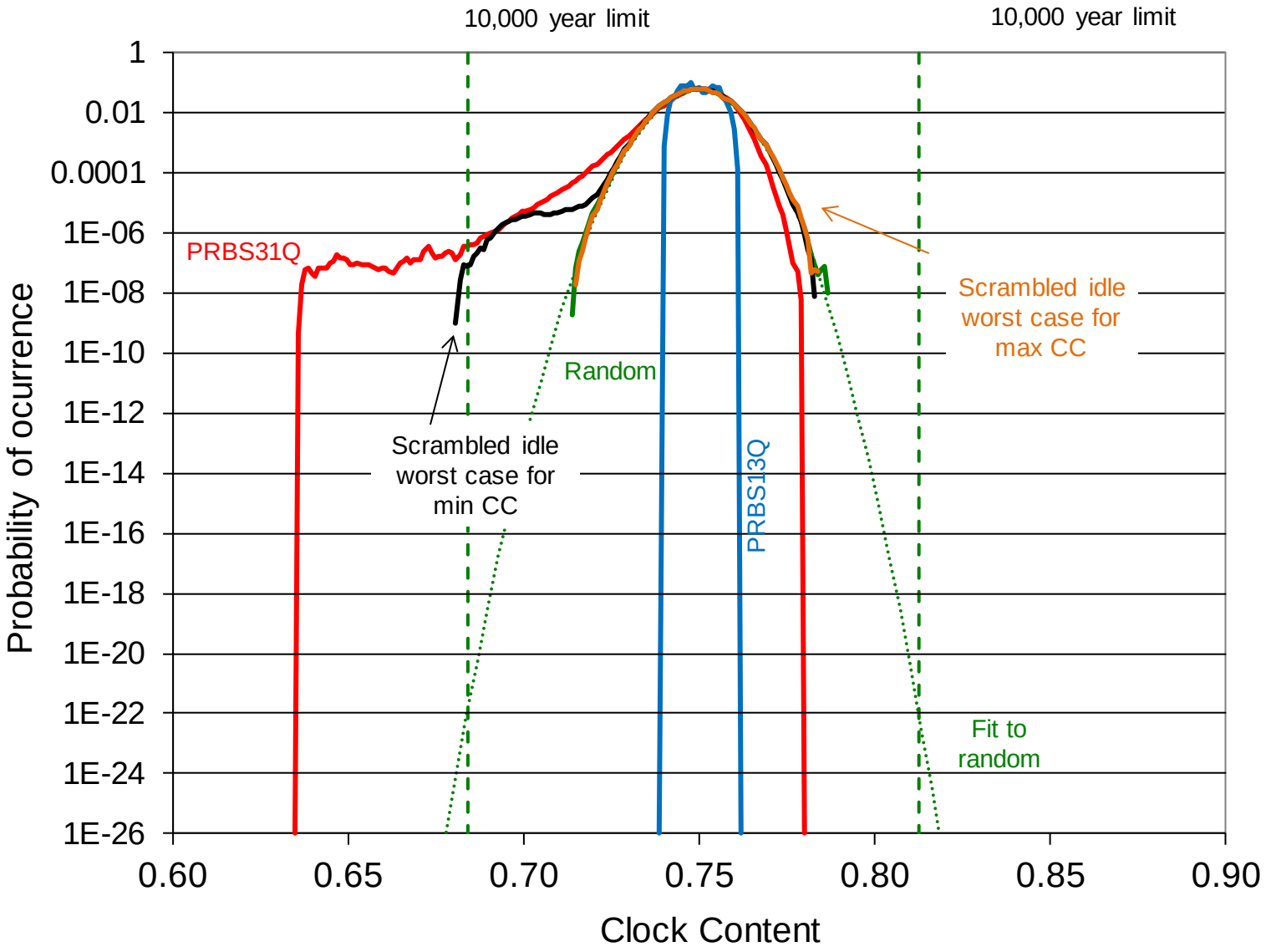
Clock, trans through ave, Bd/13281



Clock, all transitions, Bd/5313



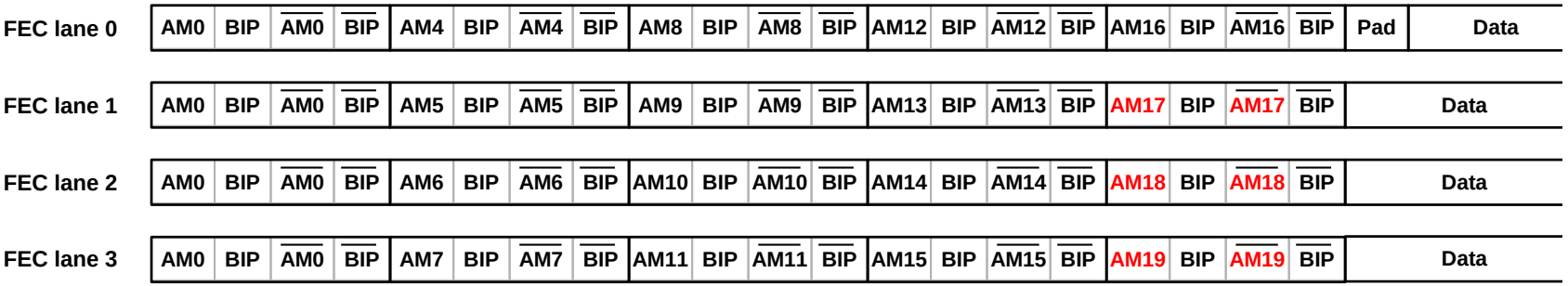
Clock, all transitions, Bd/13281



Clause 91 results

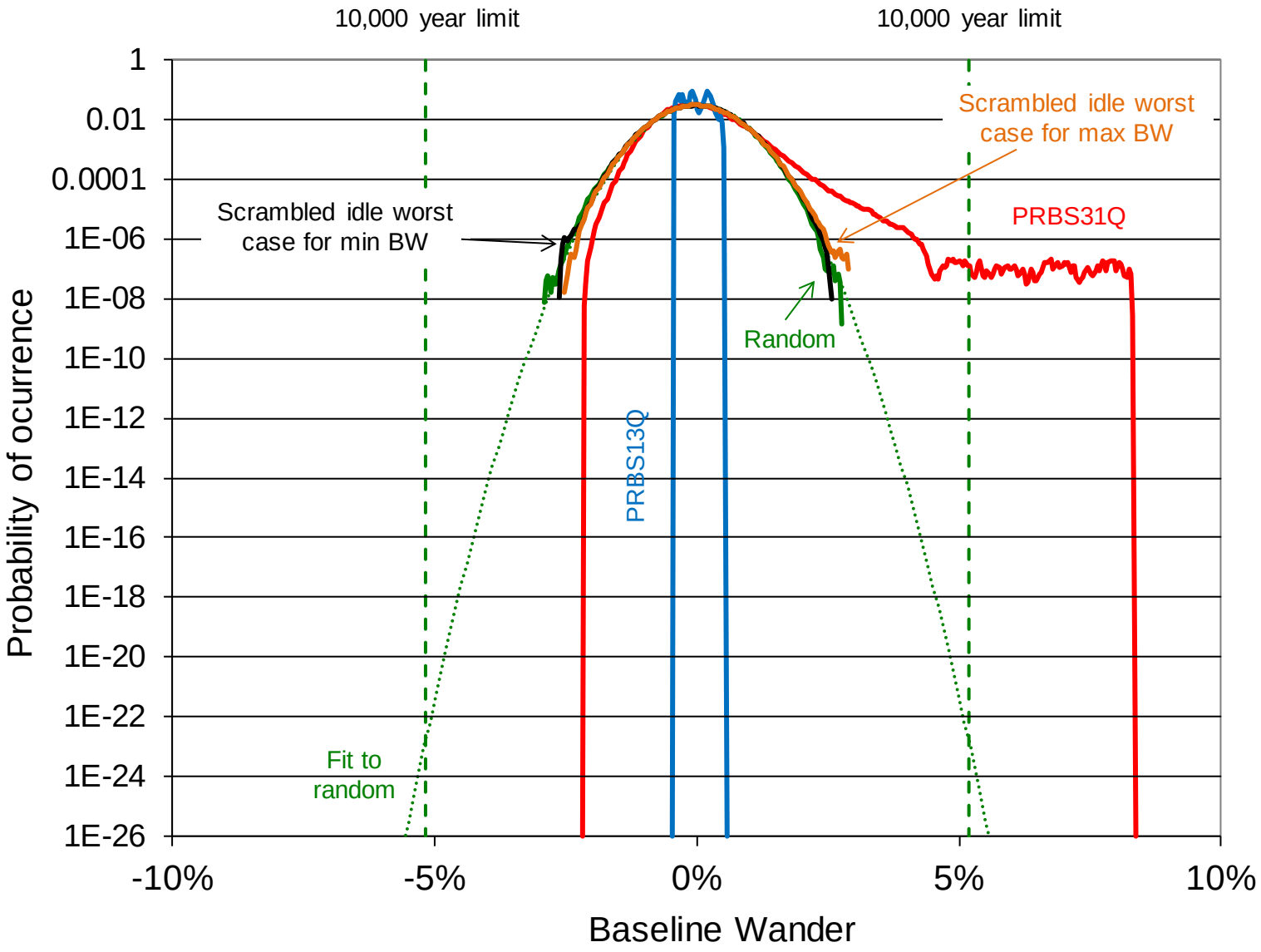
As expected from the previous analysis done for 400 Gb/s Ethernet (see anslow_01_1215_logic), the common AM0 and AM16 markers cause a significant “shoulder” on the clock content plots for 4:1 bit interleaving for a 100 Gb/s lane which cause the plots to go outside those for PRBS31Q.

Removing the second common AM would result in:

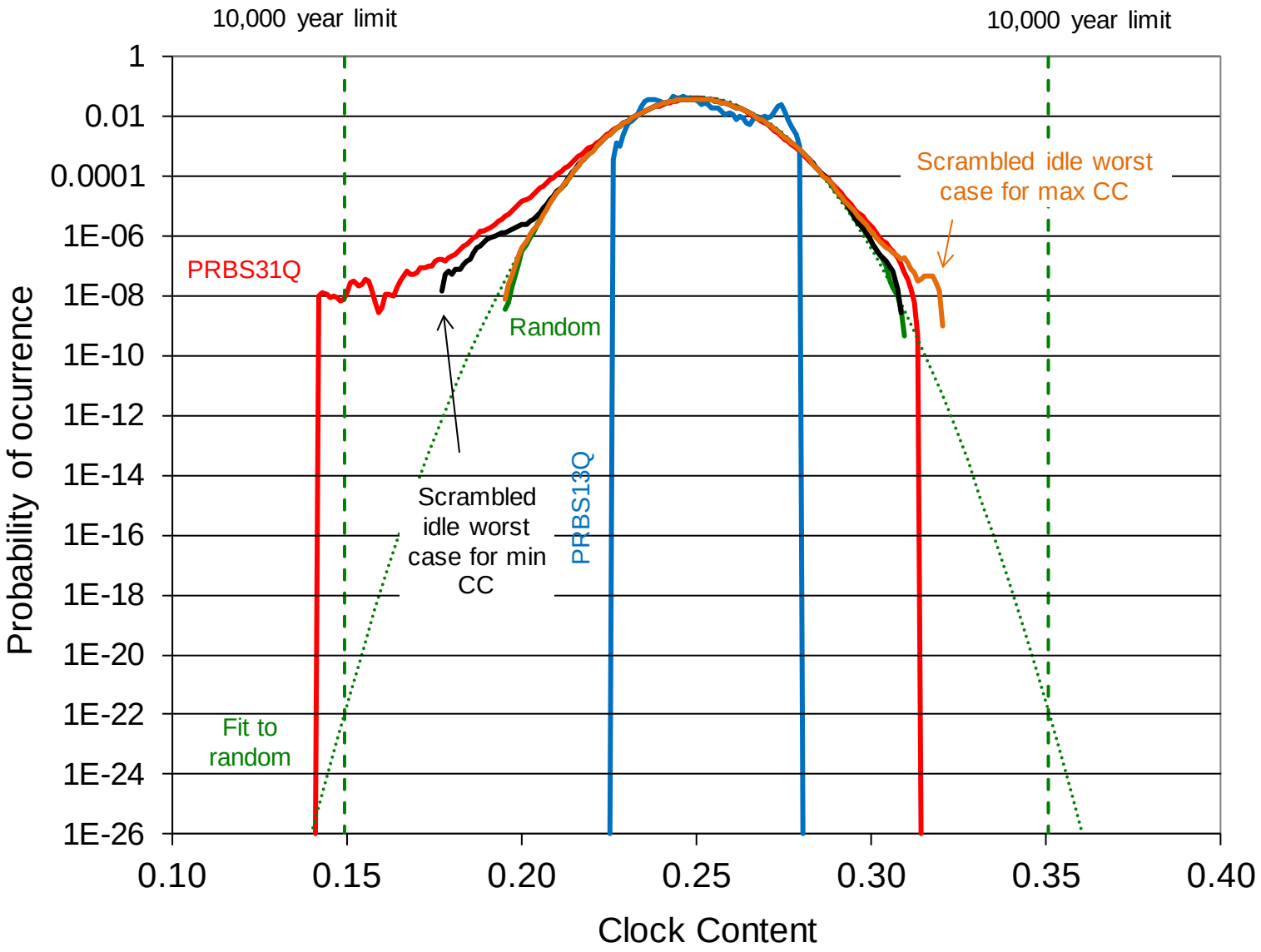


The performance of this revised scheme is shown on the following slides.

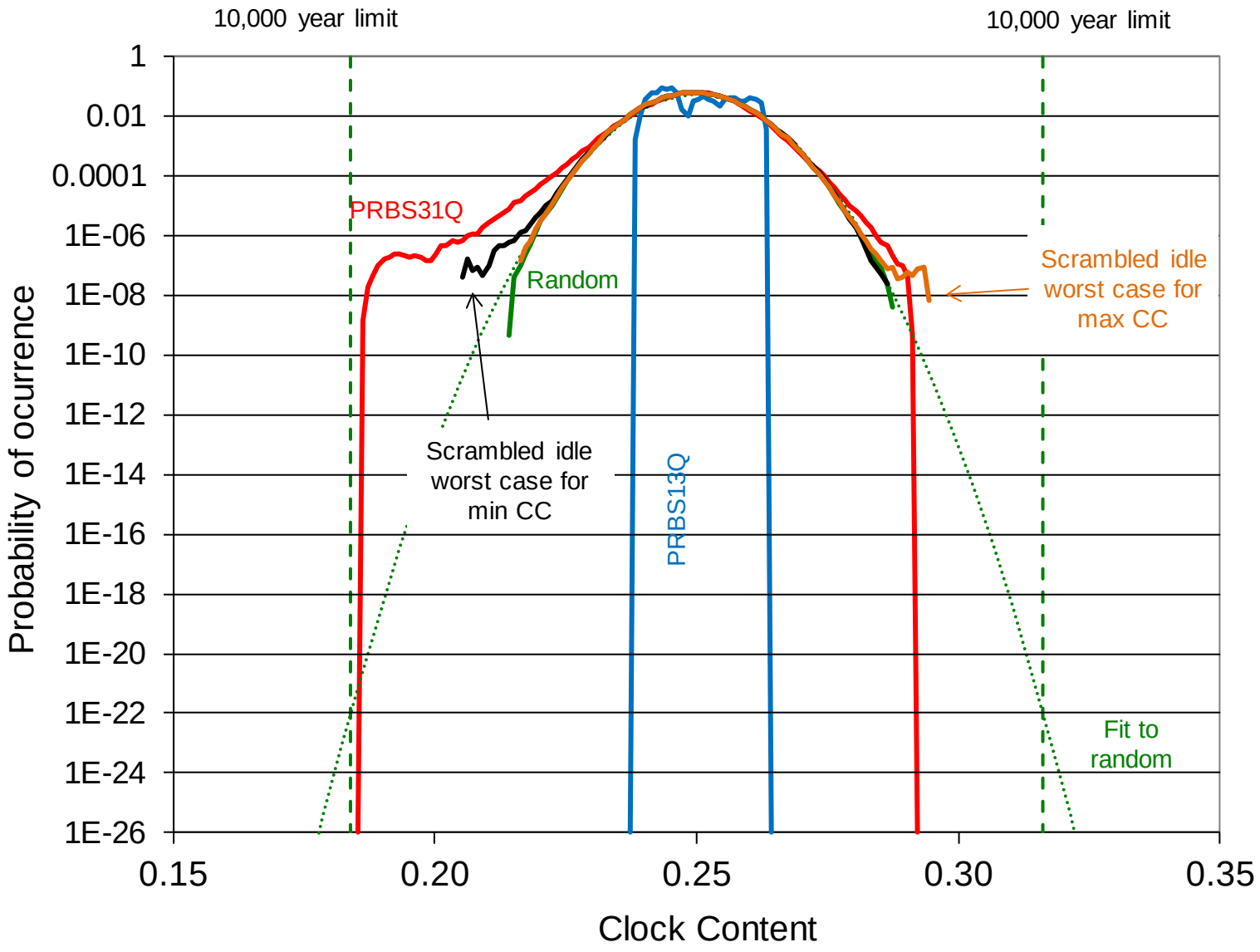
Baseline wander



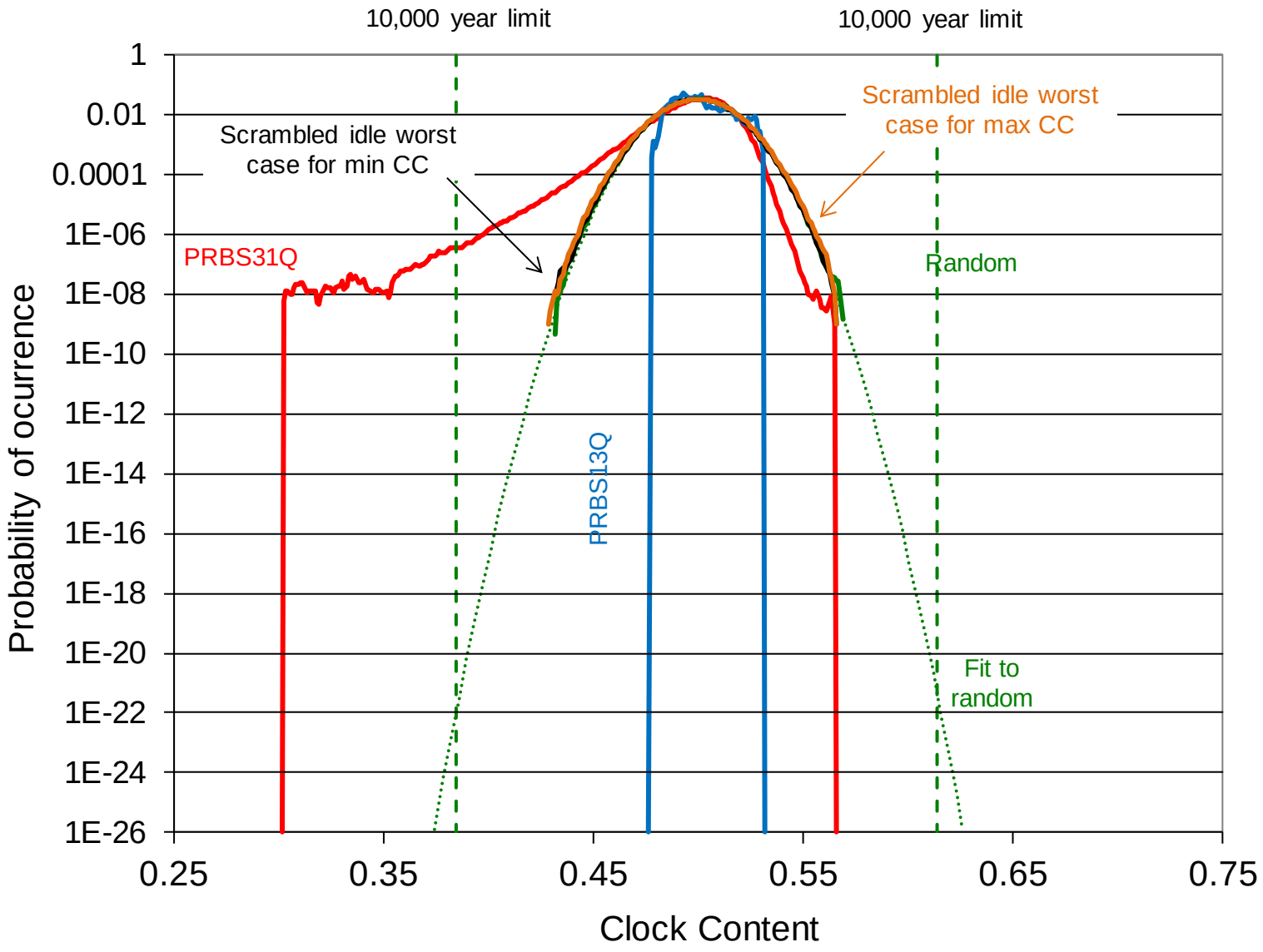
Clock, sym trans through ave, Bd/5313



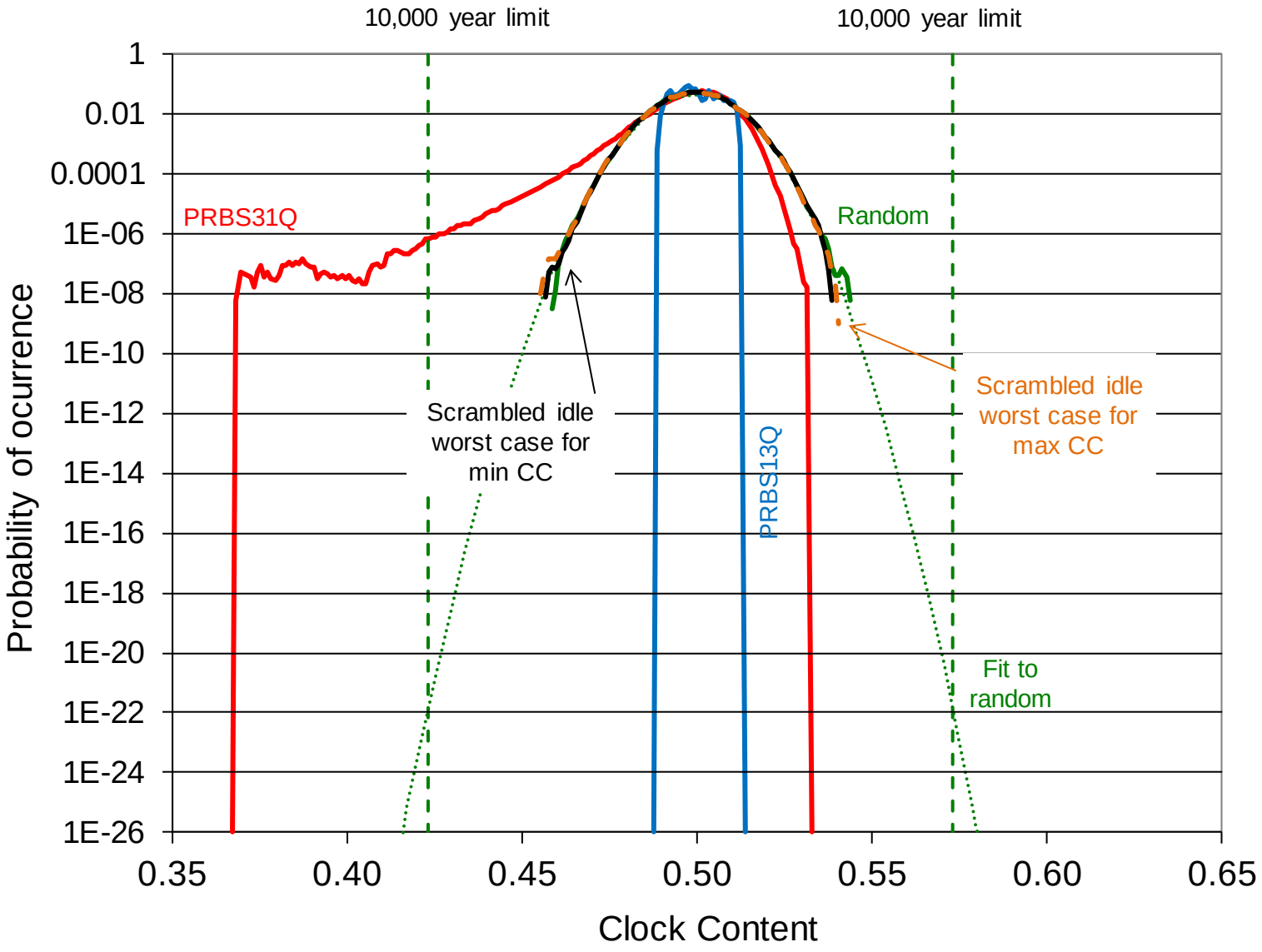
Clock, sym trans through ave, Bd/13281



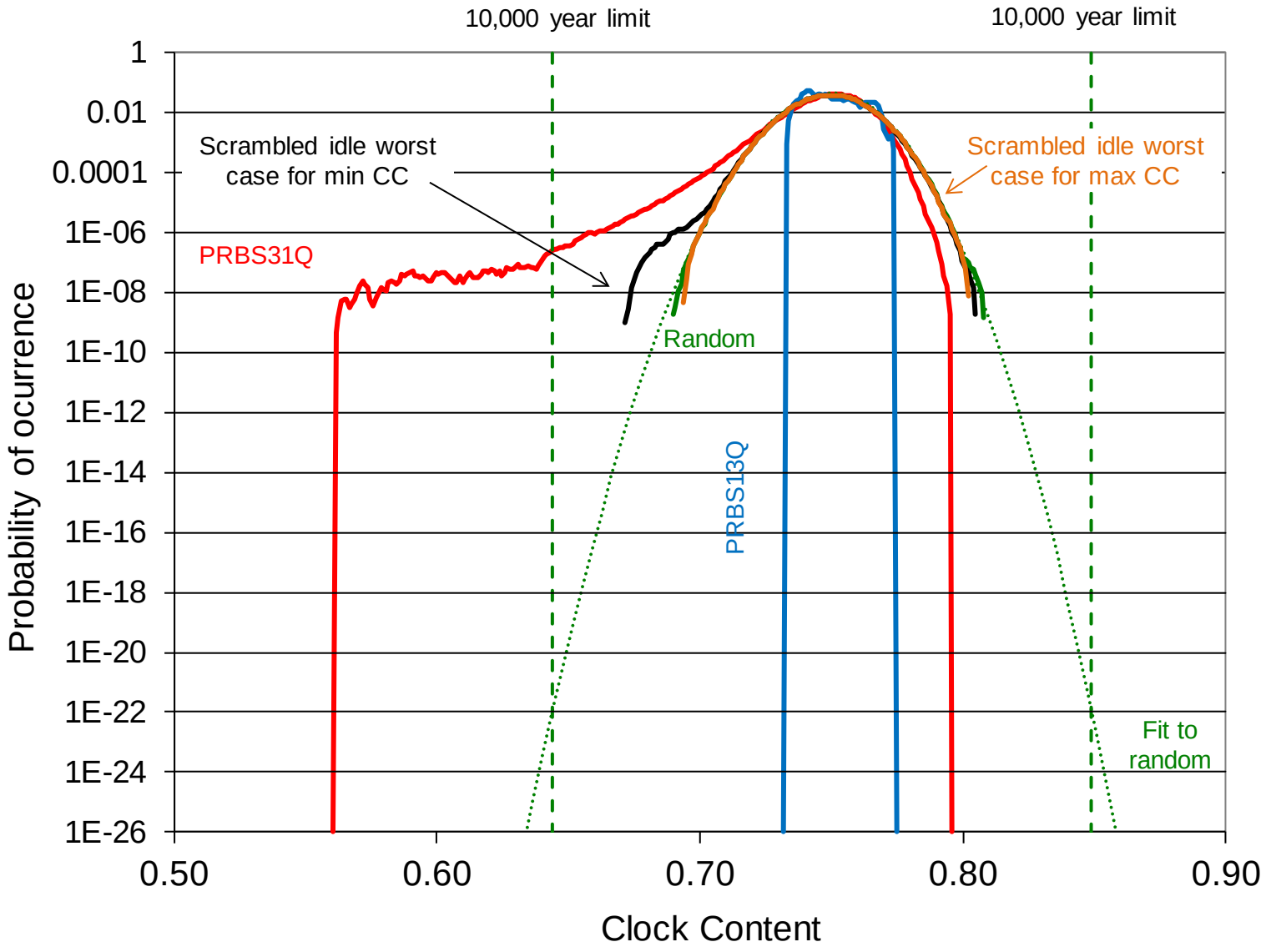
Clock, trans through ave, Bd/5313



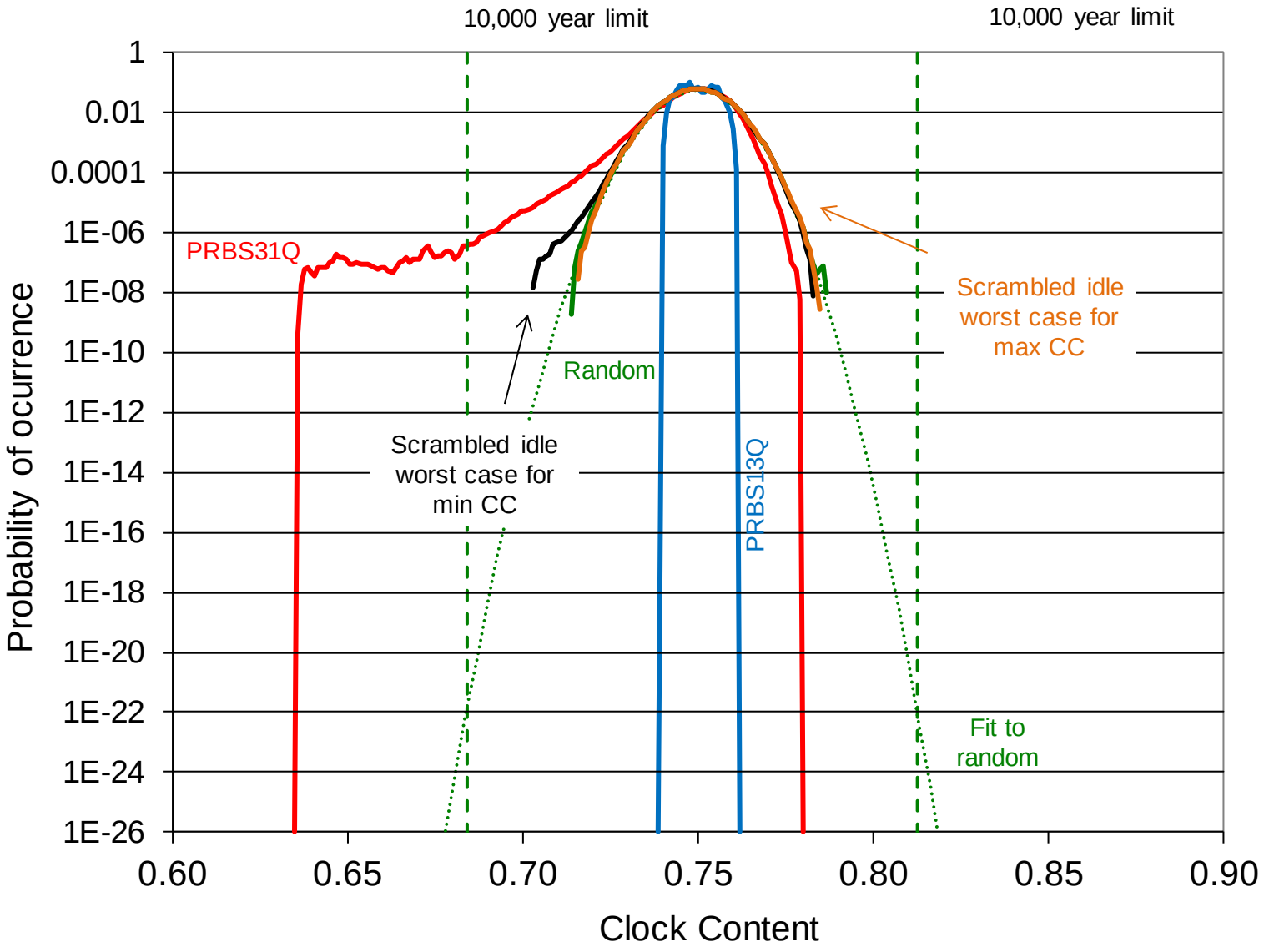
Clock, trans through ave, Bd/13281



Clock, all transitions, Bd/5313



Clock, all transitions, Bd/13281



Conclusion

Removing the second common AM as in:

FEC lane 0	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM4	BIP	$\overline{\text{AM4}}$	$\overline{\text{BIP}}$	AM8	BIP	$\overline{\text{AM8}}$	$\overline{\text{BIP}}$	AM12	BIP	$\overline{\text{AM12}}$	$\overline{\text{BIP}}$	AM16	BIP	$\overline{\text{AM16}}$	$\overline{\text{BIP}}$	Pad	Data
FEC lane 1	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM5	BIP	$\overline{\text{AM5}}$	$\overline{\text{BIP}}$	AM9	BIP	$\overline{\text{AM9}}$	$\overline{\text{BIP}}$	AM13	BIP	$\overline{\text{AM13}}$	$\overline{\text{BIP}}$	AM17	BIP	$\overline{\text{AM17}}$	$\overline{\text{BIP}}$	Data	
FEC lane 2	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM6	BIP	$\overline{\text{AM6}}$	$\overline{\text{BIP}}$	AM10	BIP	$\overline{\text{AM10}}$	$\overline{\text{BIP}}$	AM14	BIP	$\overline{\text{AM14}}$	$\overline{\text{BIP}}$	AM18	BIP	$\overline{\text{AM18}}$	$\overline{\text{BIP}}$	Data	
FEC lane 3	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM7	BIP	$\overline{\text{AM7}}$	$\overline{\text{BIP}}$	AM11	BIP	$\overline{\text{AM11}}$	$\overline{\text{BIP}}$	AM15	BIP	$\overline{\text{AM15}}$	$\overline{\text{BIP}}$	AM19	BIP	$\overline{\text{AM19}}$	$\overline{\text{BIP}}$	Data	

significantly reduces the magnitude of the “shoulder” on the clock content plots for 4:1 bit interleaving, so would be a better candidate AM mapping.

Choosing AM1, AM2, or AM3 as the first common AM might improve this further.

Thanks!