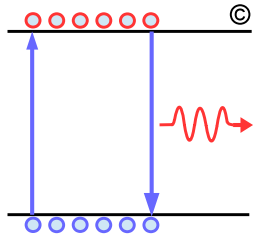


Architectural Support for 50 GbE and 100 GbE Breakout

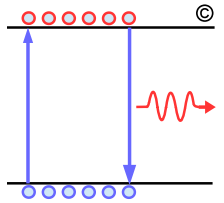
Ali Ghiasi
Ghiasi Quantum LLC

IEEE 802.3cd Task Force Meeting

San Diego

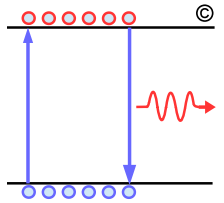
July 26, 2016

Overview



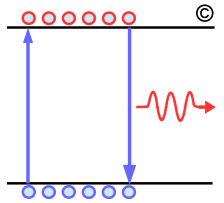
- **Baseline PCS for 50 GbE and NG 100 GbE adopted in Whistler**
  - http://www.ieee802.org/3/cd/public/May16/nicholl_3cd_01a_0516.pdf
  - Leveraging CL82 40 GbE for 50 GbE having 4 PCS lanes
  - Leveraging CL82 100 GbE PCS for NG 100 GbE having 20 PCS lanes
  - Adopted PCS's are compatible with P802.3bs architecture and supports both 25G and 50G IO
- **In Whistler we didn't make a decision on # FEC lanes or distribution to further study the burst error not using the P802.3bs interleaved FEC**
  - TX differential pre-coding was investigated for 50 Gb/s link
    - http://www.ieee802.org/3/cd/public/adhoc/archive/hegde_070616_3cd_01_adhoc.pdf
  - RS(544,514) FEC performance with pre-coding and bit/symbol were investigated
    - http://www.ieee802.org/3/cd/public/adhoc/archive/anslow_070616_3cd_01_adhoc.pdf
  - TX differential pre-coding helps burst error on links with large dominant 1st tap allowing to build a PMA supporting bit-mux and compatible with P802.3bs
  - A PMA supporting bit mux is key to building common ports/modules and breakout applications
- **Use cases for 50GAUI, 50GAUI-2, CAUI-4, and CAUI-2 where investigated in depth in Whistler**
  - http://www.ieee802.org/3/cd/public/May16/ghiasi_3cd_01a_0516.pdf
- **In this contribution the need to support 25G RS(544,514) FEC lanes on 50GAUI-2 in support of breakout applications will be discussed.**

Supporting Breakout Applications

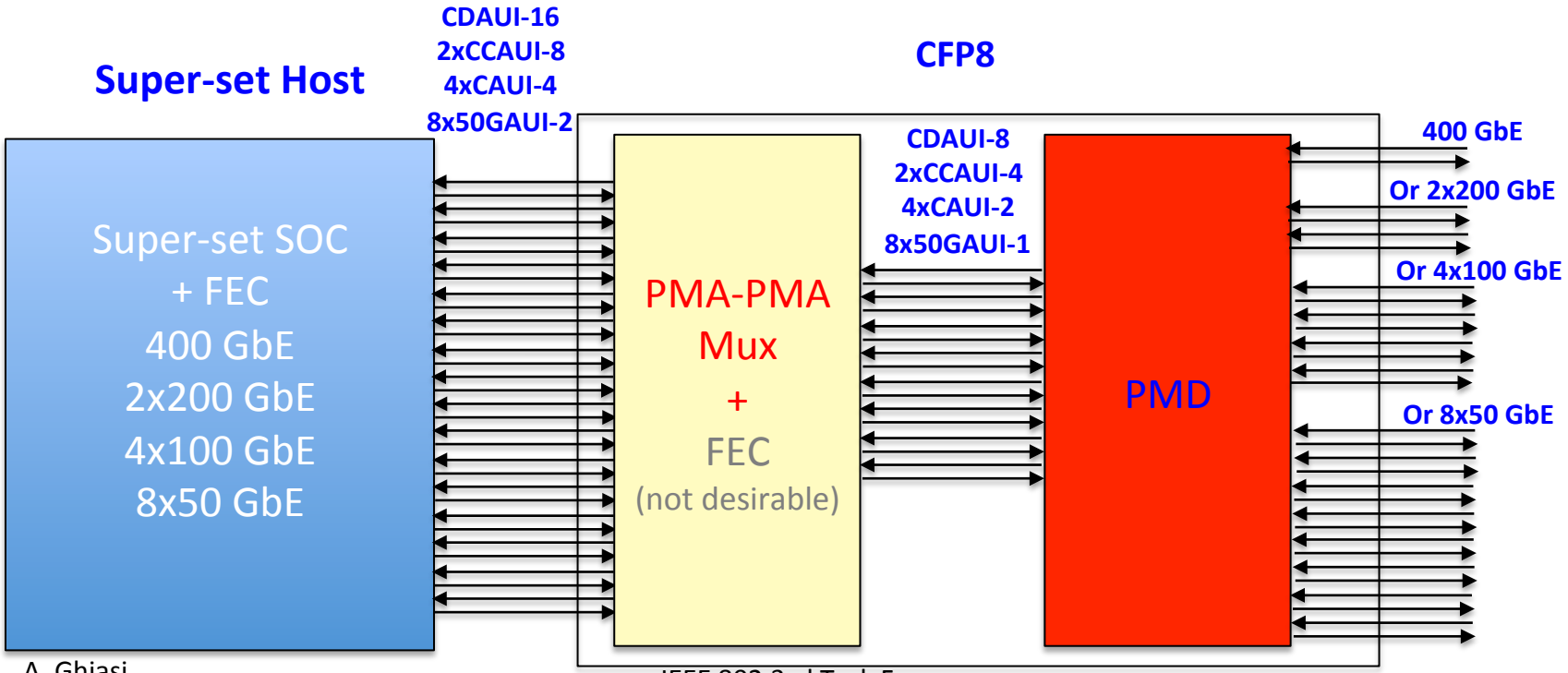


- **QSFP56 – 4x50G (200 GbE)**
  - 2x100 GbE
  - 4x50 GbE
- **QSFP-DD – 8x25G (200 GbE)**
  - 2x100 GbE
  - 4x50 GbE
  - 8x25 GbE (in the time frame not likely application)
- **CFP8 – 16x25G (400 GbE)**
  - 2x200 GbE
  - 4x100 GbE
  - 8x50 GbE
  - 16x25 GbE (in the time frame not likely application)
- **Next will examine architectural requirement to support breakout.**

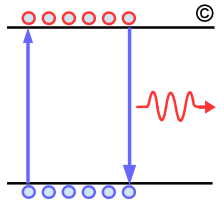
Supporting Breakout in CFP8



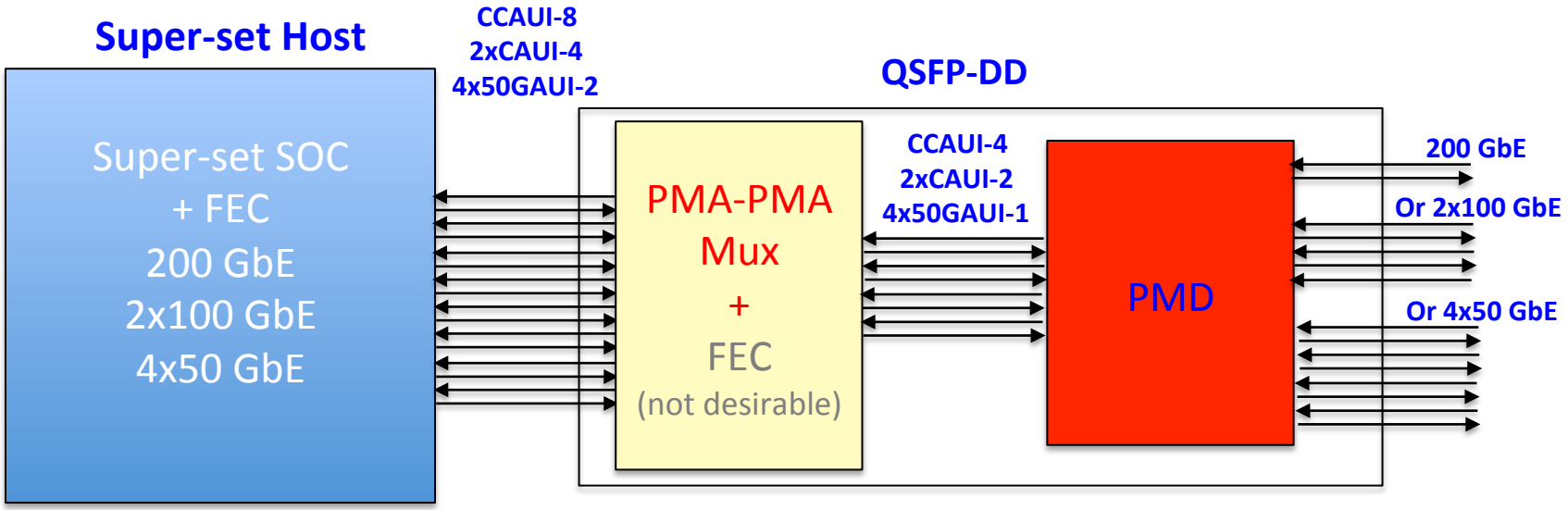
- **PCS baseline already supports 25G PCS lane ✓**
  - http://www.ieee802.org/3/cd/public/May16/nicholl_3cd_01a_0516.pdf
- **FEC also needs to support 25G FEC lane**
  - Currently 200 GbE/400 GbE support 25G FEC lanes and allow implementing FEC into 25G IO host ASIC
  - Unless 50 GbE and NG 100 GbE supports 25G FEC lane then FEC is forced into the CFP8 module resulting in more complex module
  - FEC architecture recommended to support 25G FEC lanes in support of breakout application, flexibility, compatibility with BS, and allow FEC to reside on host ASIC or in the PMA-PMA chip.



Supporting Breakout in QSFP-DD

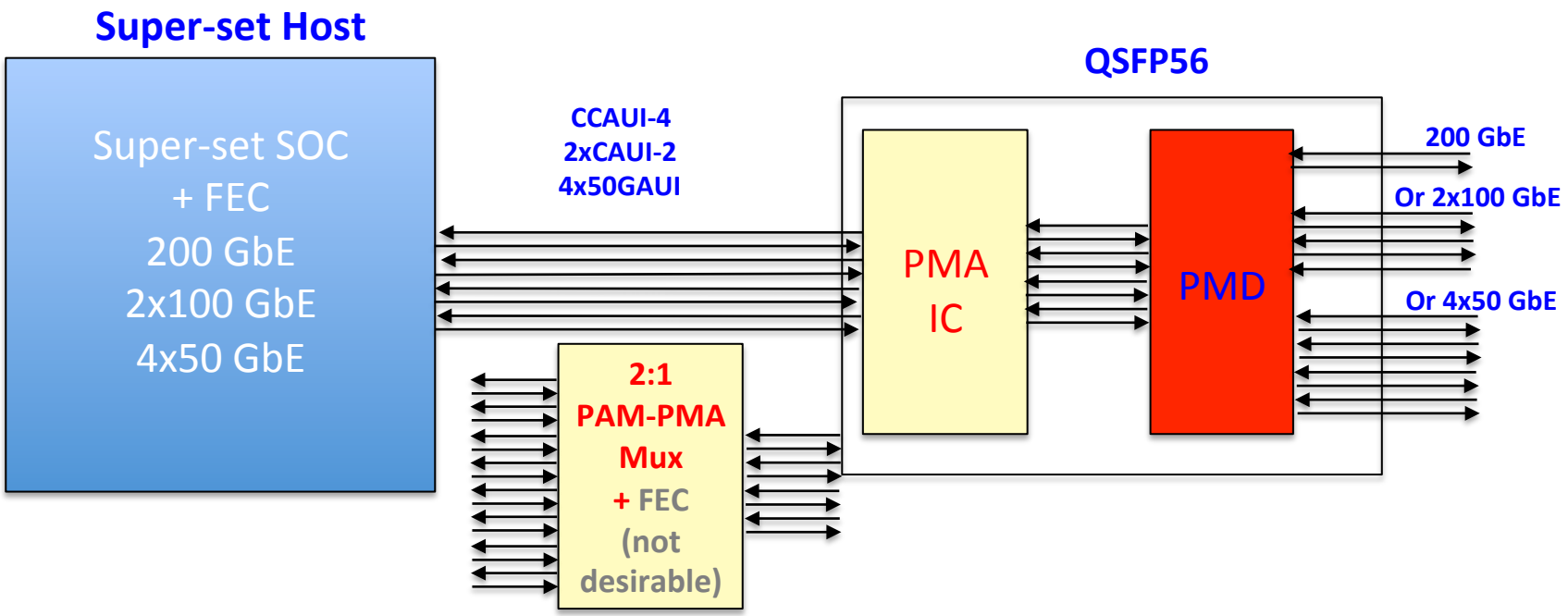


- **PCS baseline already supports 25G PCS lane ✓**
  - http://www.ieee802.org/3/cd/public/May16/nicholl_3cd_01a_0516.pdf
- **FEC also needs to support 25G FEC lane**
  - Currently 200 GbE/400 GbE support 25G FEC lanes allow implementing FEC into 25G host ASIC
  - Unless 50 GbE and NG 100 GbE supports 25G FEC lanes then FEC is forced into the QSFP-DD module resulting in more complex module and possibly exceeding QSFP-DD power envelope
  - FEC architecture recommended to support 25G FEC lanes in support of breakout application, flexibility, compatibility with BS, and allow FEC to reside on host ASIC or in the PMA-PMA chip.

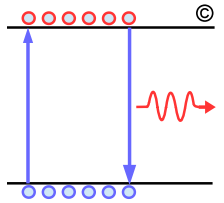


Supporting Breakout in QSFP56

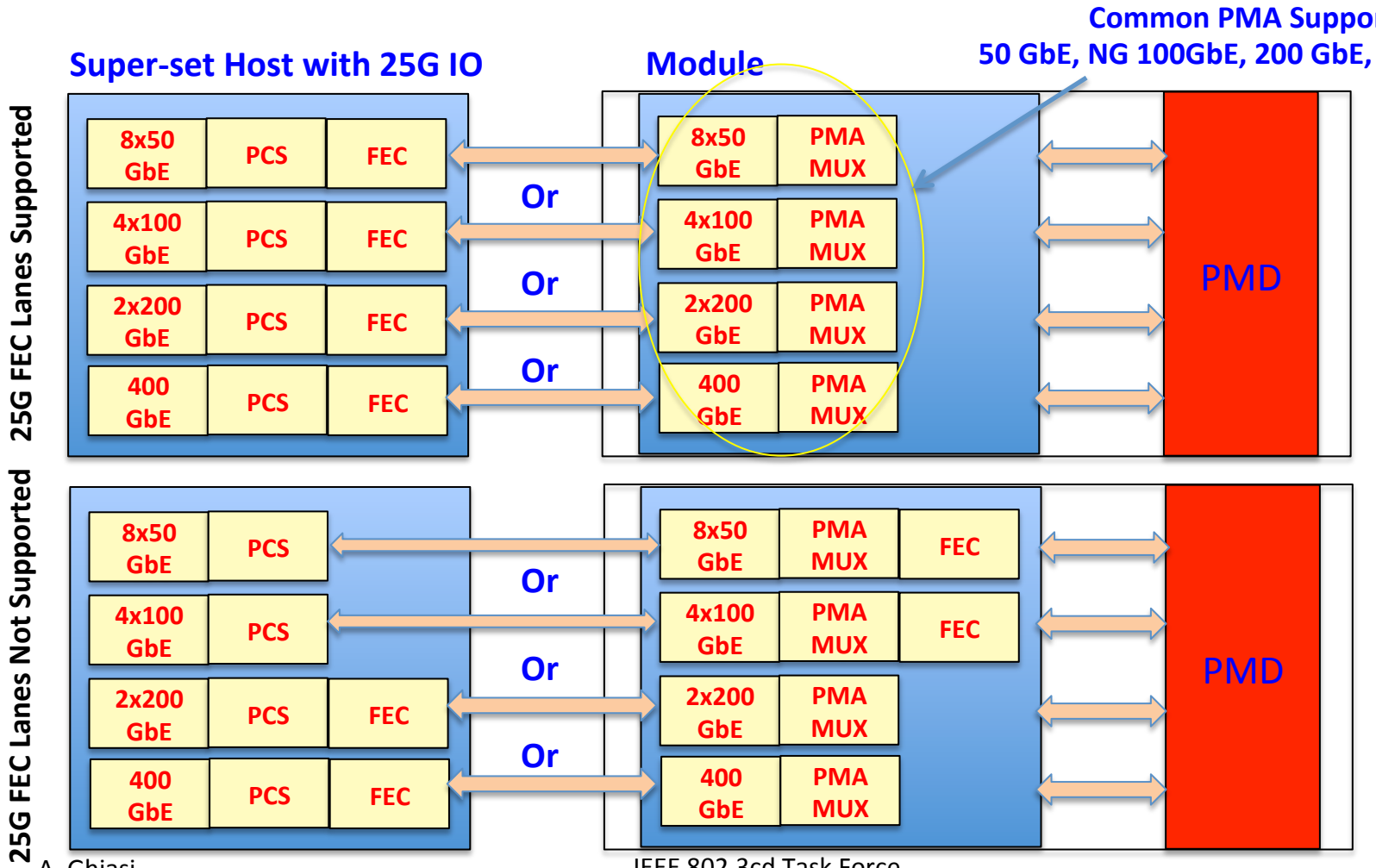
- **PCS baseline already supports 25G PCS lane ✓**
  - http://www.ieee802.org/3/cd/public/May16/nicholl_3cd_01a_0516.pdf
- **QSFP56 having native 50G IO is designed to operate with native 50G host IO but early ASIC implementation my require 2:1 PMA-PMA mux**
  - Currently 200 GbE/400 GbE support 25G FEC lanes and allow implementing FEC into 25G host ASIC
  - Any 2:1 PMA-PMA mux/FEC on the line card it will not add complexity or power to the QSFP56
  - FEC architecture supporting 25G FEC lanes provide benefit even in this scenario by allowing optimizing the implementation based on availability host ASIC/FPGA and PMA-PMA Mux.



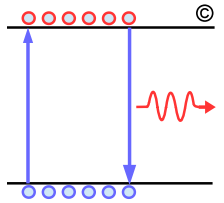
Supporting Breakout



- **In addition to the PCS supporting 25G lanes for ease of implementation FEC needs to support 25G lanes as well!**



Summary



- **Commonality of PMA and where possible PMD with 802.3bs allow broadest set of breakout applications**
  - 50 GbE will be most common breakout from 200G ports
  - 100 GbE will be the most common breakout from 400G ports
- **Adhoc investigation of (544,514) FEC with differential pre-coding indicate PMA bit mux can be support on non-interleaved 50 GbE/NG 100 GbE allowing to build common PMA/module supporting P802.3bs applications**
- **The 50 GbE and NG 100 GbE PCS supports 25 PCS lane which allow early implementation as well as more efficient 2nd generation implementations based on 50G IO**
- **Recommend FEC to also support 25 FEC lane for compatibility with P802.3bs and allow breakout application using a common PMA IC without the need to force FEC into the module.**