The need for 25G electrical lanes support

IEEE P802.3 50 Gb/s, 100 Gb/s, and 200 Gb/s Ethernet Task Force

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Introduction

- These slides discuss why we should support 25G per lane electrical interfaces (C2C and C2M) for the next generation 100GbE/50GbE interfaces

Test Equipment Background

- Test equipment extensively uses FPGAs, modest volumes rules out custom ASICs
- Test equipment must be available early to enable the market:

Challenges – FPGA impact

- Protocol aware test equipment is usually based on high end FPGAs
  - Time to market
  - Flexibility
  - Address future protocols and emerging standards
- So products 'gated' by FPGA
  - I/O speed (and performance)
  - Size (FEC, PCS, Logic)

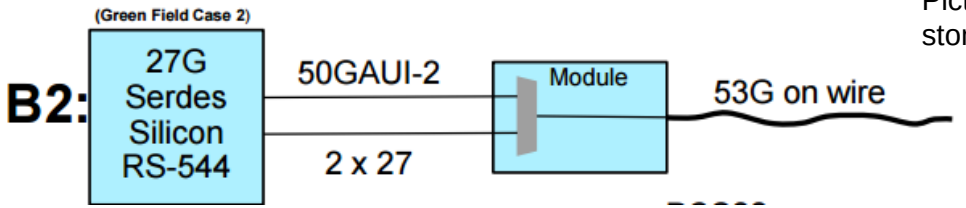
- Expectation is to have 'real' test equipment ready ~18 months before standard.

brooks_3bs_01a_0115.pdf

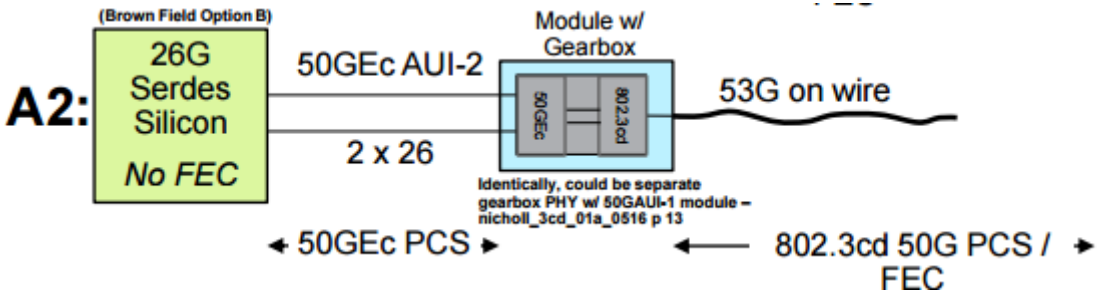
The Need for 25G

- There has been demonstrations of 50G SerDes by major FPGA vendors, but devices with 50G integration are not available in the market in the near term
- There are two options to enable next generation 50GbE/100GbE:
  1. Enable natively 25G electrical lanes with FEC and bit muxing support in the standard directly
     - This is by far the preferred mode as long as it is feasible
     - Enables test equipment to include FEC in the FPGA natively, allows control of test cases, error insertion, negative testing etc.

Pictures from stone_060816_3cd_01a_adhoc.pdf



  2. If the above is not possible, rely on an external mux device with FEC in them
     - This is used only as a last resort due to loss of flexibility and control



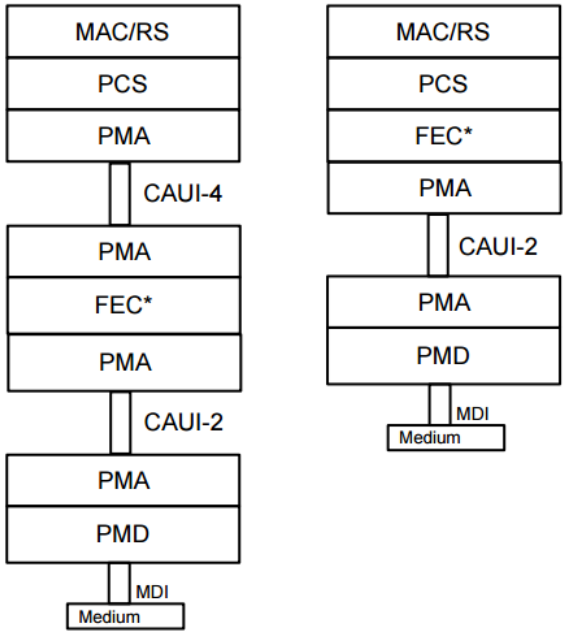
Impact to the Spec

- For 100GbE you can use the PCS/FEC from 802.3bj directly and keep the distribution to four FEC lanes, and then allow bit muxing down to two lanes
  - Almost identical to nicholl_3cd_01a_0516.pdf with the exception of the FEC distribution
- Need to add the 26G rate to the CAUI-4 interface (leverage similar specs from CDAUI-16/CCAUI-8)
- 50GbE architecture is similar

NG 100GbE Overview

- Separate PCS & FEC sub-layers
  - same as current 100GbE architecture
  - allows PCS and FEC to be physically separated
- Existing 100GbE (CL82) PCS
  - no changes proposed
  - supports optional CAUI-4 /w no-FEC
- RS (544,514) FEC
  - based on 802.3bj (CL 91) but distributed over 2 FEC lanes
  - optimized for 50 Gb/s lane rate AUI and PMD
  - no FEC codeword interleaving (minimize latency)

nicholl_3cd_01a_0516.pdf

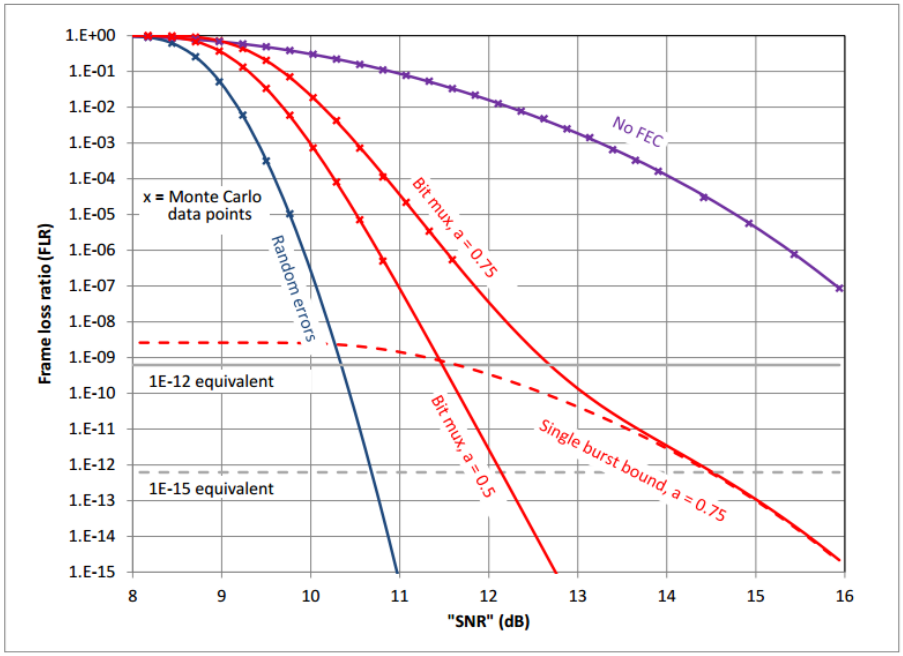


*FEC is a separate sublayer

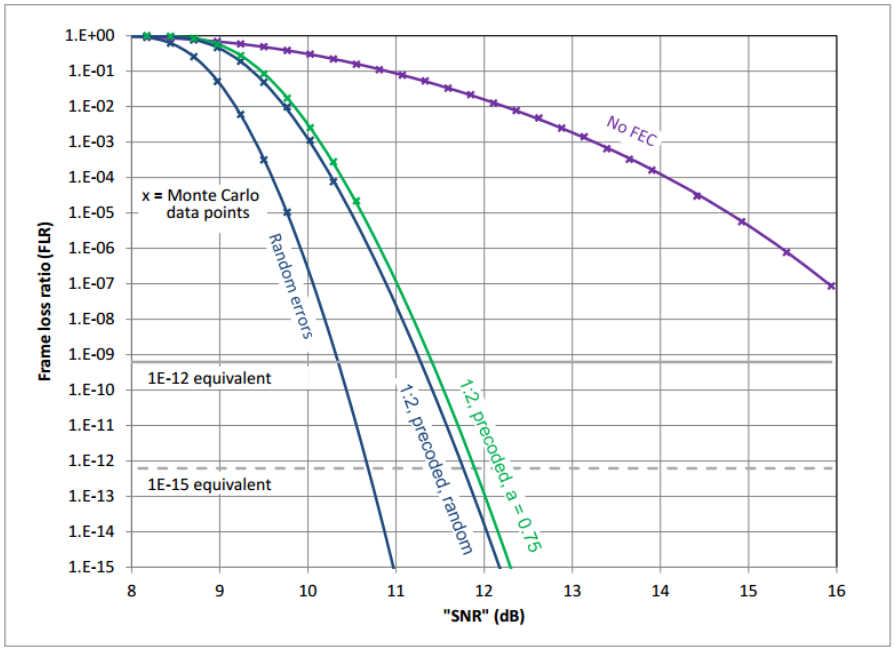
Impact to Link Performance

- As shown in anslow_070616_3cd_01_adhoc and hegde_070616_3cd_01_adhoc, with the combination of precoding for receivers that have heavy first tap DFE and with a lower probability of long error bursts with other receiver types, the impact to performance budgets is extremely small

RS(544,514) 2:1 bit mux



RS(544,514) 2:1 bit mux with precoding



anslow_070616_3cd_01_adhoc.pdf

Summary

- Supporting 25G electrical (C2C and C2M) for next generation 100GbE/50GbE is feasible and should be supported in the standard
- Very minor performance degradation due to bit muxing when coupled with pre-coding
- Consistent with 400GbE/200GbE where 25G electrical interfaces are natively supported
- Minor changes to the specification, in fact it simplifies the FEC sublayer for 100GbE
- Enables the test market which is required for everyone else to be successful
- Support for 25G electrical (C2C and C2M) interfaces for next generation 100GbE/50GbE is feasible and should be supported in the standard

Thanks!