Baseline proposal for the 100 Gb/s SMF PHY 2 km objective using single wavelength PAM4 modulation 100GBASE-FR

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802.3cd Objectives: v2

100 Gb/s Ethernet PHYs

- Define a two-lane 100 Gb/s PHY for operation over
  - copper twin-axial cables with lengths up to at least 3m.
  - printed circuit board backplane with a total channel insertion loss of <= 30dB at 13.28125 GHz.
  - MMF with lengths up to at least 100m
  - SMF with lengths up to at least 500m
- Define a 100 Gb/s PHY for operation over SMF with lengths up to at least 2 km

(*) http://www.ieee802.org/3/cd/P802d3cd_objectives_v2.pdf

Motivation

- Single lane implementation has delivered lowest cost in high volume optical interfaces
- Significant industry investment in building blocks for 100Gbps/λ
- Leveraging single lane of 400GBASE-DR4 being standardized in 802.3bs
  - Provides path for physical breakout of 400GBASE-DR4

Technical Feasibility

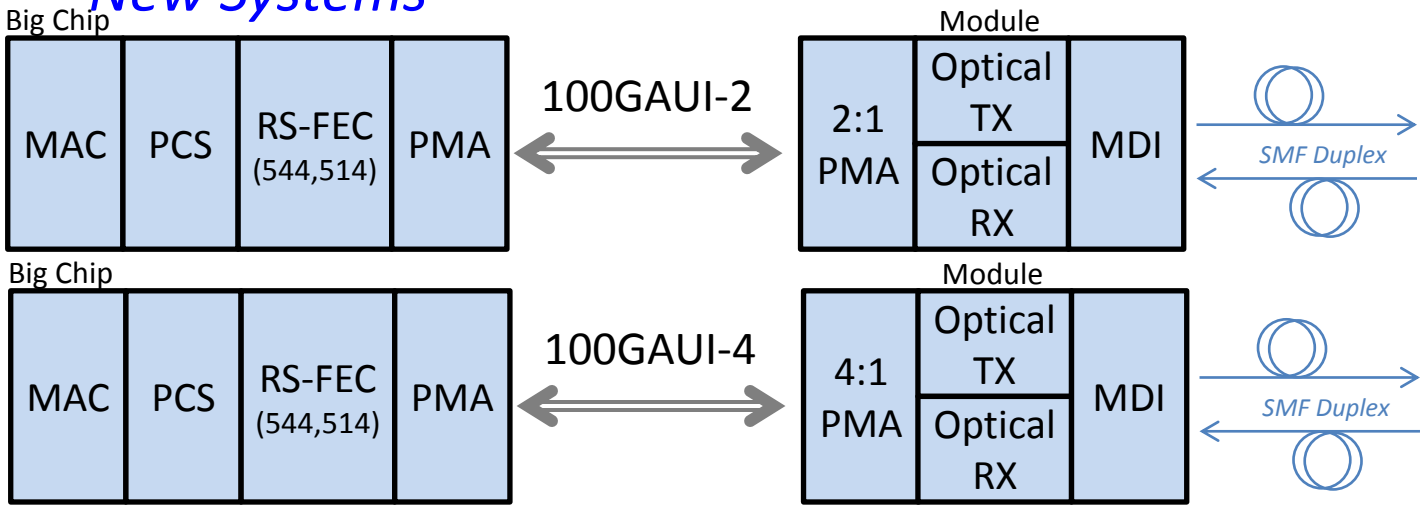
- Refer/pointers to separate presentation(s)
  - Planned presentation(s) at July meeting
    - traverso_3cd_01_0716
  - 802.3bs DR4 links
    - mazzini_02a_1215_smf
    - tipper_3bs_01a_0515
    - way_3bs_01_0515
    - welch_3bs_02a_0115

Baseline Proposal for 100GBASE-FR

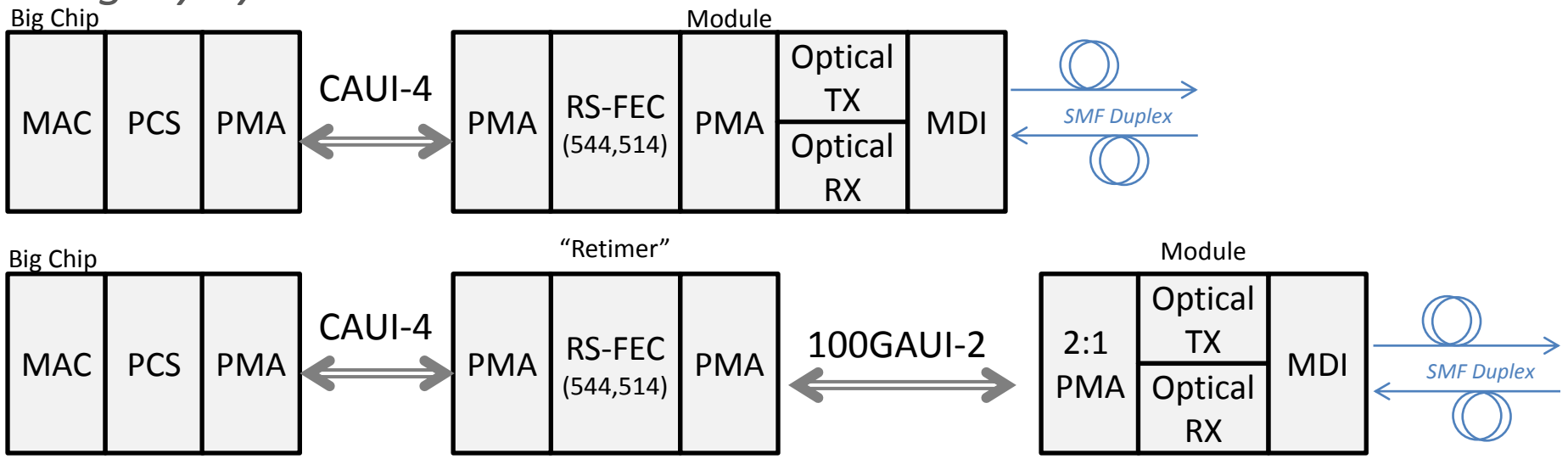
- Single optical lane per direction using PAM4 modulation at 53.125 GBaud over duplex fiber
- Presumes RS(544,514) FEC with a pre-FEC BER target of 2.4×10^{-4}
- New mode of operation for PMA required to support to 100G serial bit stream
  - 4:1 and 2:1 PMAs need to be defined (trivial)

Use cases for 100GBASE-FR

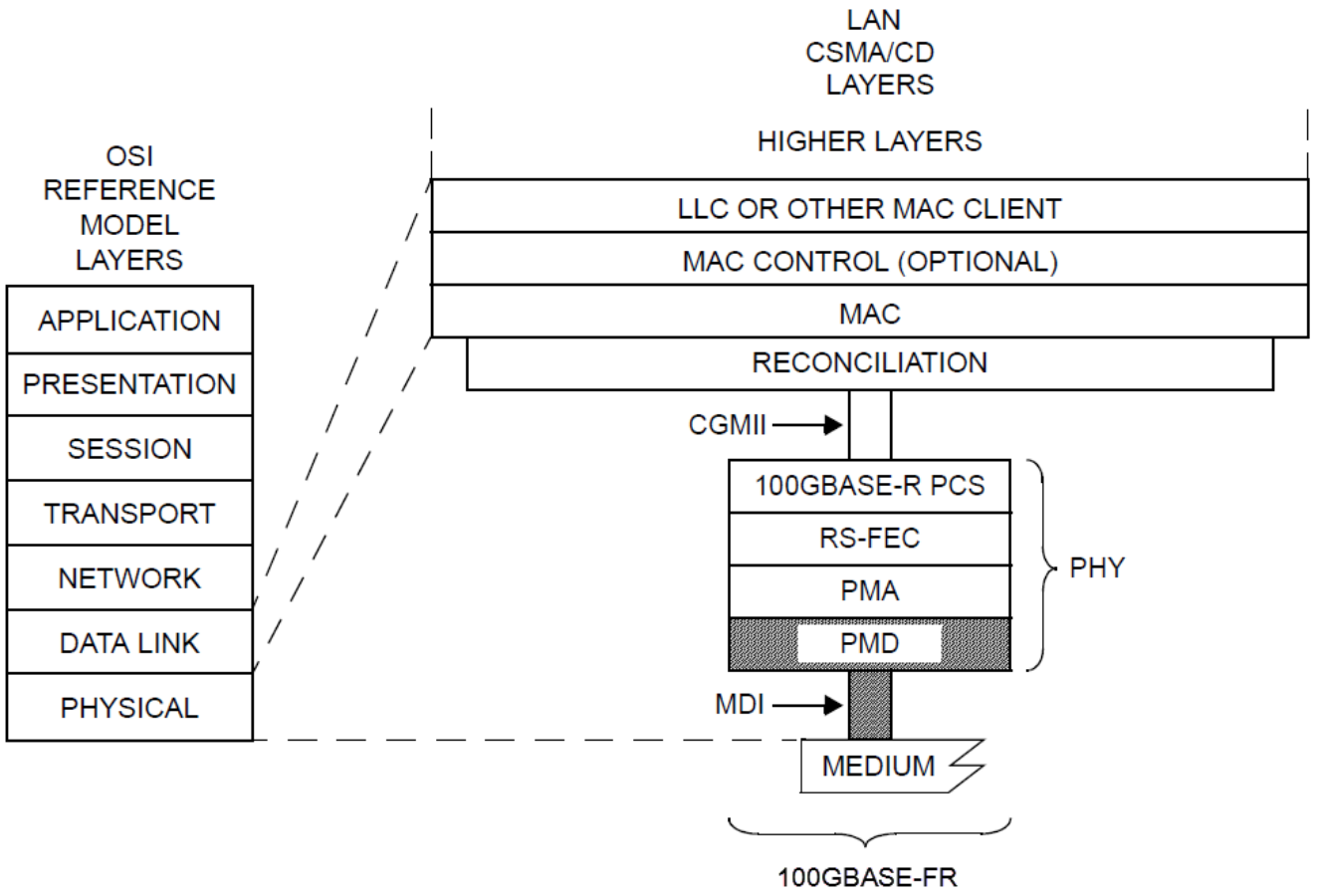
New Systems



Legacy Systems



100GBASE-FR: Position in 802.3 architecture



CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION
FR = PMD FOR SINGLE-MODE FIBER - 2 KM

Proposed Transmitter Specification

Description	100GBASE-FR Proposal	400GBASE-DR4, D1.5	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm	53.125 ± 100 ppm	GBd
Modulation format	PAM4	PAM4	-
Lane wavelength (range)	1304.5 to 1317.5	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	30	dB
Average launch power, each lane (max)	4	4	dBm
Average launch power, each lane (min)	-2.4	-2.4	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	4.2	4.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)	-0.3	-0.3	dBm
Launch power in OMA_{outer} minus TDECQ, (min)	-1.3	-1.3	dBm
Transmitter & dispersion eye closure for PAM4 (TDECQ), each lane (max)	2.5	2.5	dB
Average launch power of OFF transmitter, each lane (max)	-30	-30	dBm
Extinction ratio, each lane (min)	5	5	dB
$RIN_{17.8}OMA$	-142, tbc	-	dB/Hz
$RIN_{22.8}OMA$	-	-142	
Optical return loss tolerance (max)	17.8	22.8	
Transmitter reflectance (max)	-26	-26	dB

Proposed Receiver Specification

Description	100GBASE-FR Proposal	400GBASE-DR4, D1.5	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm	53.125 ± 100 ppm	GBd
Modulation format	PAM4	PAM4	-
Lane wavelength (range)	1304.5 to 1317.5	1304.5 to 1317.5	nm
Damage threshold , each lane	6.5	6.5	dBm
Average receive power, each lane (max)	4	4	dBm
Average receive power, each lane (min)	*-6.4*	-5.4	dBm
Receive power (OMA_{outer}), each lane (max)	4.2	4.2	dBm
Receiver reflectance (max)	-26	-26	dB
Receiver sensitivity (OMA_{outer}), each lane (max)	*-5.6*	-4.4	dBm
Stressed receiver sensitivity (OMA_{outer}), each lane (max)	*-3.1*	-1.9	dBm
Conditions of stressed receiver sensitivity test:			
Stressed eye closure for PAM4 (SECQ), lane under test	2.5	2.5	dB
OMA_{outer} of each aggressor lane	4.2	4.2	dBm

Illustrative 100GBASE-FR link budget

Description	100GBASE-FR Proposal	400GBASE-DR4, D1.5	Unit
Power budget (for max TDECQ)	6.8	5.6	dB
Operating distance	2000	500	m
Channel insertion loss	4	3	dB
Maximum discrete reflectance	-35	-45	dB
Allocation for penalties (for max TDECQ)	2.8	2.6	dB
Additional insertion loss allowed	0	0	dB

Conclusion

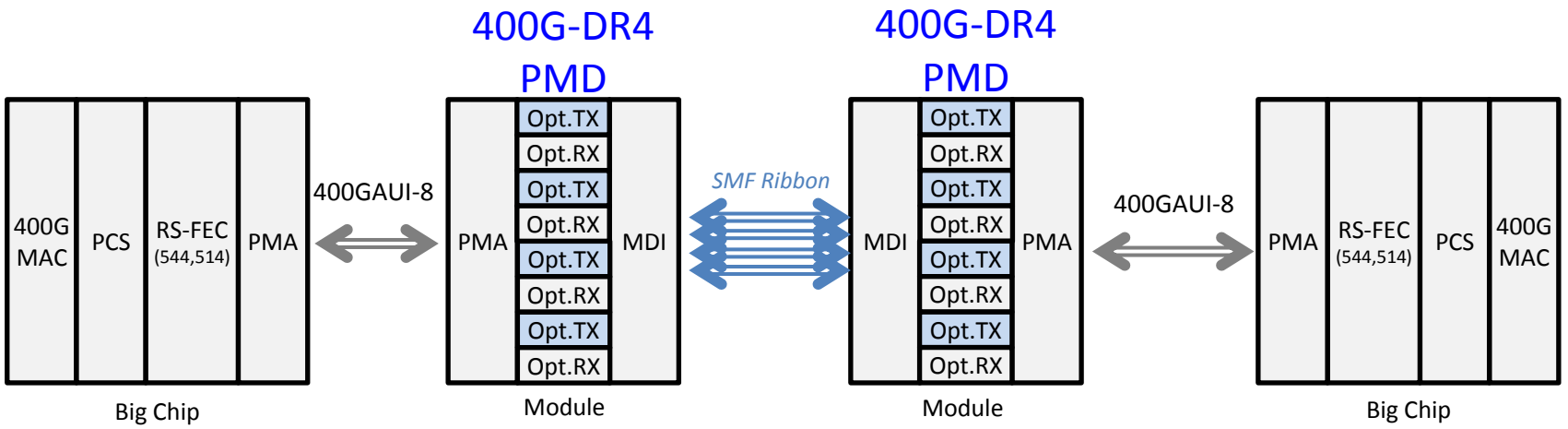
- Baseline proposal for 100GBASE-FR based on FEC-supported 53.125 GBd PAM4 modulation
- Builds on substantial industry investment in 100Gbps/λ by multiple vendors
- Provides a path to breakout applications with 400GBASE-DR4

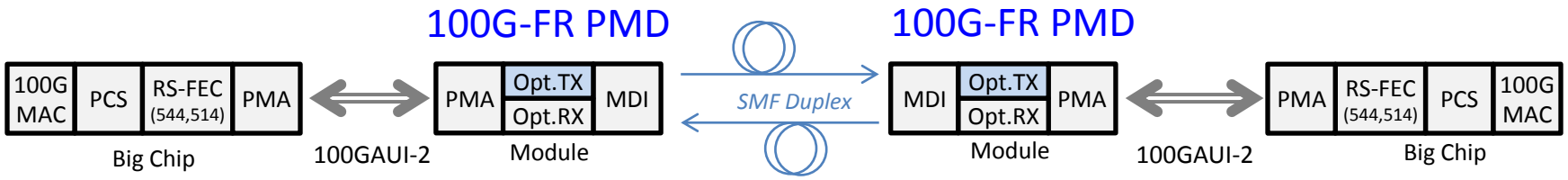
Proposal

- Propose to adopt lewis_3cd_01_0716.pdf as the baseline to address the 100 Gb/s SMF over 2km objective

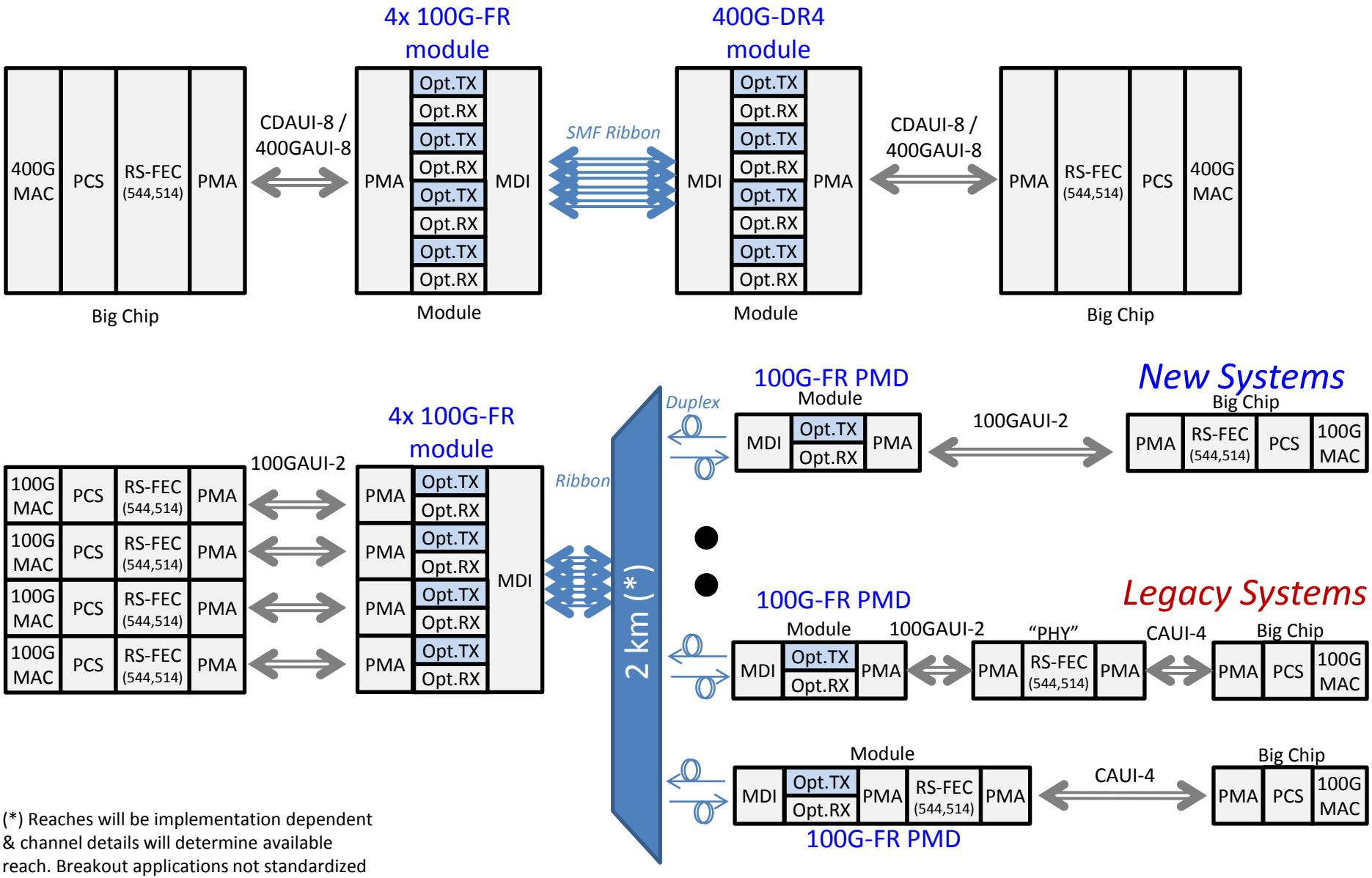
BACKUP

Direct Applications





Breakout Applications



(*) Reaches will be implementation dependent & channel details will determine available reach. Breakout applications not standardized within IEEE.