PreFEC BER Signaling Features

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2016-07 : San Diego, CA

Supporters

Background

- We added PreFEC BER monitoring features to 802.3bs

- History:
  - maki_3bs_01a_1115.pdf – Background and Justification
  - ofelt_3bs_01a_0116.pdf – Initial proposal
  - ofelt_3bs_01_0316.pdf
  - ofelt_3bs_01_0416_logic.pdf
  - ofelt_3bs_01_0516.pdf

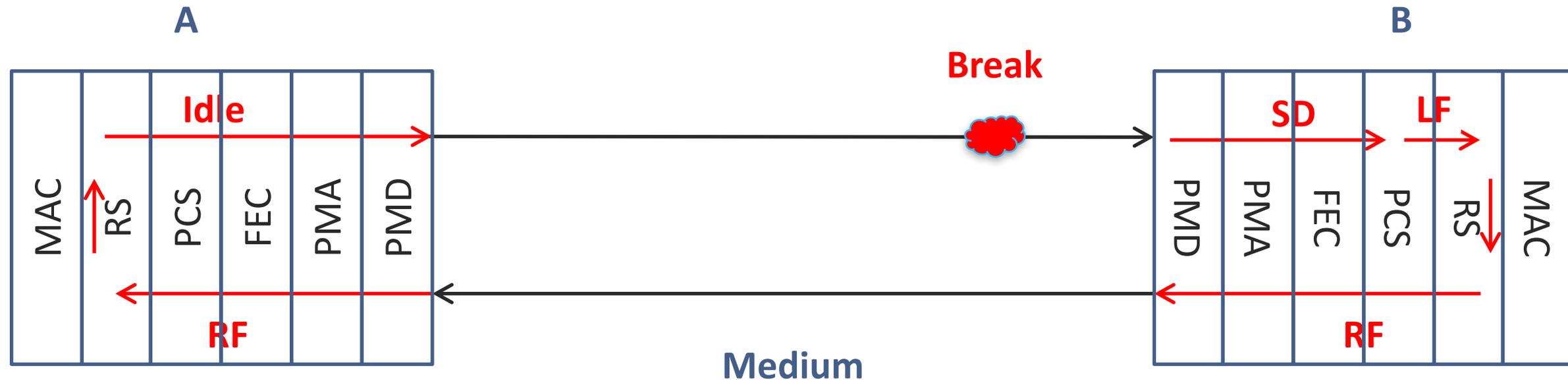- The features are interesting for many of the usecases in 802.3cd

PreFEC Degrade

- Degrade
  - Separate activate and de-activate threshold with shared interval

- Set if corrected symbols in Period is more than the Assert threshold

- Cleared if corrected symbols in Period is less than the Deassert threshold
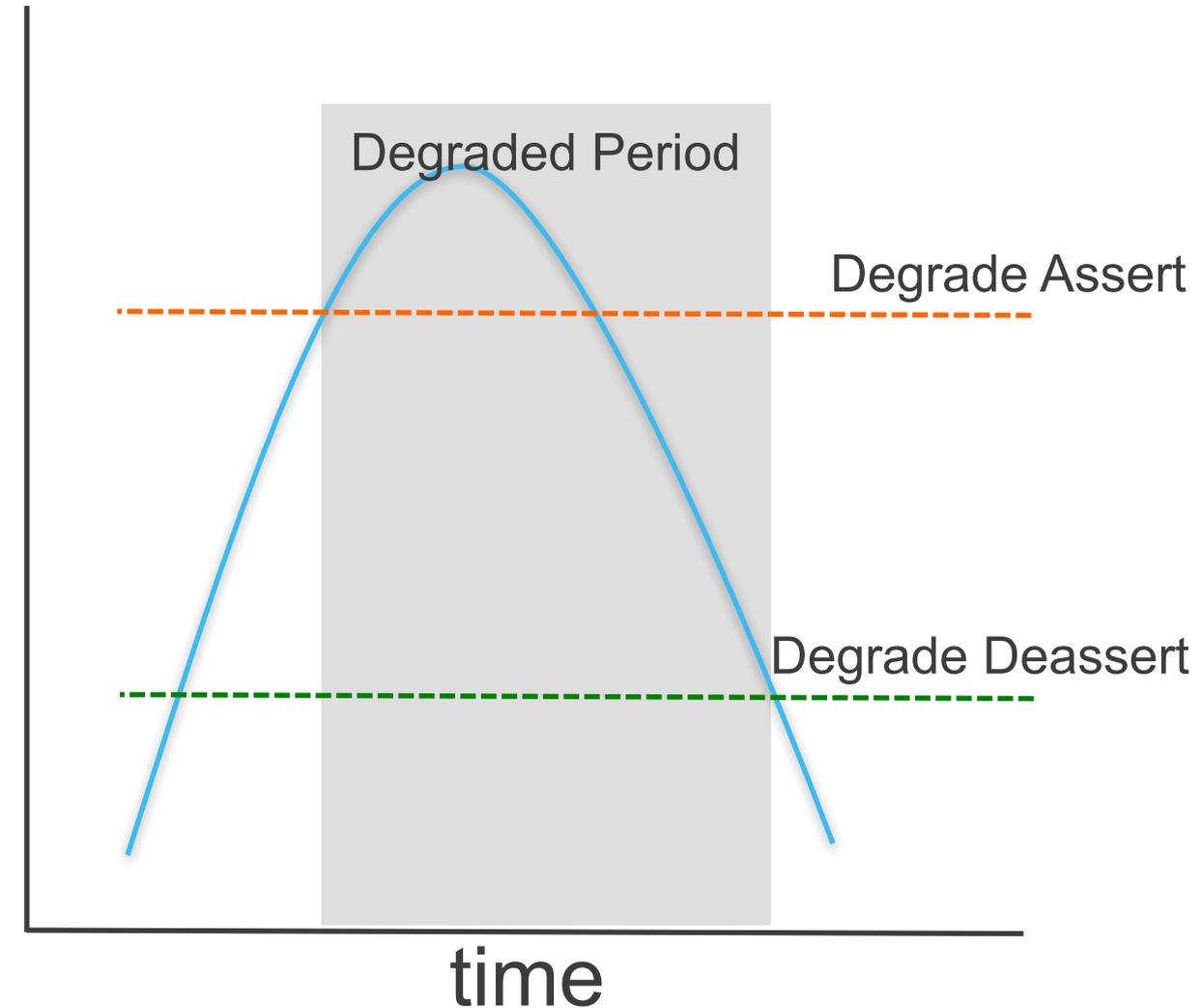
Existing local fault / remote fault


Use-case figures from Pete Anslow, Ciena

- PMD Rx at B sets SIGNAL_DETECT (SD) to FAIL
- PCS at B sends local fault (LF) to RS at B
- RS at B sends remote fault (RF) to A
- RS at A receives RF and sends all idle characters

Pre-FEC degrade FEC integrated in host ASIC

A

B

Degrade

MAC RS PCS FEC PMA PMD

RD

Medium

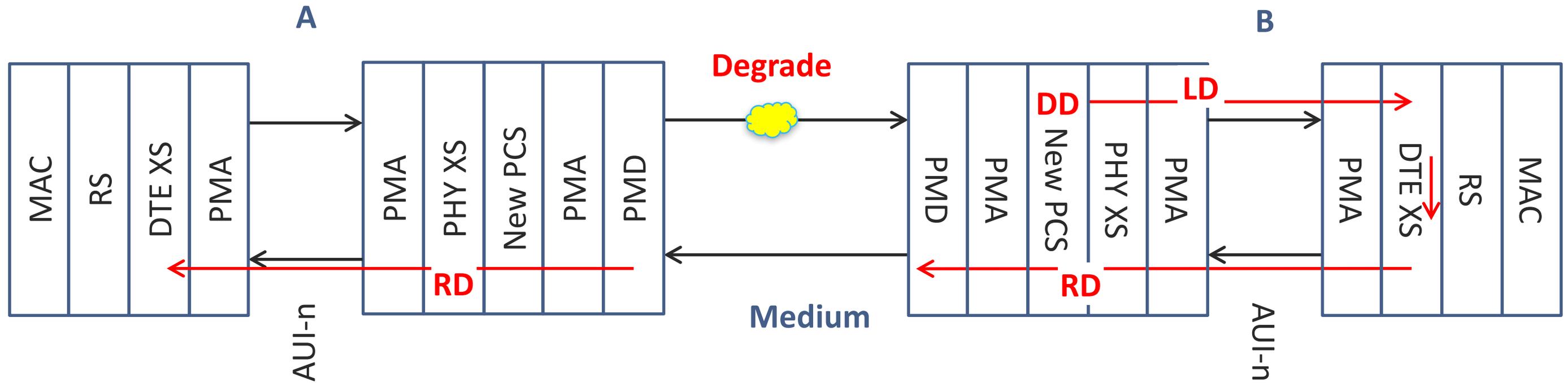PMD PMA FEC PCS RS MAC

DD

RD
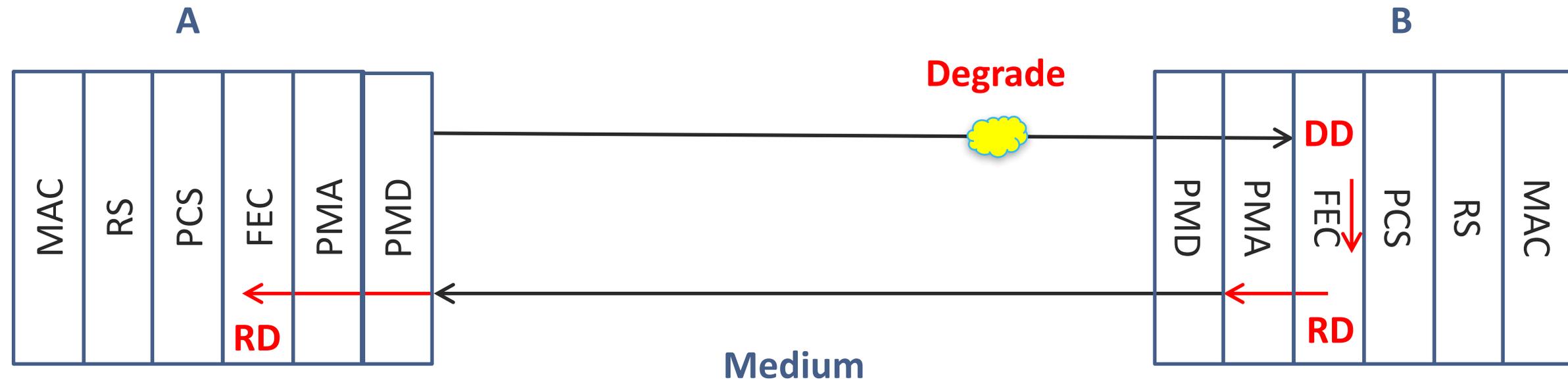
- FEC at B exceeds pre-FEC symbol error ratio (SER) threshold and detects degrade (DD)
- FEC at B sends remote degrade (RD) to PCS at A
- Traffic unaffected
- Is the PCS involved at all?

Pre-FEC degrade legacy host ASIC
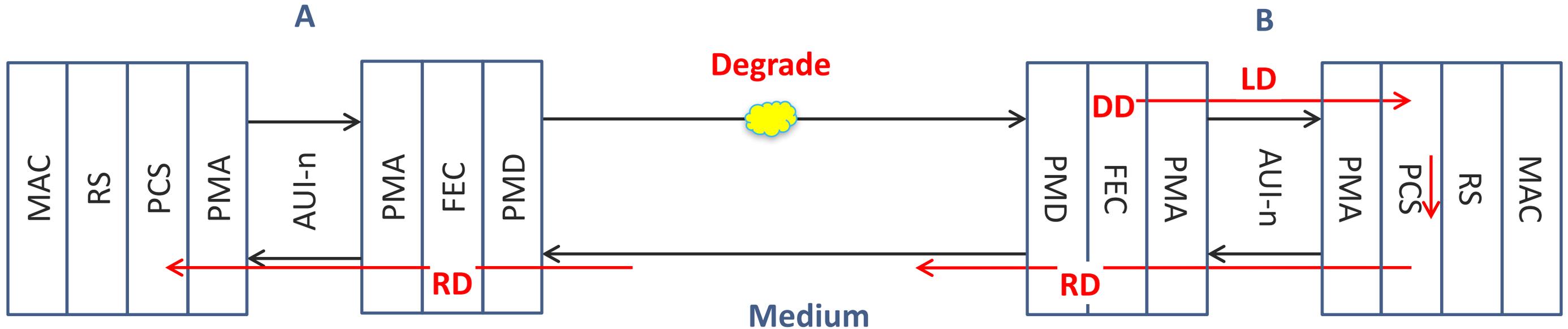
- External FEC at B exceeds pre-FEC symbol error ratio (SER) threshold and sends local degrade (LD) to PCS at B

- DTE XS at B sends remote degrade (RD) to PCS at A

- Traffic unaffected

- Unclear how to signal over the AUI since legacy is defined
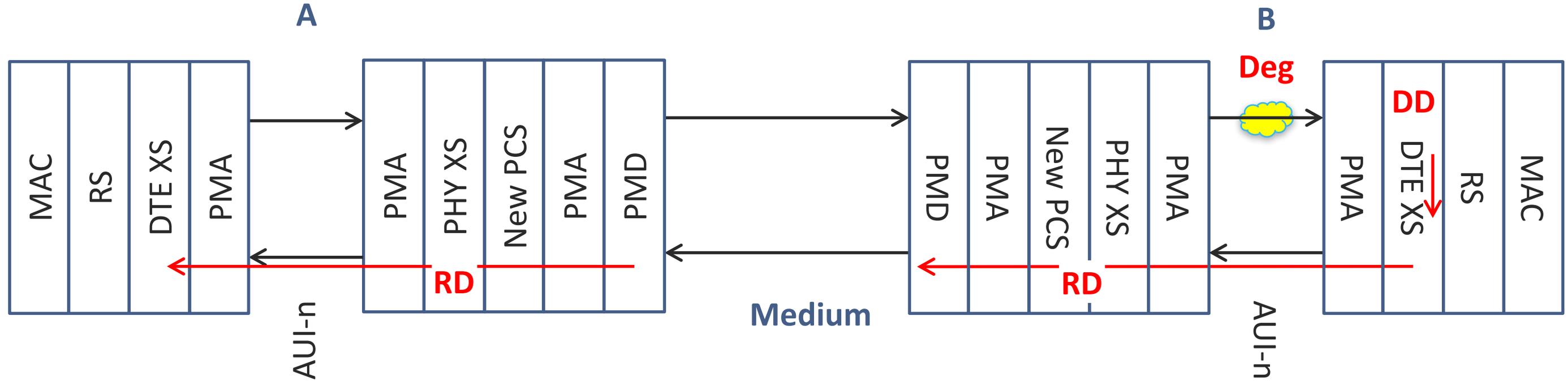   - Punt?

.3bs Pre-FEC degrade with extender sublayer 1

- New PCS at B exceeds pre-FEC symbol error ratio (SER) threshold and sends local degrade (LD) to DTE XS at B

- DTE XS at B sends remote degrade (RD) to DTE XS at A

- Traffic unaffected

.3bs Pre-FEC degrade with extender sublayer 2

- DTE XS at B exceeds pre-FEC symbol error ratio (SER) threshold and sends remote degrade (RD) to DTE XS at A
- Traffic unaffected

.3bs Pre-FEC degrade with extender sublayer 3
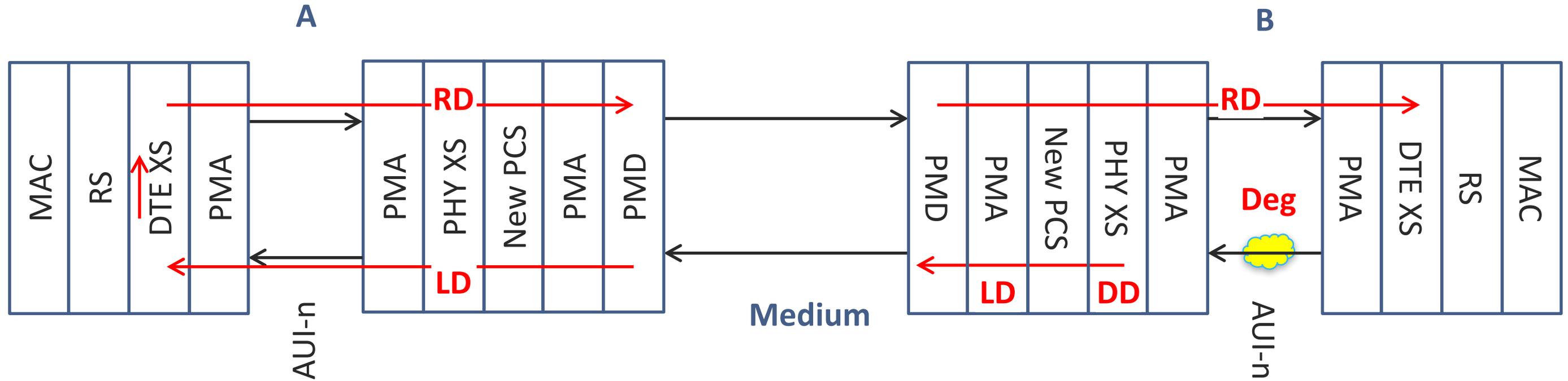
- PHY XS at B exceeds pre-FEC symbol error ratio (SER) threshold and sends local degrade (LD) to DTE XS at A
- Traffic unaffected

Scope of the changes

- 802.3bs Changed:
  - PCS clause (119)
  - Extender Sublayer Clause (118)
  - Added Management registers & bits (45)
- For 802.3cd:
  - Propose adding the same PreFEC features to appropriate .3cd clauses
  - Open questions on what the separate FEC sublayer does for this feature
    - External FEC sublayer with legacy ASIC hard to support, since host is by definition done
    - Extender sublayer may still be interesting for future PMDs or transport handoff
  - Need a place to put the LD/RD bits in the alignment markers
    - 3 bits total – LD, RD, and a bit allowing for future expansion

100GbE in-band LD/RD bits

- Can use last 3 bits of existing 5 bit pad
- Assuming no clock content issues as we did in .3bs

NG 100GbE - Alignment Marker mapping to FEC lanes

FEC Lane	Reed-Solomon symbol index, k (10-bit symbols)																							
	0	1	2	3	4	5	6	7	8	9	10	11	12			25	26	27	28	29	30	31	32	33
Lane 0	amp_tx_0						amp_tx_4									amp_tx_16								
Lane 1	amp_tx_1						amp_tx_5									amp_tx_17								
Lane 2	amp_tx_2						amp_tx_6									amp_tx_18								
Lane 3	amp_tx_3						amp_tx_7									amp_tx_19								

5 bit pad

tx_scrambled

start of FEC codeword

5 x 257-bit alignment marker block (including 5 bit pad)
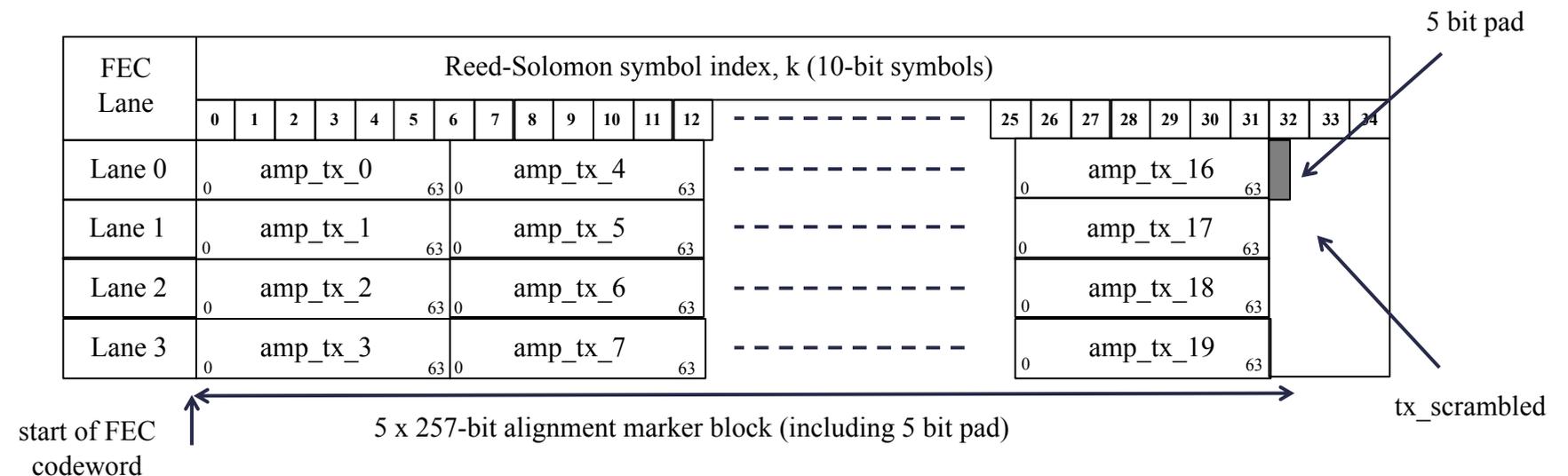
- Based on Clause 91. Exact AM mapping still TBD
- Initial analysis indicates that Clause 91 AM mapping needs to be modified to avoid clock content issues with repeating AM0 and AM16 patterns when bit muxing FEC lanes.

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From nicholl_3cd_01_0716.pdf

50GbE in-band LD/RD bits

- Not enough pad bits to make things easy

- BIP is not useful with FEC

  - Should we harvest BIP bits?

  - If so- which ones?

50GbE - Alignment Marker mapping to FEC lane
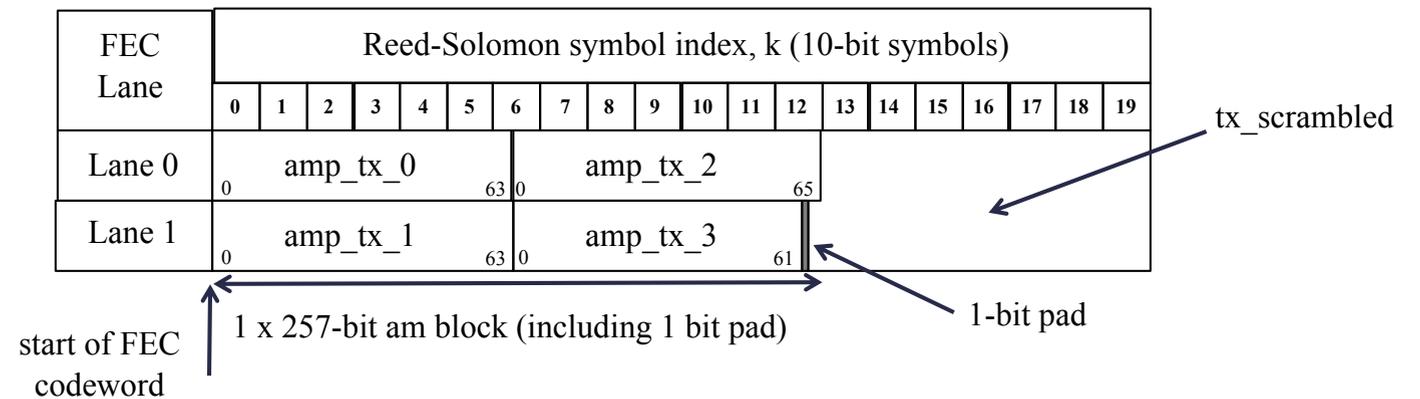
- Based on Clause 91 mapping, but modified to support 4 PCS lanes, 2 FEC lanes and to enable bit muxing of FEC lanes

- Exact AM mapping still TBD

- Note: amp_tx_0, amp_tx_1 =64 bits, amp_tx_2=66 bits, amp_tx_3=62 bit

From nicholl_3cd_01_0716.pdf

Summary

- Proposed adding the PreFEC BER feature from .3bs to .3cd
  - Most details should be easily ported
  - Questions about impact of separate FEC layer and if we need/want an extender sublayer.
  - Signaling bits
    - 100GbE has a natural place for the new signaling bits
    - Some work needed to find signaling bits for 50GbE

Thanks