PCS Consideration for 50GE & NG100GbE

Tongtong Wang, Xinyuan Wang

HUAWEI TECHNOLOGIES CO., LTD.

IEEE 802.3cd 50G&NGOATH Study Group

HUAWEI

Background and Introduction

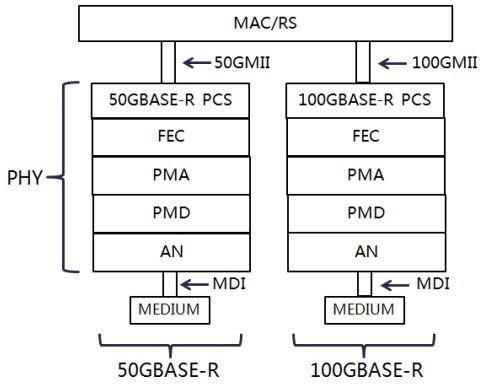
- Supporting 25Gbps IO in IEEE 50GbE and NG100GbE project will benefit industry with early product and lower cost in near term.
  - *wang_50GE_NGOATH_01_0316*
  - *ghiasi_50GE_NGOATH_02_0316*
  - Preference to include 25G class IO in 50GE and NG100GE project is expressed in many offline discussion.
- Latest baseline proposal satisfies this requirement and enables versatile use cases, supporting legacy and new port in ASICs
- This contribution further explore PCS/FEC architecture with assumption of 25G FEC lanes in 50GbE and NG100GbE and bit mux in PMA layer.

PCS/FEC Baseline Proposal

- In “nicholl_3cd_01_0716.pdf” , proposal of 50GbE/NG 100GbE PCS/FEC baseline have the following description:

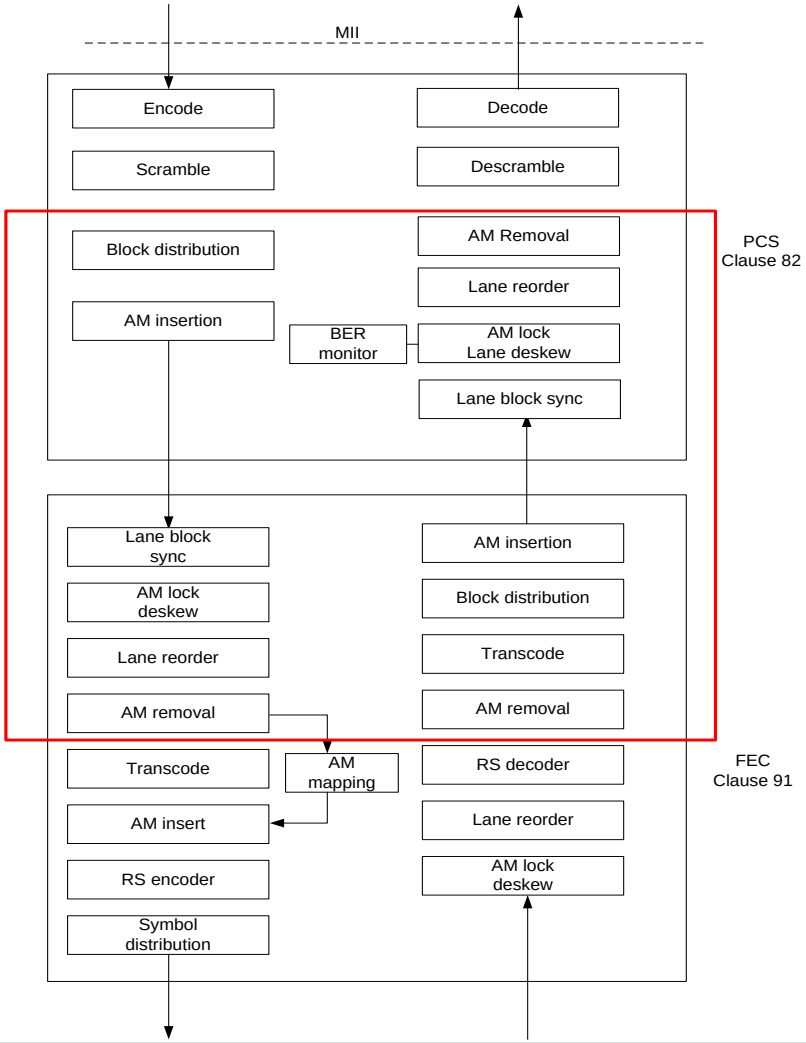
  Architecture Overview

  - Based on 802.3ba system architecture
  - Separate PCS and FEC sub layers
  - FEC is mandatory
  - PCS and FEC can be separated by an optional AUI
  - FEC can be carried over either a 25Gb/s or 50Gb/s per lane optional AUI
  - Bit-muxing PMA



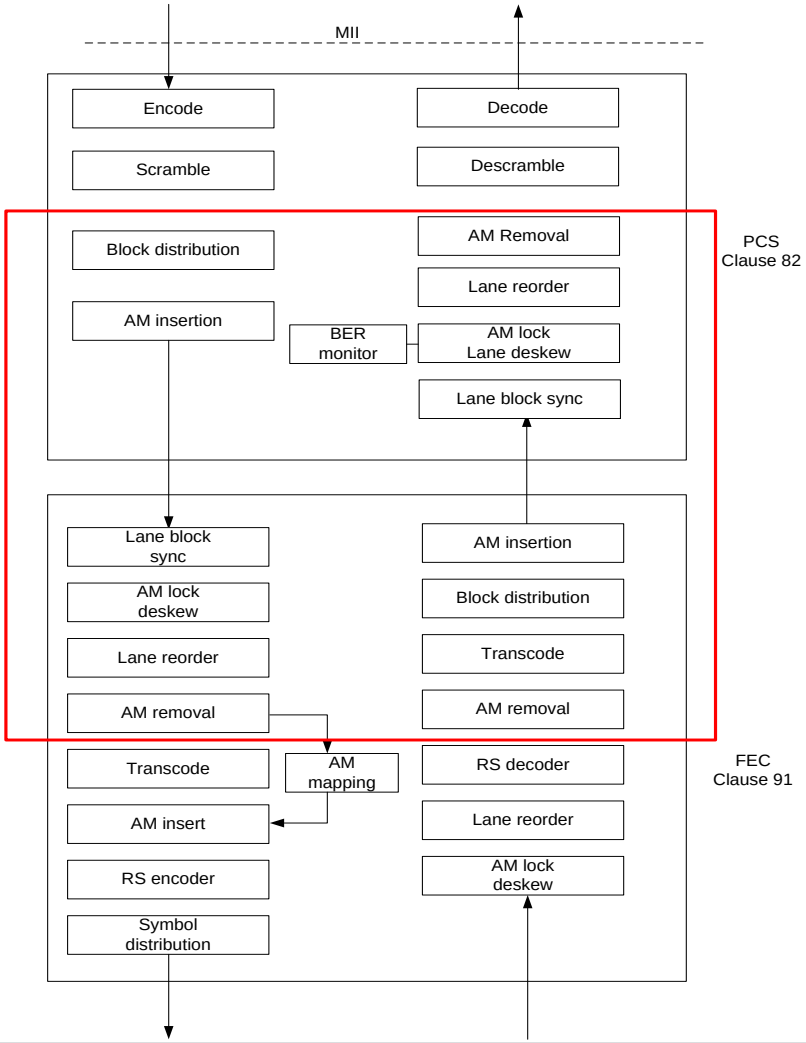
- PCS/FEC layers can be integrated or separate in different use cases. Suggest to clarify that part of PCS function is optional when PCS and FEC layers are integrated in future host ASIC.

Redundant PCS Functions in Integrated PCS/FEC Use Case



- Reusing clause 82 PCS and clause 91 FEC, function blocks in red block are not in use and will bring more latency and complexity in PCS/FEC integrated ASICs.
  - PCS lane distribution
  - AM insertion on PCS lanes
  - PCS Lane lock and deskew
  - PCS lane reorder
  - AM removal on PCS lanes
  - And reverse operations in RX path

Redundant PCS Functions in Integrated PCS/FEC Use Case



- Optimal solution in PCS/FEC integrated solution prefer to skip these function blocks.
- But MDIO registers or configurations on redundant blocks will be invalid or misleading.

Potential Changes in PICS

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	40GBASE-R Block Lock	82.2.19.3	Implements 4 block lock processes as depicted in Figure 82–12	PCS40:M	Yes [ ] No [ ]
SM2	100GBASE-R Block Lock	82.2.19.3	Implements 20 block lock processes as depicted in Figure 82–12	PCS100:M	Yes [ ] No [ ]
SM3	The SLIP function evaluates all possible bit positions	82.2.19.2.3		M	Yes [ ] No [ ]

82.7.4.4 Alignment Markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	82.2.7	Alignment markers are inserted periodically as described in section 82.2.7	M	Yes [ ] No [ ]
AM2	Alig				
AM3	Lan				

91.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	91.5.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps	M	Yes [ ]
TF2	Lane reorder	91.5.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]

SM10	100GBASI				
SM11	40GBASE-		Figure 82–16		No [ ]
SM12	100GBASE-R Transmit process	82.2.19.3	Meets the requirements of Figure 82–16	PCS100:M	Yes [ ] No [ ]
SM13	40GBASE-R and 100GBASE-R Receive process	82.2.19.3	Meets the requirements of Figure 82–17	PCS40:M	Yes [ ] No [ ]
SM14	100GBASE-R Receive process	82.2.19.3	Meets the requirements of Figure 82–17	PCS100:M	Yes [ ] No [ ]

- Suggest to change some requirement in conformance statement to relax implementation limitation

Summary

- Suggest not to enforce mandatory implementation of some redundant PCS/FEC functions to enable optimal integrated PCS/FEC solution with lower latency and benefit user applications.

- Suggest to clarify mandatory and optional part of PCS layer to help consistency between optimal implementation and standard text.

Thank you