Proposal For Die Level PMD Specification

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IEEE 802.3 50 Gb/s, 100 Gb/s, and 200 Gb/s Ethernet Task Force
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Supporters

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- Yasuo Hidaka, Fujitsu
- Erdem Matoglu, Amphenol-TCS
- Jim Nadolny, Samtec
- Rick Rabinovich, IXIA
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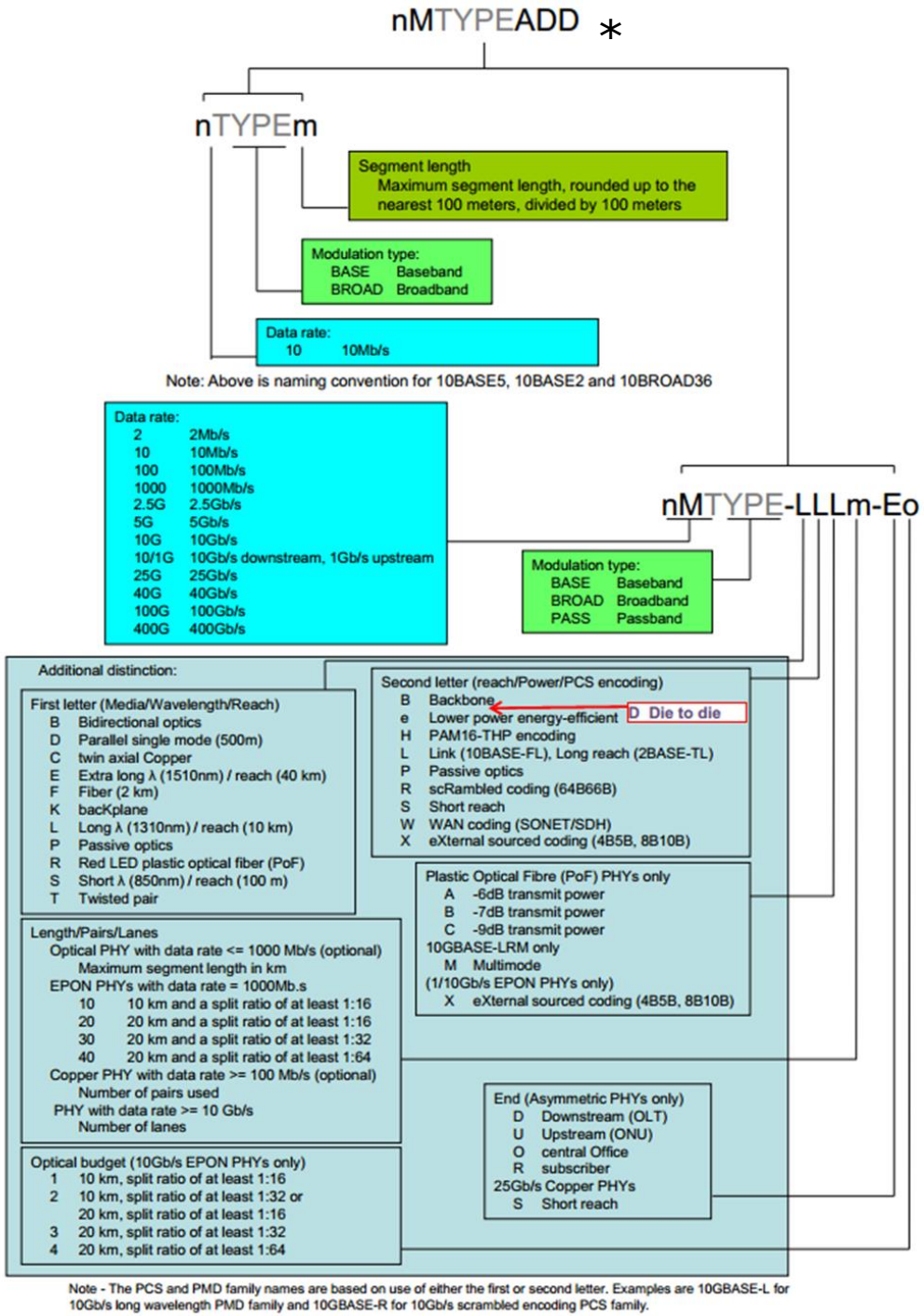
- Andrew Zambell, FCI

Presentation Purpose

- Expand the Ethernet stack to embrace systems build up from Ethernet IP die level components.
- Not to tear down all the previous IEEE802.3 work, but to build upon it. Keep KR and CR.

Market Proposition and Limitations

- Packages are a large chunk of the channel operating margin (COM).
  - For example the channel, PAM4_2conn_MP_v2_85ohm_30dB_Nom_thru, has a COM or 1.26 dB for package 2, 2.48 dB for package 1, and 3.3 dB with no package.
- Recouping 2dB of COM margin or asymmetric budgets are attractive.
- Pin level specification is challenged because of parallel market requirements for
  - large and small chips
  - high and low volume manufacturing
- Many companies have broad portfolios of IP.
  - Some system implementers would benefit for Ethernet compliant IP leaving the entire interconnect up to them
- The proposal is to keep the pin level PMD specification but add another PMD specification at the die.



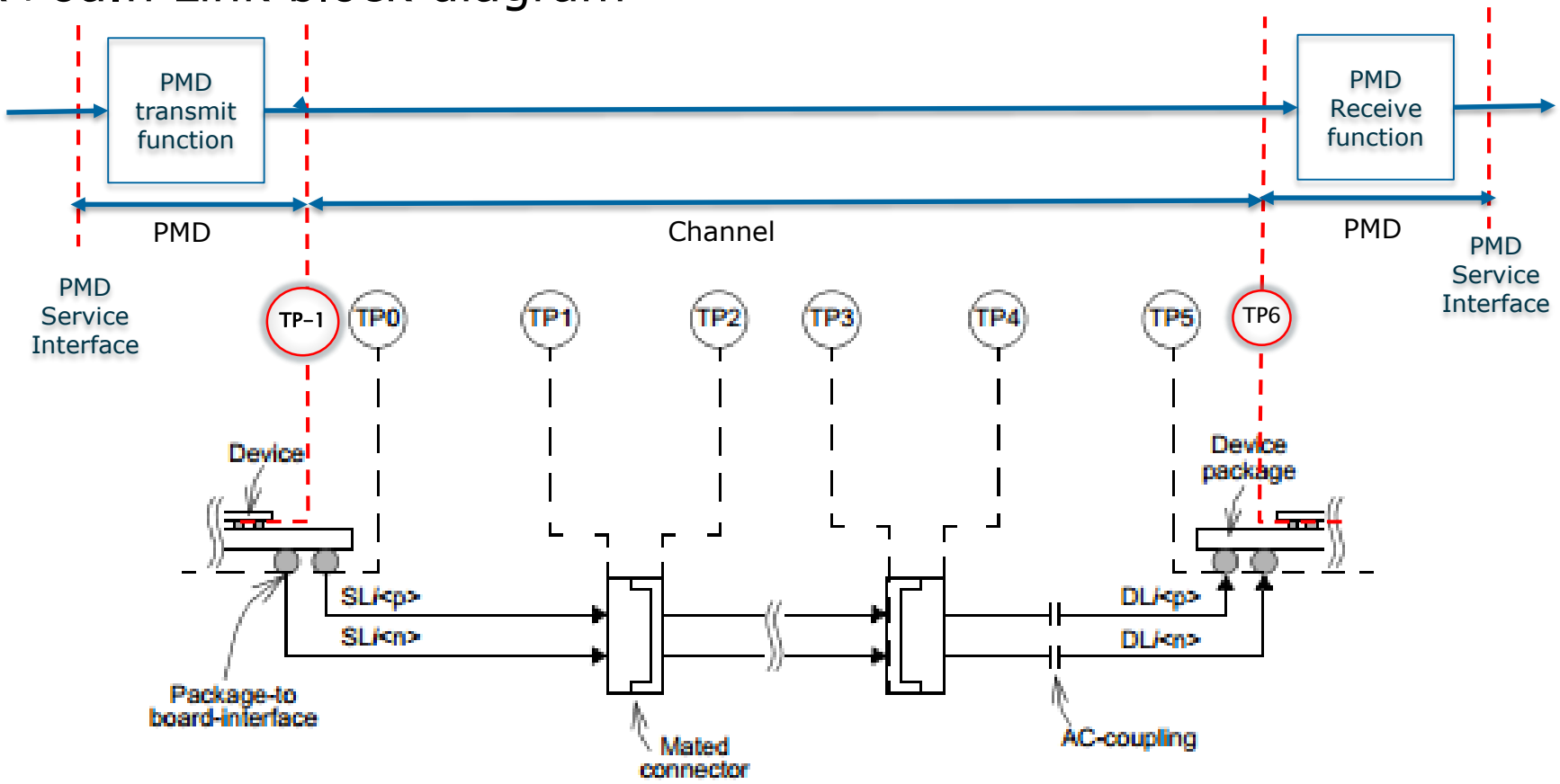
KD is another PMD
i.e. backplane die to die

*http://www.ieee802.org/3/cb/public/jan16/PHY_names_1115.pdf

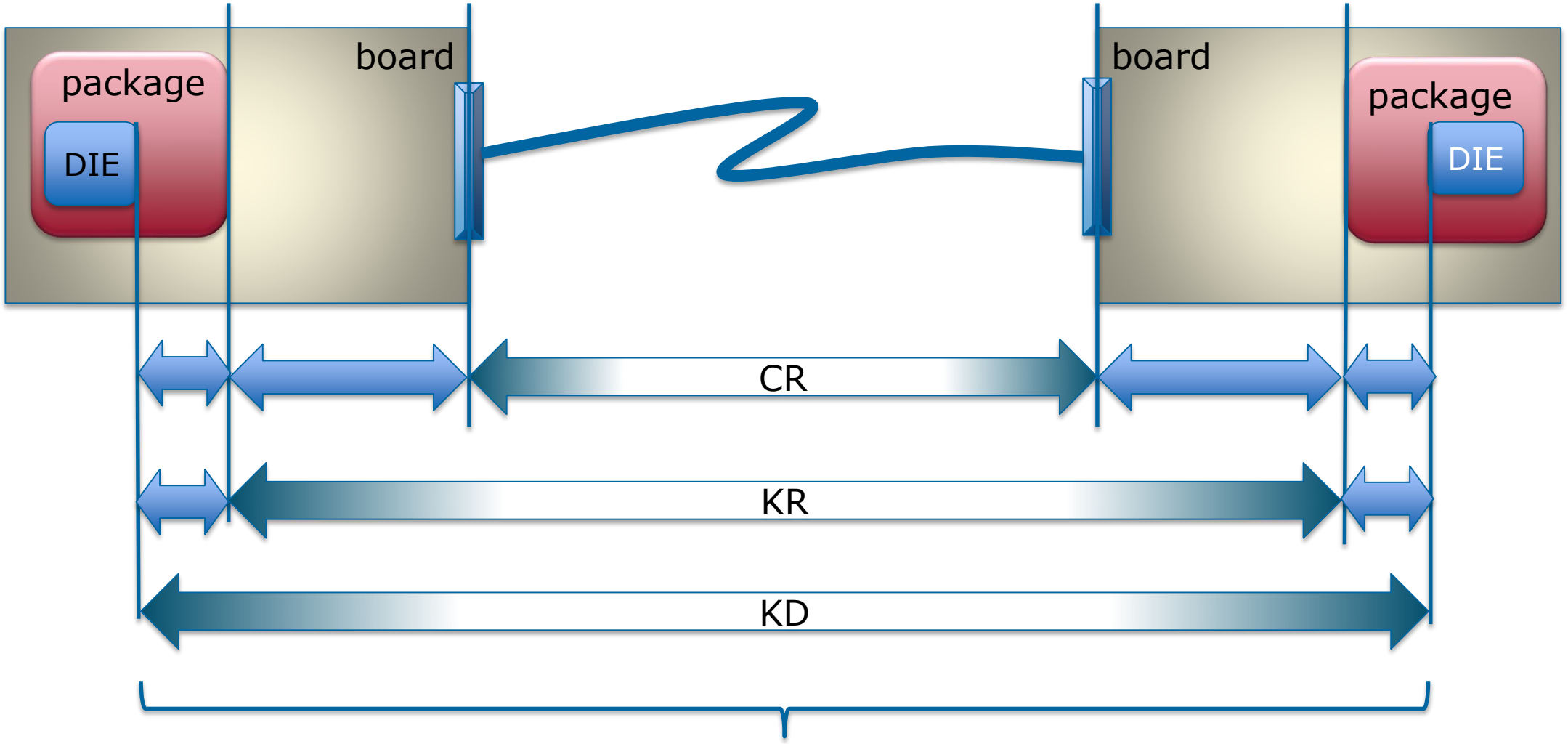
Add a PMD Annex for 50GBASE-KD operation with test points at the die pad.

- X+6.n PMD functional specifications

X+6a.n Link block diagram



Keep KR and CR: Add base capability KD



Same COM and loss budget but different amount of added interconnect

Transmitter test fixture (same electrical specs)

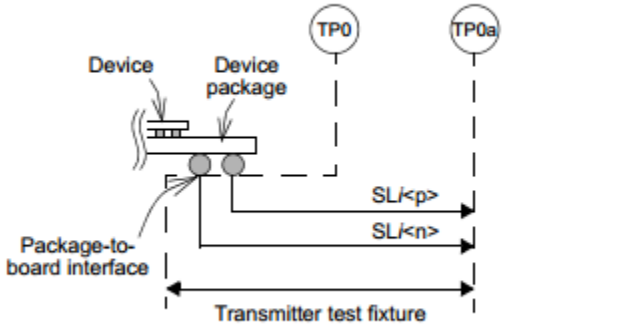
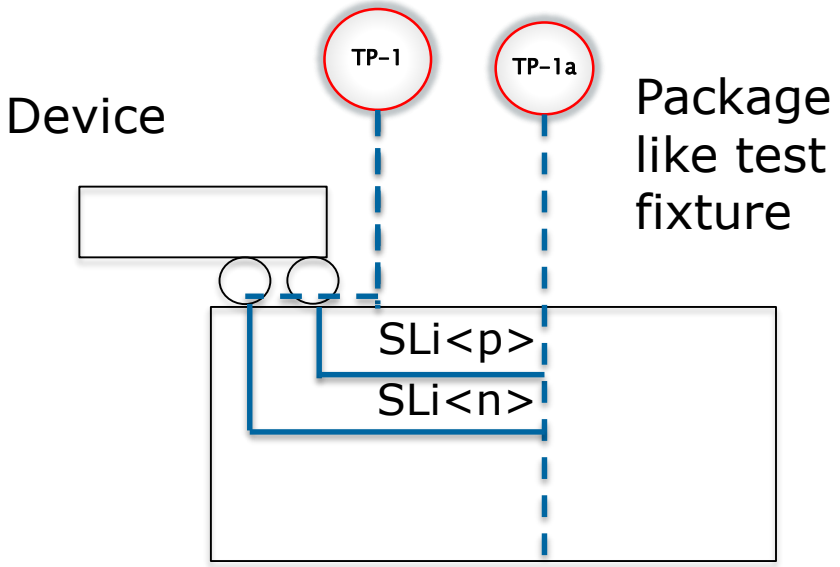


Figure 93–5—Transmitter test fixture and test points



Adapt KR transmitter parameters to reflect RL at die.

93.8.1.4 Transmitter output return loss

The differential output return loss, in dB, of the transmitter shall meet Equation (93–3) where f is the frequency in GHz. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ω

$$RL_d(f) \geq \begin{cases} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 19 \end{cases} \text{ dB} \qquad (93\text{–}3)$$

The differential return loss limit is illustrated by Figure 93–7.

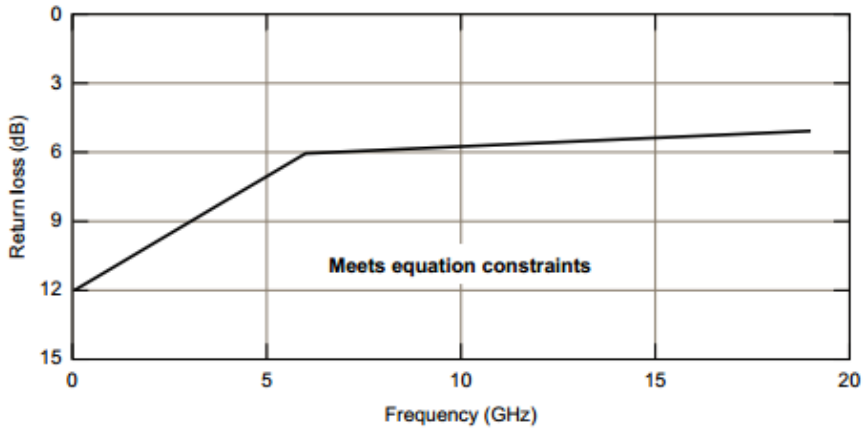
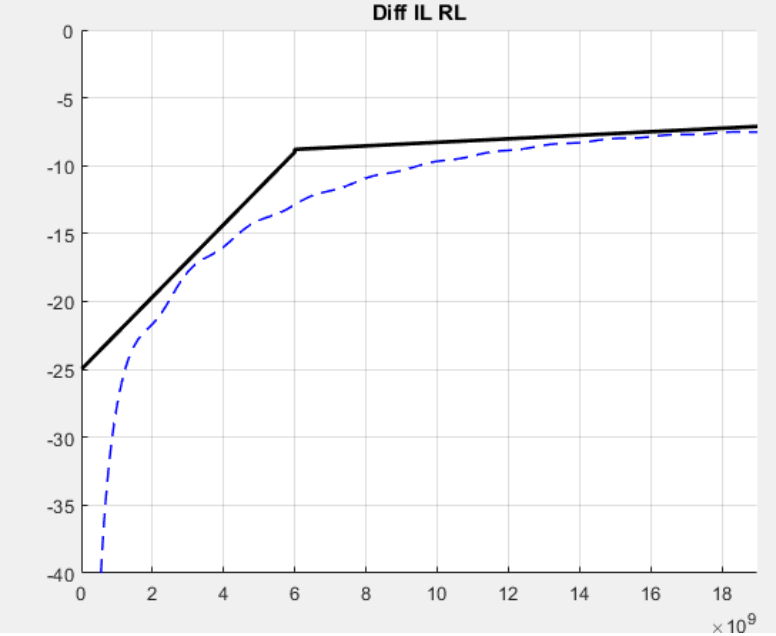


Figure 93–7—Differential return loss limit

The common-mode output return loss, in dB, of the transmitter shall meet Equation (93–4) where f is the frequency in GHz. This output impedance requirement applies to all valid output levels. The reference impedance for common-mode return loss measurements shall be 25 Ω

$$RL_d(f) \geq \begin{cases} 25 - 2.667f & 0.5 \leq f \leq 6 \\ 9.5773 - 0.13f & 6 < f \leq 19 \end{cases} dB$$



Adapt KR Transmitter Fit Parameters

93.8.1 Transmitter characteristics

Transmitter characteristics measured at TP0a are summarized in Table 93–4.

Table 93–4—Summary of transmitter characteristics at TP0a

Parameter	Subclause reference	Value	Units
Signaling rate	93.8.1.2	25.78125±100 ppm	GBd
Differential peak-to-peak output voltage (max.) Transmitter disabled Transmitter enabled	93.8.1.3	 30 1200	 mV mV
DC common-mode output voltage (max.)	93.8.1.3	1.9	V
DC common-mode output voltage (min.)	93.8.1.3	0	V
AC common-mode output voltage (RMS, max.)	93.8.1.3	12	mV
Differential output return loss (min.)	93.8.1.4	Equation (93–3)	dB
Common-mode output return loss (min.)	93.8.1.4	Equation (93–4)	dB
Output waveform Steady-state voltage v_f (max.) Steady-state voltage v_f (min.) Linear fit pulse peak (min.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	 93.8.1.5.2 93.8.1.5.2 93.8.1.5.2 93.8.1.5.4 93.8.1.5.4 93.8.1.5.5 93.8.1.5.5	 0.6 0.4 0.71 × v_f 0.0083 0.05 1.54 4	 V V V — — — —
Signal-to-noise-and-distortion ratio (min.)	93.8.1.6	27	dB
Output jitter (max.) Even-odd jitter Effective bounded uncorrelated jitter, peak-to-peak Effective total uncorrelated jitter, peak-to-peak	93.8.1.7	 0.035 0.1 0.18	 UI UI UI

26.5625 +/-100ppm

0.905xv$_f$

32.32dB (starting with 31db and 4 mV for package crosstalk

Change receiver test fixture diagram

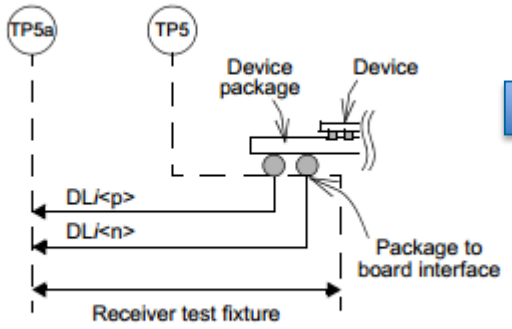
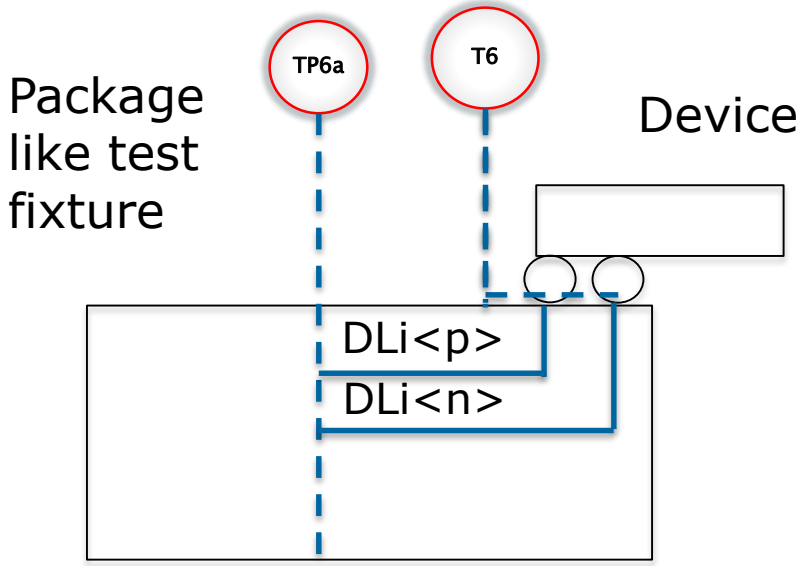


Figure 93–10—Receiver test fixture and test points



Adapt KR Transmitter Reviever Parameters

13.28125 GHZ

Table 111–4—25GBASE-KR interference tolerance parameters, RS-FEC mode

Parameter	Test 1 (low loss)		Test 2 (high loss)		Units
	Min	Max	Min	Max	
Insertion loss at 12.89 GHz[a]	—	30	35	—	dB
Fitted insertion loss coefficients[b]					
a_0	−0.9	0.9	−0.9	0.9	dB
a_1	0	3.3	0	3.3	dB/GHz$^{1/2}$
a_2	0	—	0	—	dB/GHz
a_4	0	0.03	0	0.043	dB/GHz^2
COM	—	3	—	3	dB
Test pattern	Scrambled idle encoded by RS-FEC				
RS-FEC symbol error ratio required[c]	$< 10^{-4}$				
b_{max} used in COM calculation	1				
DER_0 used in COM calculation	10^{-5}				

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C–4) using the method in 93A.3 with f_{min}=0.05 GHz, f_{max}=25.78125 GHz, and maximum Δf=0.01 GHz.
[c]The RS-FEC symbol error ratio is measured using the RS-FEC symbol error counter (see 108.6.9).

16 dB

35.4 dB = 30 +
2.7dB*2 for package

TPt to
TP6

93C modifications

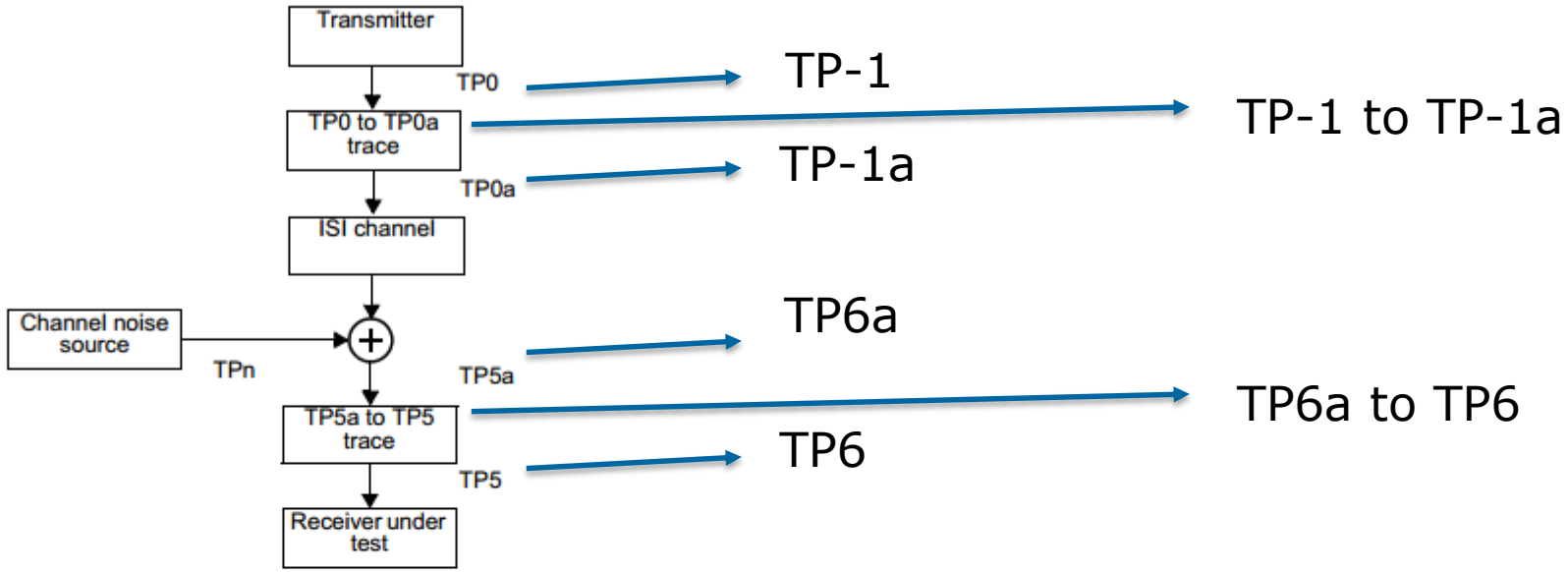


Figure 93C–2—Interference tolerance test setup

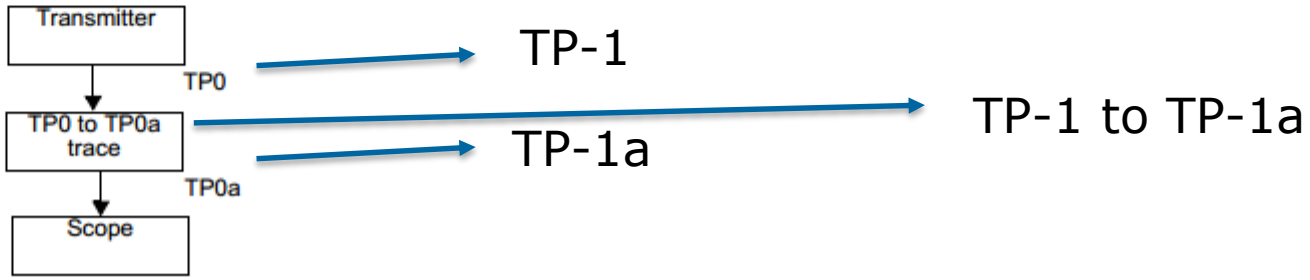


Figure 93C–3—Interference tolerance transmitter test setup

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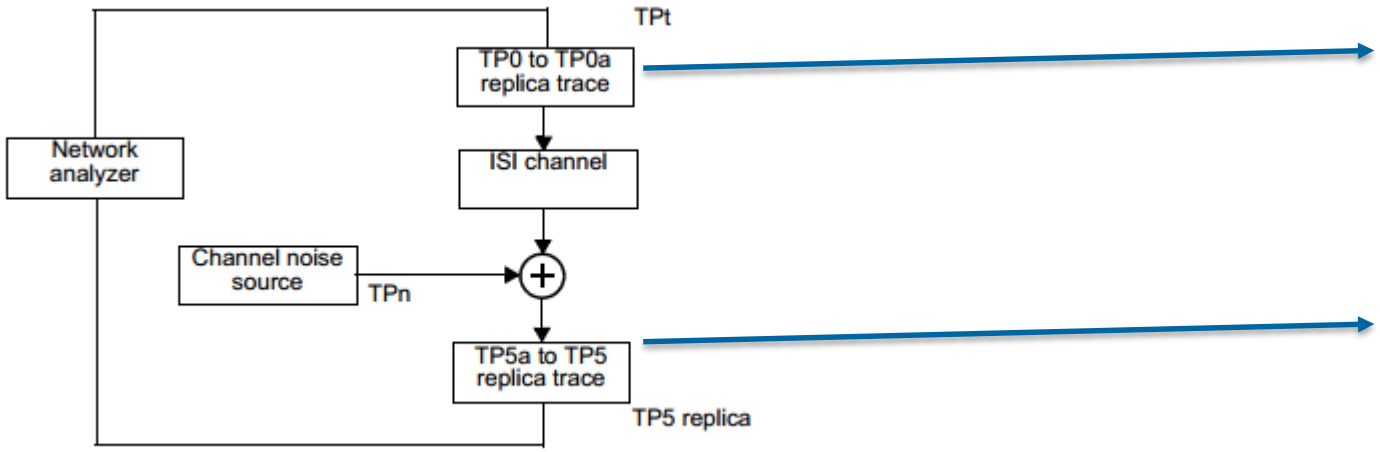
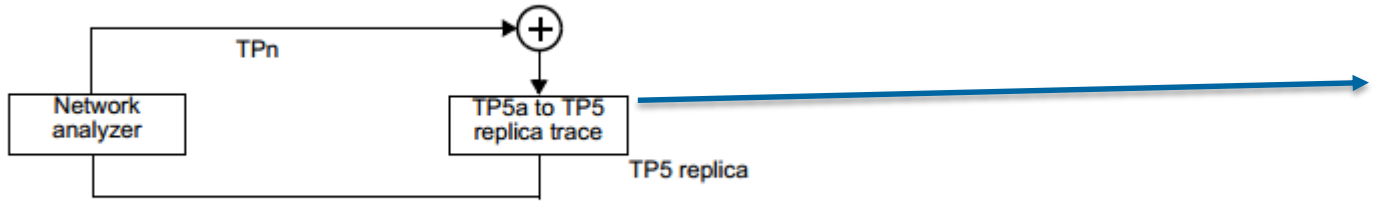
More 93C N modifications



TP-1 to TP-1a

TP6a to TP6

Figure 93C–4—Interference tolerance channel s-parameter test setup

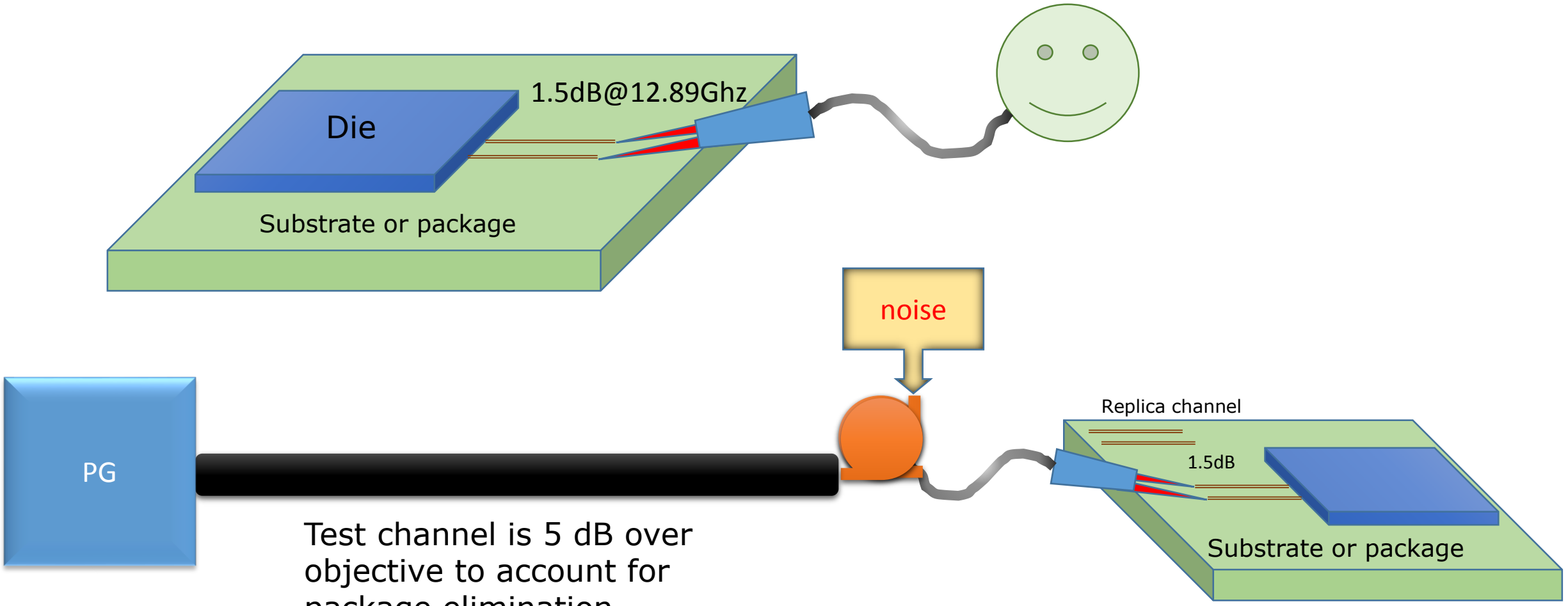


TP6a to TP6

Figure 93C–5—Interference tolerance channel noise path test setup

Test fixture is a substrate or package

*Tx and Rx compliance test is similar to KR for '*by



Test channel is 5 dB over objective to account for package elimination

Potential COM table

- This is only a starting point
- Contribution may change parameters

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	26.5625	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[2.8e-4 2.8e-4]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	0	mm	[test cases]
z_p (NEXT)	0	mm	[test cases]
z_p (FEXT)	0	mm	[test cases]
z_p (RX)	0	mm	[test cases]
C_p	0.00E+00	nF	[TX RX]
R_0	50	Ohm	
R_d	[55 55]	Ohm	[TX RX]
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.15:0.05:0]		[min:step:max]
c(-2)	[0:0.05:0.15]		
c(1)	[-0.35:0.05:0]		[min:step:max]
g_DC	[-15:1:0]	dB	[min:step:max]
f_z	10.625	GHz	
f_p1	10.625	GHz	
f_p2	1.00E+99	GHz	
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.65	V	
L	4		
M	32		
N_b	16	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	2.60E-08	V^2/GHz	
SNR_TX	32.32	dB	
R_LM	0.95		
DER_0	1.00E-04		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2

g_DC_HP	[-4:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

Summary

- Proposal is to add and ANNEX for a 50GBASE-KD PMD at the die
  - 100GBASE-KD2 and 200GBASE-KD4 as well