Open electrical issues

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My list of list of what needs to be done in 802.3bs before that project can be complete

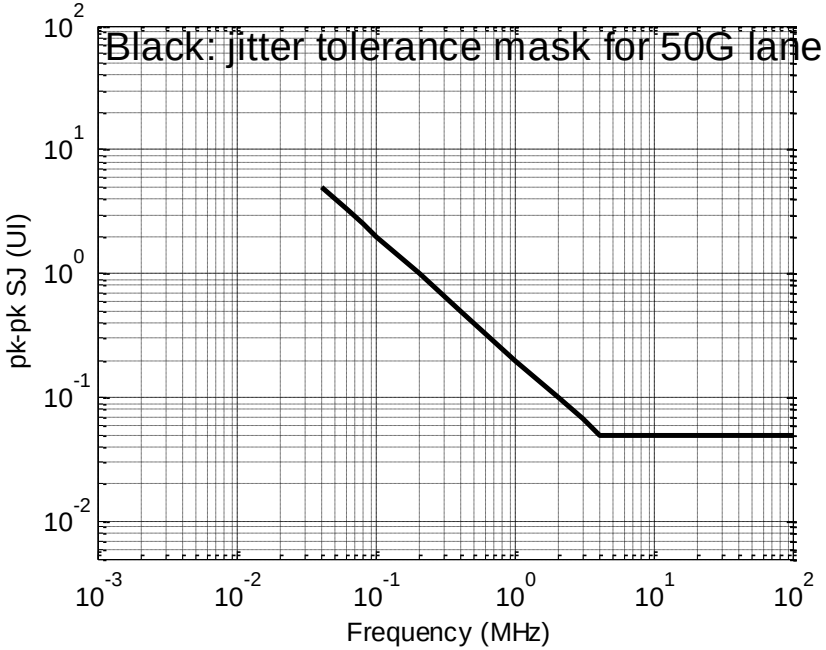
1. Jitter specs for 400GAUI-8 and 400GBASE-DR4 are not compatible

2. 400GAUI-8 C2C needs a channel RL spec to complement the RL spec it has (Clause 137 has a channel RL spec already)
3. 400GAUI-8 C2C test fixture RL is not compatible with tightened RL spec
4. 400GAUI-8 C2C RL is too tight at low frequencies
5. 400GAUI-8 C2C SNR_ISI limit is so tight that even test equipment appears borderline: not practical
6. Similar problem with SNDR
7. Change COM to use more corners, or one corner at neutral impedance?

8. 400GAUI-8 C2M precursor ratio spec is more restrictive than it should be
9. Exclude pathological big bad C2M host signals that no-one needs to make but this draft spec allows

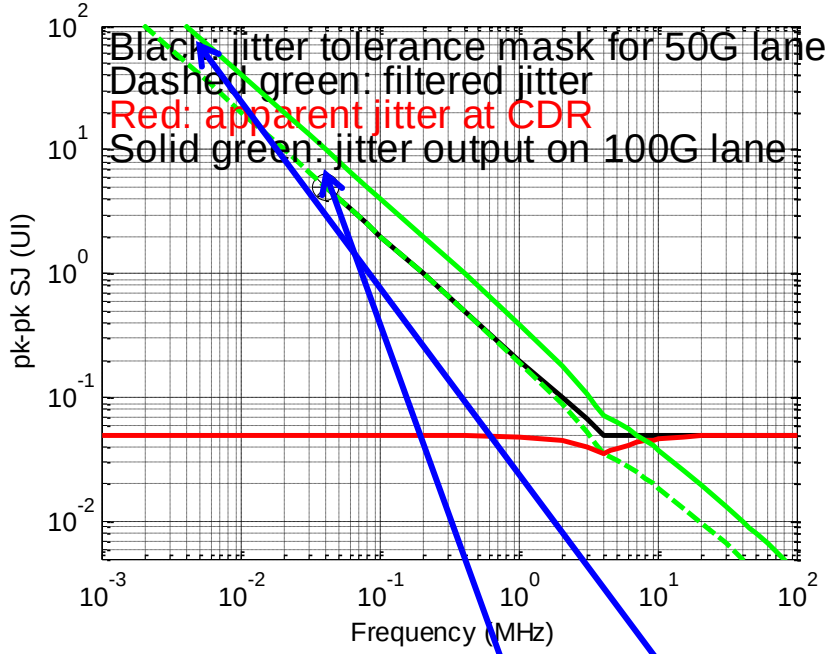
- Plus optical issues not listed here
- *What has to be added to this list?*

1. Jitter specs for 400GAUI-8 and 400GBASE-DR4 are not compatible



- Module with 400GAUI-8 electrical input, 400GBASE-DR4 optical output
- The module's electrical input can be tested at six SJ points on the mask on the left
- The host's output jitter must be near or below the (extrapolated?) mask
- This is also the jitter mask for the 100G optical lanes, but 1 UI is different there

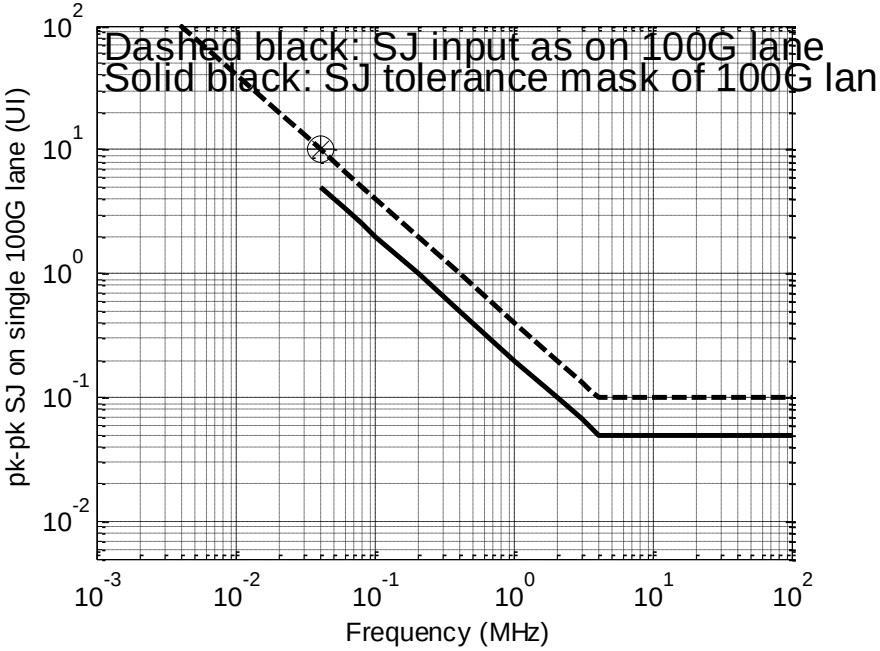
1. Jitter specs for 400GAUI-8 and 400GBASE-DR4 are not compatible



- Module with a conventional CDR (with minimum bandwidth) transfers jitter at low f (dashed green), blocks jitter at high f (electrical signal appears to the module to have the red jitter)
- 1 UI out (100G optical lane) is half as long as 1 UI in (50G electrical lane); the early or late bits from two lanes have to be sent out on one lane

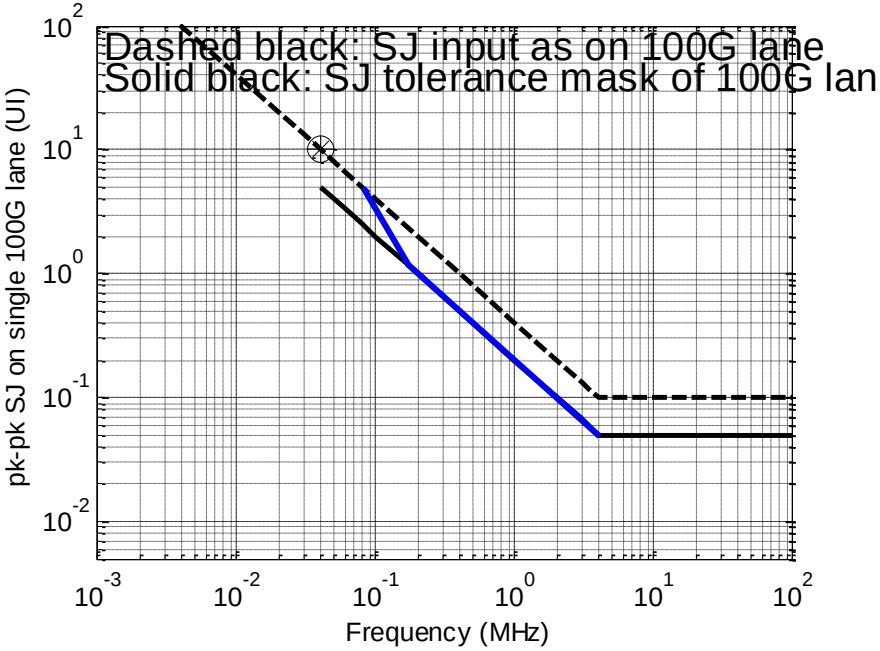
- So the jitter after the input CDR (solid green line) is twice what is allowed
  - with CDR bandwidth tolerance, even more
- Add a FIFO and a second PLL. This costs power and requires a low noise second PLL
- How large a FIFO? 5 UI / lane? 50 UI / lane? 500 UI / lane? More?
- The spec doesn't work

1. Jitter specs for 400GAUI-8 and 400GBASE-DR4 are not compatible



- The two lines are the wrong way round at low frequencies
- Need to make the solid line equal or higher than the dashed line at low frequencies
  - this was hinted in ghiasi_3bs_01a_0116
- There may be more than one way to do this

1. Jitter specs for 400GAUI-8 and 400GBASE-DR4 are not compatible

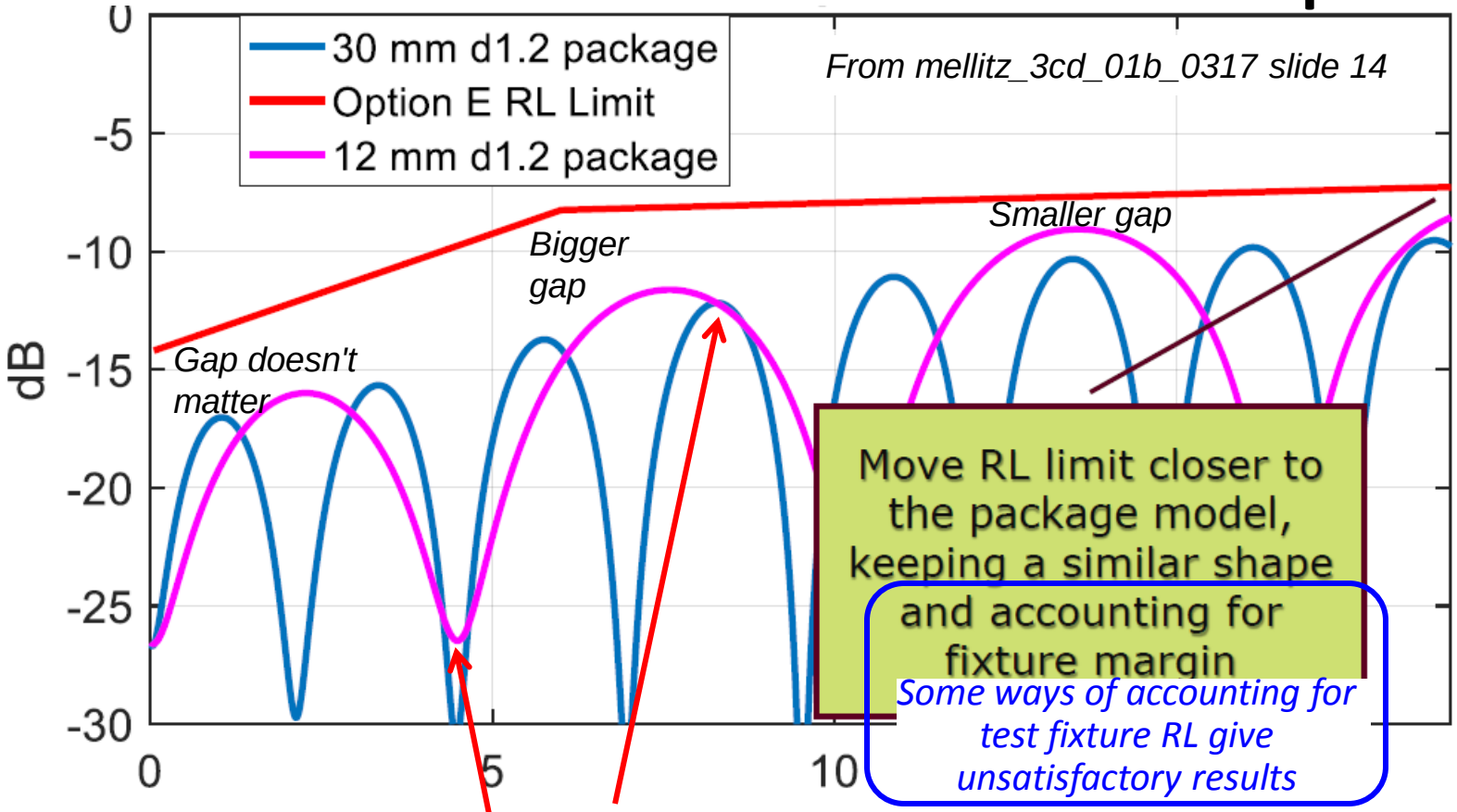


- One way would be to modify the 100G jitter tolerance mask and reference CRU as the blue line

2. C2C needs a channel RL spec
4. C2C RL is too tight at low frequencies

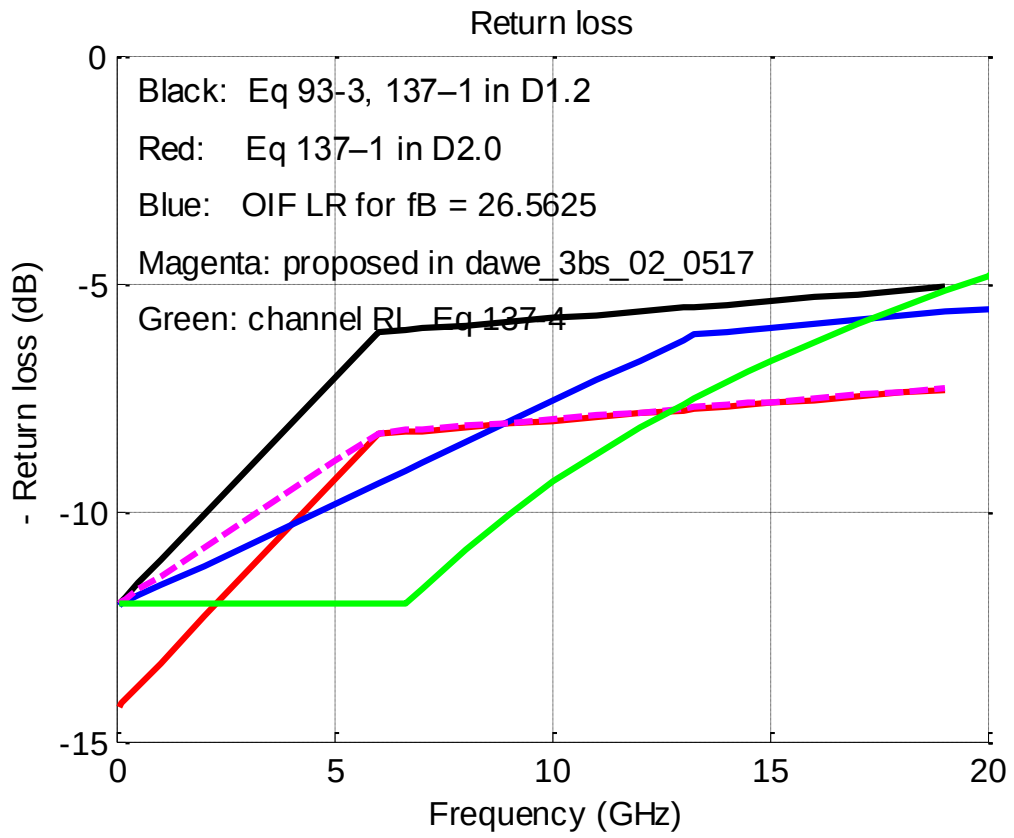
- For much the same reason we have a Tx return loss spec – to control echoes between e.g. Tx and channel that cause ISI that COM does not know about
  - See dawe_3bs_02_0517 for some initial calculations on this
  - It turns out that the end-to-end reflections are insignificant in comparison; except for channels with minimal loss, the channel insertion loss, which appears twice in an echo path, makes them much smaller than end-to-channel reflections.
    At very low frequencies they could have equal spectral density, but few hertz, and in practice at very low frequencies the channel RL is much better than -12 dB
- For practical RL limits, it seems that the 5-15 GHz range is the important area

2. C2C needs a channel RL spec



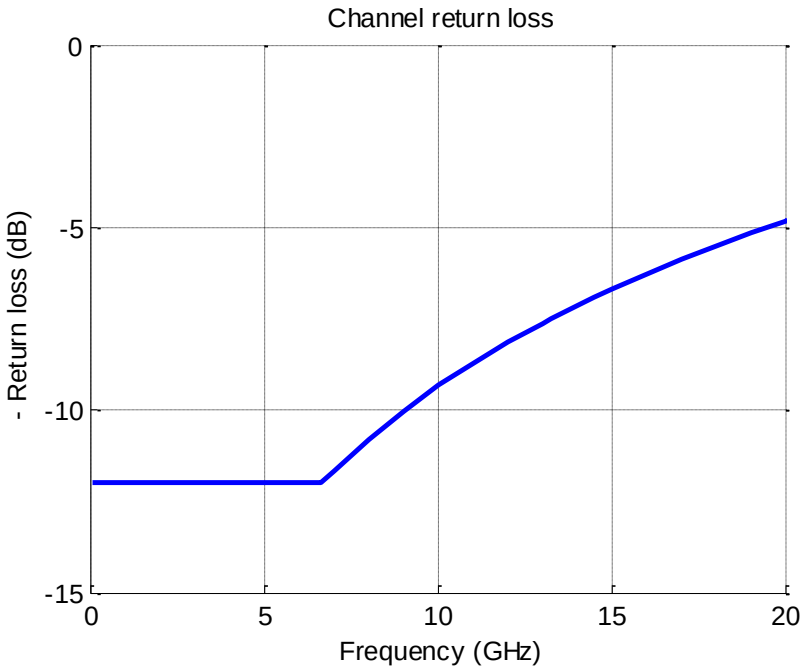
- A channel reflection at this frequency degrades that channel's long-package COM
  - as it should
- A channel reflection at this frequency is pretty much ignored by COM
  - gap in the spec
- We could add more COM package lengths, but...
- A channel RL spec is useful because it treats reflections consistently with frequency

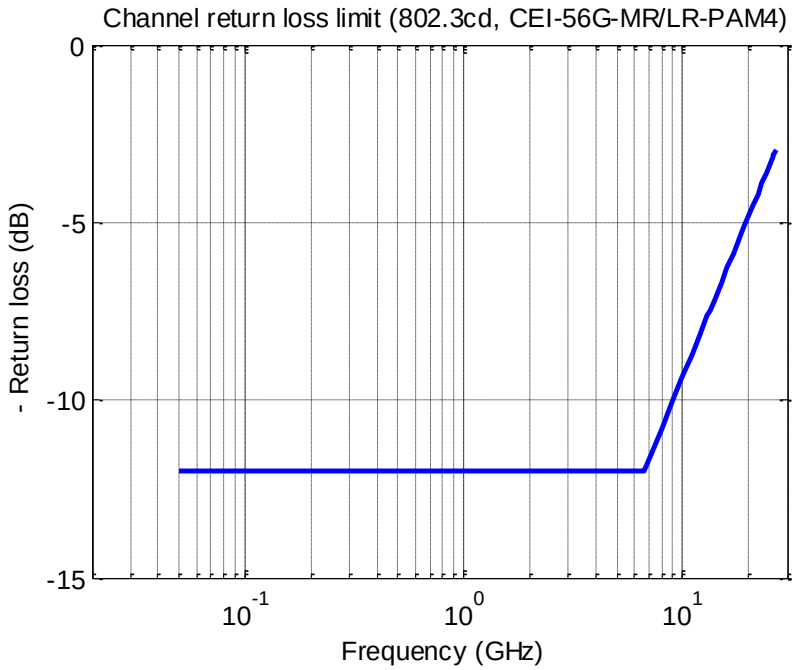
Showing the Clause 137 channel return loss limit



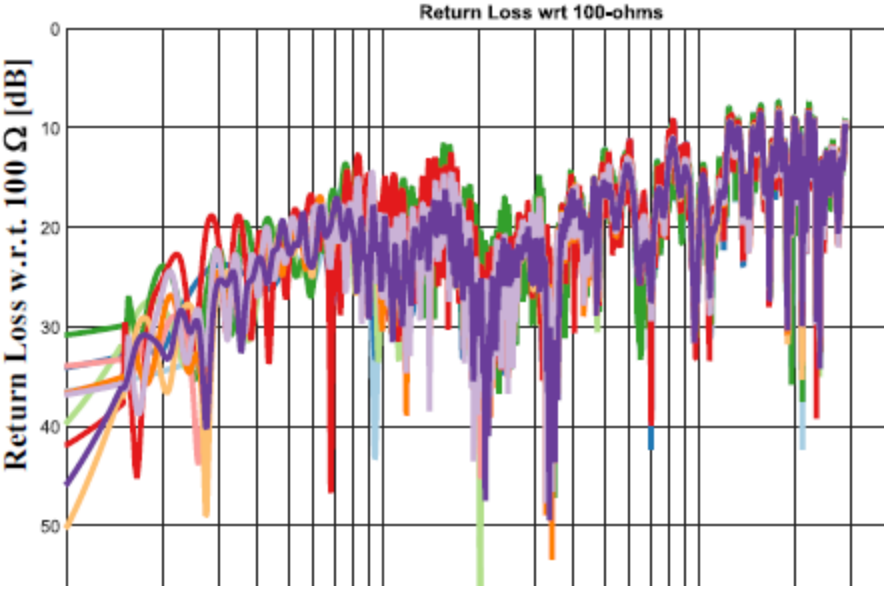
- Channels have lower return loss than this at very low frequencies – but that doesn't mean we need to adjust the spec there
- Should any C2C channel RL spec be the same as Cl. 137 -KRn?
- Should it apply to all channels, or e.g. only if COM < 4 or 5 dB?

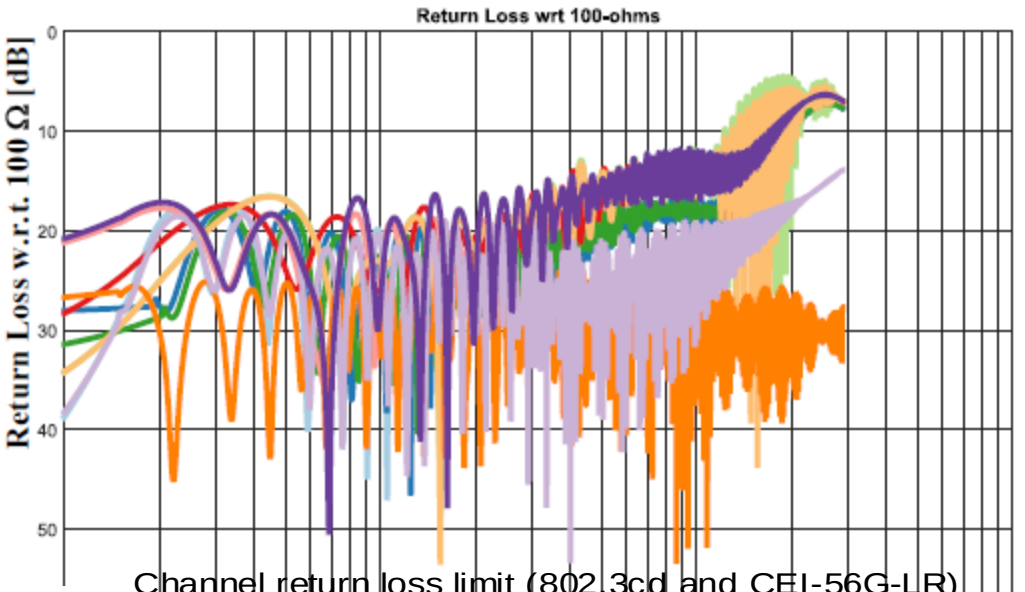
Channel return loss

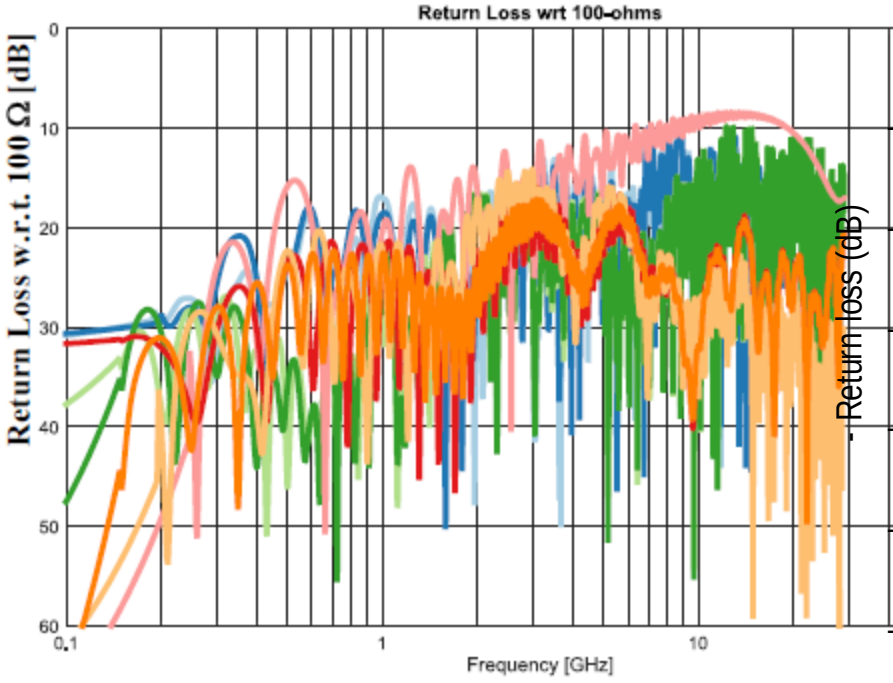




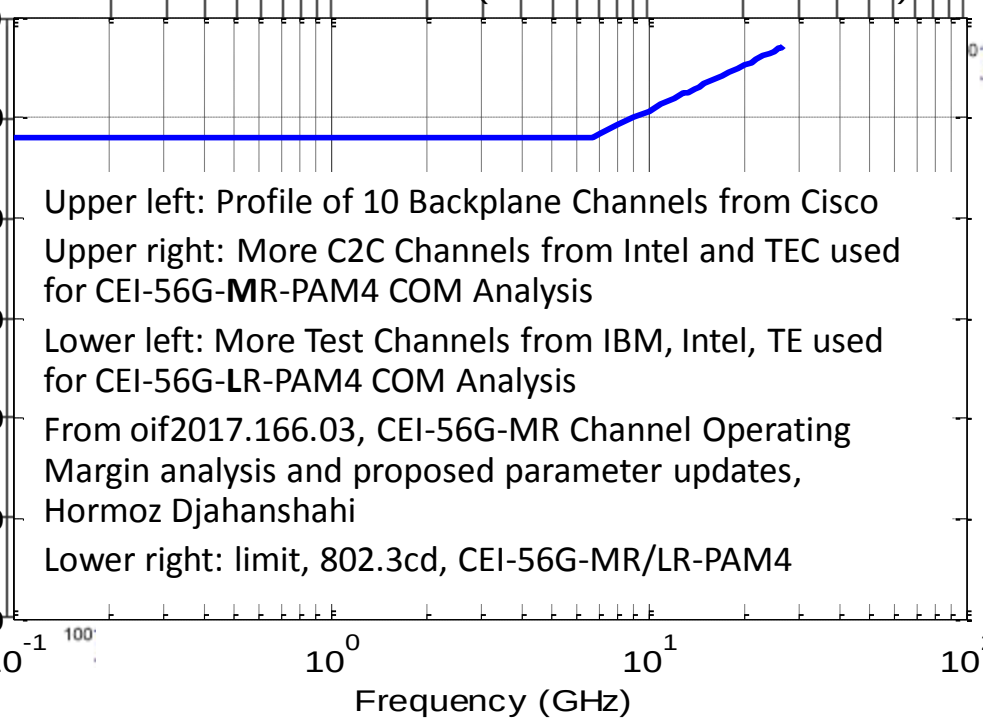
- Channel return loss (at TP0 or TP5) from 802.3cd Eq. 137-4 and OIF
- CEI-56G-MR-PAM4 Eq 17-3 and LR-PAM4 Eq 21-3 *(but not C2C)*
- *C2C needs a channel RL spec, otherwise the Tx RL spec is not very useful*







Channel return loss limit (802.3cd and CEI-56G-LR)



Upper left: Profile of 10 Backplane Channels from Cisco

Upper right: More C2C Channels from Intel and TEC used for CEI-56G-**M**R-PAM4 COM Analysis

Lower left: More Test Channels from IBM, Intel, TE used for CEI-56G-**L**R-PAM4 COM Analysis

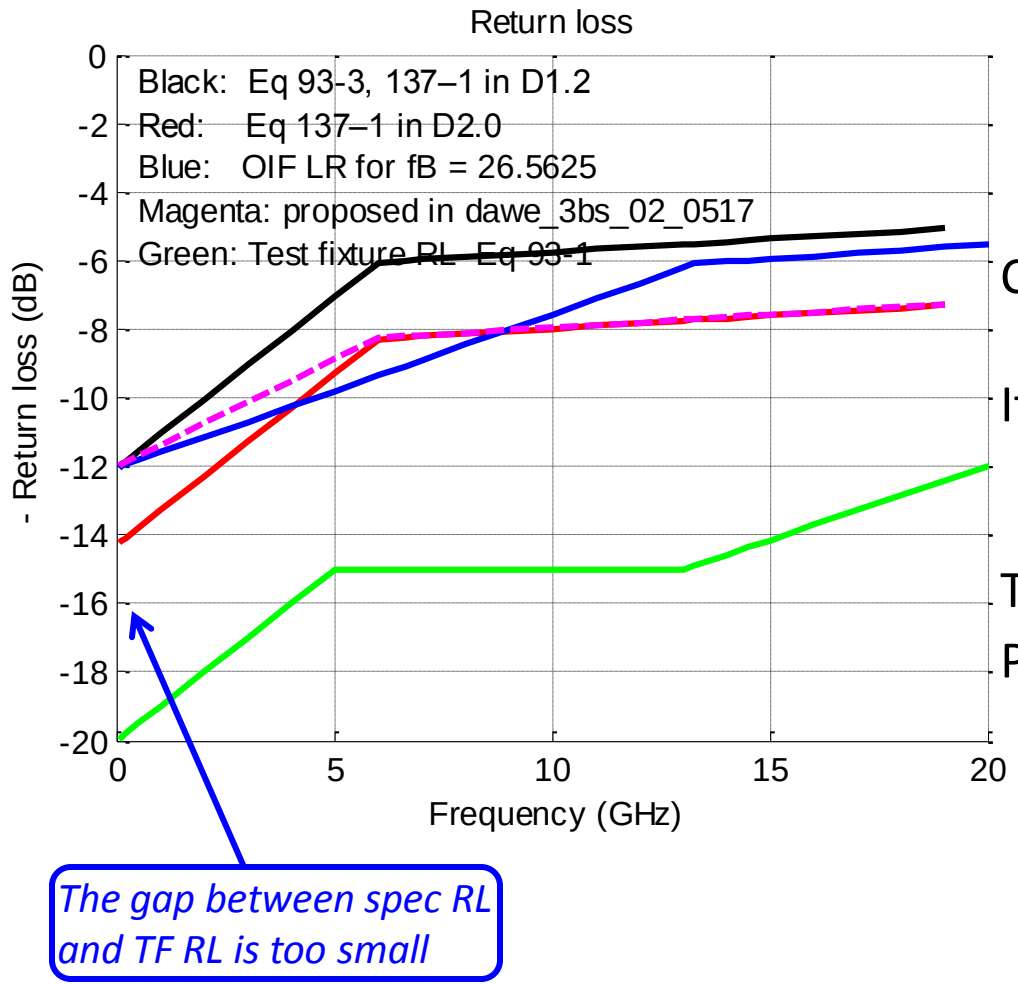
From oif2017.166.03, CEI-56G-MR Channel Operating Margin analysis and proposed parameter updates, Hormoz Djahanshahi

Lower right: limit, 802.3cd, CEI-56G-MR/LR-PAM4

Test points and test fixtures

- 802.3bs C2C, 802.3cd -KRn, and OIF CEI-56G-MR-PAM4 and CEI-56G-LR-PAM4 define the channel insertion loss from package ball to package ball (TP0 to TP5)
- Two of them have channel return loss limits, to same test points
- 802.3bs C2C and 802.3cd -KRn specify return loss of transmitter or receiver as observed through a test fixture: at TP0a and Tp5a
  - This test fixture has specified insertion and return loss
  - It is not the same as a C2M compliance board

3. Backplane/C2C test fixture RL



- If the apparent RL is given by the red line, and the test fixture has allowed reflections per green line, the IC on the test fixture has to be much better than intended
- Changing from black to red made this issue worse
- It's the difference in V/V that matters, not in dB, so the problem is worst at low frequencies
- The test fixture also has insertion loss
- Per 93.8.1.1, "The effects of differences between the insertion loss of an actual test fixture and the reference **insertion** loss are to be accounted for in the measurements"
- De-embed the return loss differences too, or tighten the TF RL spec?