50 Gb/s Ethernet over a Single Lane and Next Generation 100 Gb/s and 200 Gb/s Ethernet Study Groups Considerations for Cable Assembly, Test Fixture and Channel Specifications

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Purpose

•Considerations for 50 Gb/s cable assembly, test fixture and channel specifications consistent with adopted objectives

– Define single-lane 50 Gb/s PHYs for operation
  - copper twinaxial cables.
  - printed circuit board backplane.
  - MMF with lengths up to at least 100m.
  - SMF with lengths up to at least 2km.
  - SMF with lengths up to at least10km

–Define single-lane 200 Gb/s PHYs for operation
  - copper twinaxial cables.
  - printed circuit board backplane.
  - MMF with lengths up to at least 100m.

–Provide physical layer specifications which support 200 Gb/s operation over
  - At least 2 km SMF
  - At least 2 km SMF

– Define a two lane 100 Gb/s PHY for operation over copper twinaxial cables.

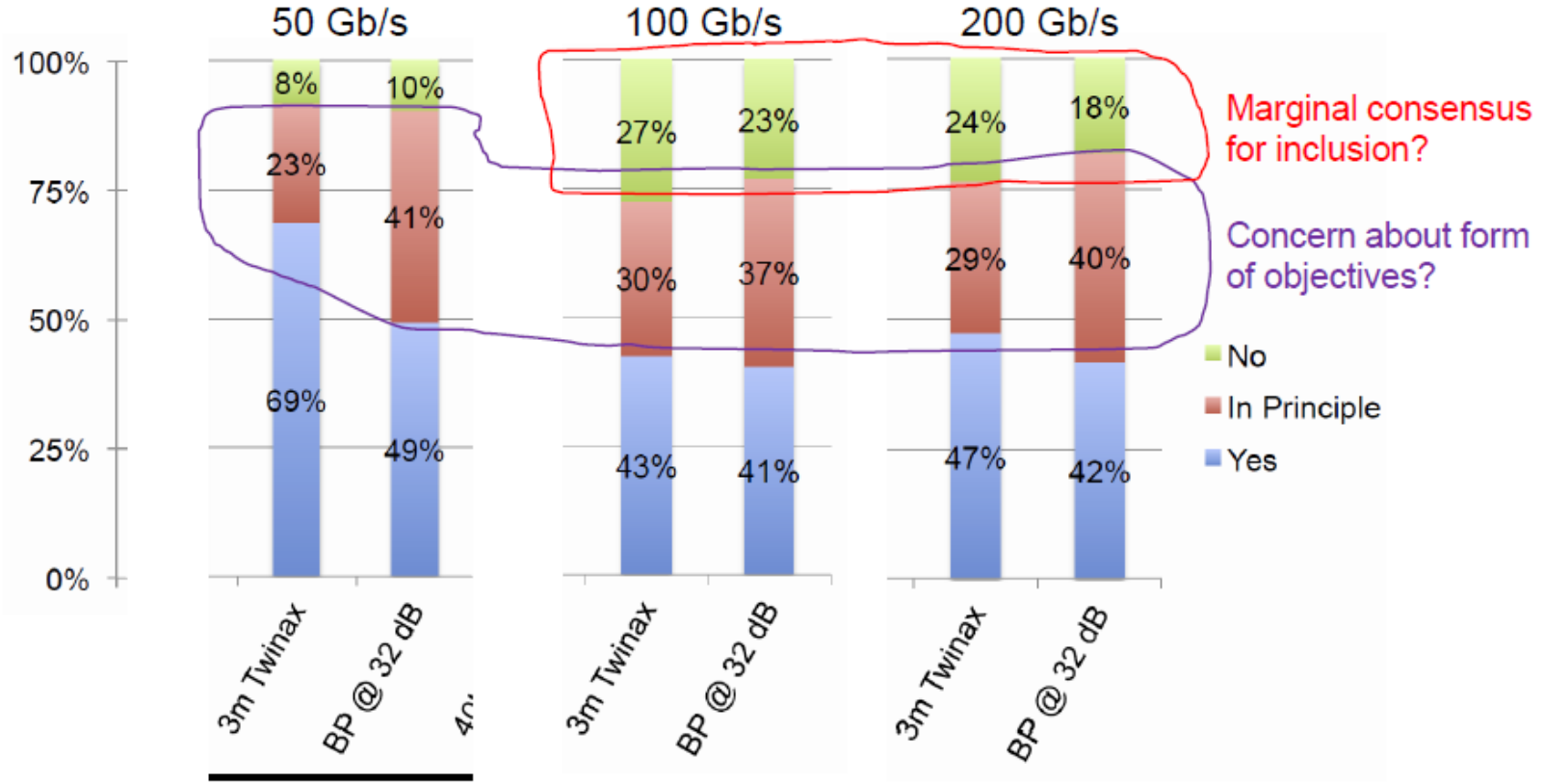
– Define a two lane 100 Gb/s PHY for operation over a printed circuit board backplane.

–Define a two fiber 100 Gb/s PHY for operation over MMF with lengths up to at Least 100m

Source: http://www.ieee802.org/3/50G/public/objectives_50G_NGOATH_01a_0116.pdf

Consensus survey monkey

- Survey monkey results were published from Mark Nowell.



from: http://www.ieee802.org/3/50G/public/adhoc/archive/nowell_010616_50GE_NGOATH_adhoc.pdf

Consensus survey comments

3m Twinax → 50Gb/s no-FEC option for low-latency applications. → We should be open to a slightly shorter reach to ensure practicality. → need confirmation of technical feasibility **Backplane** → The numbers 32 and 12.9 are wrong. Nyquist frequency for the likely encoding is approx. 13.3 GHz. The work done in OIF suggests that an insertion loss of 27-28 dB is the limit for reasonable PAM4 transceivers at this rate, far less than 32 dB. <snip> I intend to propose an objective for "PCB backplane consistent with a total insertion loss equivalent to 3m of Twinax cable". → Need technical feasibility data → I think an insertion loss in the range of 28 to 30dB is more realistic. → More detailed work on Channel loss → uncertain of the 32 dB limit.	50 Gb/s
3m Twinax → need BMP data → We should be open to a slightly shorter reach to ensure practicality. → Only reach should be defined. Strongly recommend to consider high performance computing applications where latency is critical and Active cable may be needed. **Backplane** → Adoption of a backplane objective is fine. It is not clear what an appropriate insertion loss target should be. → With serial 100 Gb/s not technically feasible it does not make sense to define 2x50G Cu → technical feasibility and should mirror 50G objective. → uncertain of the 32 dB limit.	100 Gb/s
3m Twinax → I see no reason to define a 200G copper PMD at this point in time. The primary purpose for such PMDs would be to connect servers to TOR switches… → We should be open to a slightly shorter reach to ensure practicality. → Only reach should be defined. Strongly recommend to consider high performance computing applications where latency is critical and Active cable may be needed. **Backplane** → The numbers 32 and 12.9 are wrong. Nyquist frequency for the likely encoding is approx. 13.3 GHz. The work done in OIF suggests that an insertion loss of 27-28 dB is the limit for reasonable PAM4 transceivers at this rate, far less than 32 dB. <snip> I intend to propose an objective for "PCB backplane consistent with a total insertion loss equivalent to 3m of Twinax cable". → Same reason as above. I see no need for a 200GE backplane interface at this point in time → I think an insertion loss in the range of 28 to 30dB is more realistic. → More detailed work on Channel loss → uncertain of the 32 dB limit.	200 Gb/s

Observation: Common theme is concern for choice of backplane insertion loss number.

from: http://www.ieee802.org/3/50G/public/adhoc/archive/nowell_010616_50GE_NGOATH_adhoc.pdf

Copper twinaxial cables objectives

•Considerations for 50 Gb/s cable assembly, test fixture and channel specifications consistent with adopted objectives

– Define single-lane 50 Gb/s PHYs for operation

- copper twinaxial cables.

–Define a two lane 100 Gb/s PHY for operation over copper twinaxial cables.

–Define single-lane 200 Gb/s PHYs for operation

- copper twinaxial cables.

•802.3by Adopted and approved Objective

– Define a single-lane 25 Gb/s PHY for operation over links consistent with copper twin axial cables, with lengths up to at least 3m

•Considerations for 50 Gb/s, 100 Gb/s, 200 Gb/s cable assembly, test fixture and channel specifications consistent with adopted objectives

– Define single-lane 50 Gb/s PHYs for operation over links consistent with copper twin axial cables with lengths up to at least 3 m.

–Define two-lane 100 Gb/s PHYs for operation over links consistent with copper twin axial cables with lengths up to at least 3 m.

–Define four-lane 200 Gb/s PHYs for operation over links consistent with copper twin axial cables with lengths up to at least 3 m.

Copper twinaxial cables objectives

•Considerations for 50 Gb/s, 100 Gb/s, 200 Gb/s cable assembly, test fixture and channel specifications consistent with adopted objectives

– Define single-lane 50 Gb/s PHYs for operation over links consistent with copper twin axial cables with lengths up to at least 3 m.

–Define two-lane 100 Gb/s PHYs for operation over links consistent with copper twin axial cables with lengths up to at least 3 m.

–Define four-lane 200 Gb/s PHYs for operation over links consistent with copper twin axial cables with lengths up to at least 3 m.

•Length considerations predicated on development of channel insertion loss budget

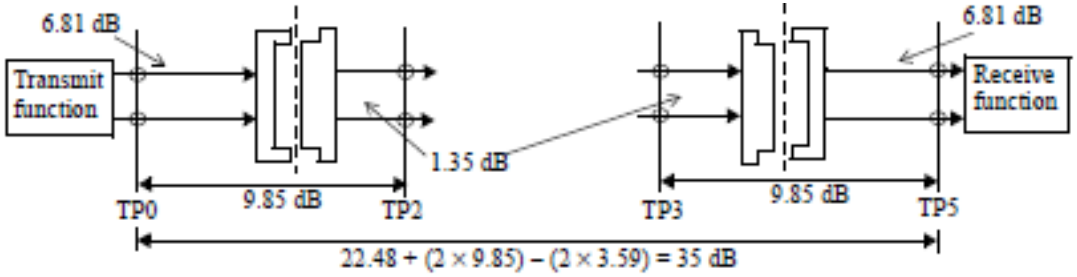


Table 110A–1—Cable insertion loss budget values at 12.8906 GHz

Parameter	CA-25G-L	CA-25G-S	CA-25G-N	Units
IL_{Chmax}	35	29	28.02	dB
IL_{Camax}	22.48	16.48	15.50	dB
$IL_{Ch0.5m}$	20.52			dB
IL_{Camin}	8			dB
IL_{Host}	9.85			dB
$IL_{MateITF}$	3.59			dB

Leverage of industry investment

Technology	Nomenclature	Description	Status
Backplanes	100GBASE-KP4 & KR4 CEI-56G-LR-PAM4	4 x 25 Gb/s backplane 56 Gb/s PAM4	IEEE 802.3bj Published Straw Ballot
Chip-to-Module	CDAUI-8 CEI-56G-VSR-PAM4	8 x 50 Gb/s PAM4 60 Gb/s PAM4	IEEE P802.3bs in Task Force Rev Straw Ballot
Chip-to-Chip	CDAUI-8 CEI-56G-MR-PAM4	8 x 50 Gb/s PAM4 60 Gb/s PAM4	IEEE P802.3bs in Task Force Rev Straw Ballot
SMF Optical	400GBASE-FR8 & LR8 400GBASE-DR4	8 x 50 Gb/s PAM4 4 x 100 Gb/s PAM4	IEEE P802.3bs in Task Force Review
Module Form Factor	SFP56	1 x 50 Gb/s	Extension to Summary Document SFF-8402
	QSFP56	4 x 50 Gb/s	Extension to Summary Document SFF-8665

CAUI/CDAUI chip-to-module interfaces

- CAUI-4 signaling rate for each lane is 25.78125 GBd[1].

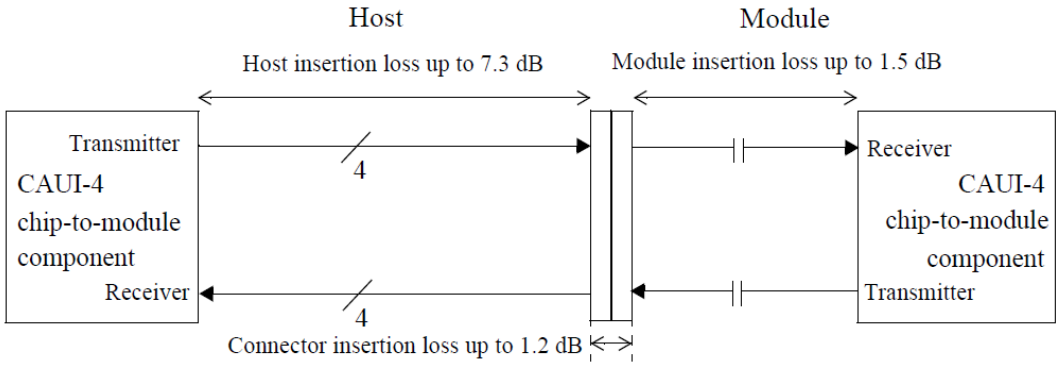


Figure 83E–2—Chip-to-module insertion loss budget at 12.89 GHz

- CDAUI-8 signaling rate for each lane is 26.5625 GBd[2]

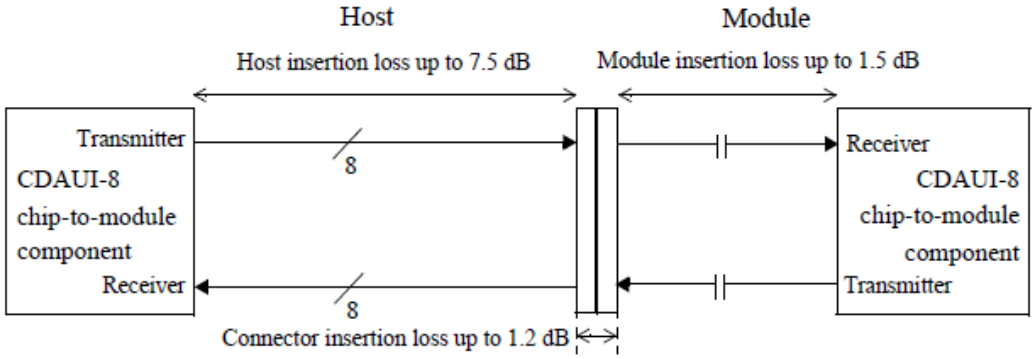


Figure 120E–2—Chip-to-module insertion loss budget at 13.28 GHz

[1] using spec similar to CEI-28G-VSR, [2] using spec similar to CEI-56G-VSR-PAM

Host Channels

- CAUI-4 signaling rate for each lane is 25.78125 GBd[1].

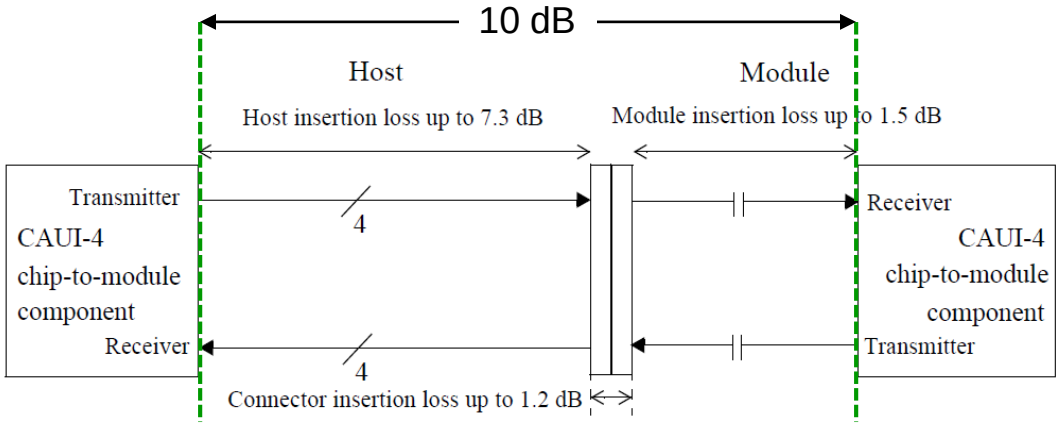


Figure 83E–2—Chip-to-module insertion loss budget at 12.89 GHz

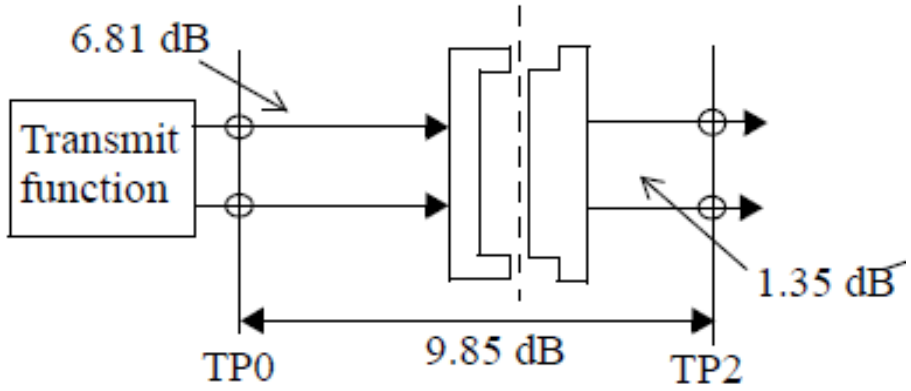
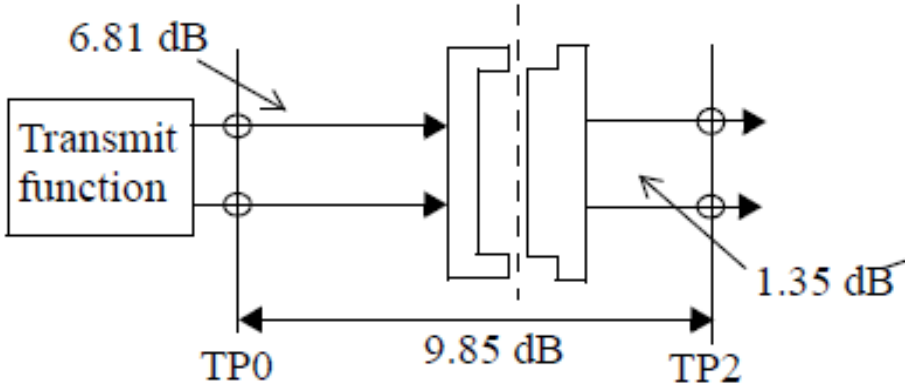


Figure 110A–1—Host Loss budget at 12.8906 GHz

[1] using spec similar to CEI-28G-VSR, [2] using spec similar to CEI-56G-VSR-PAM

Tx/RX PCB and Test Fixture PCB - Baseline

- Transmitter and receiver differential printed circuit board trace loss (with IL @ 13.28GHz)
  - Specified in 92A.4 EQ(92A-1 and 92A-2)– referenced 110A.4
- Test fixture printed circuit board reference insertion loss (with IL @ 13.28 GHz)
  - Specified in 92.11 EQ(92-35) – referenced 110B.1.1



Host Loss budget at 12.8906 GHz

Transmitter and receiver differential PCB IL

- IL @ 13.28 GHz

$$IL_{PCB}(f) \le IL_{PCBmax}(f) = 0.5(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)}$$

for 0.01 GHz $\le f \le$ 19 GHz.

where

f is the frequency in GHz
$IL_{PCB}(f)$ is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmax}(f)$ is the recommended maximum insertion loss for the transmitter and receiver PCB

IL @ 12.89 GHz = 6.81 dB
IL @ 13.28 GHz = 7.00 dB

$$IL_{PCB}(f) \ge IL_{PCBmin}(f) = 0.086(0.0694 + 0.4248\sqrt{f} + 0.9322f) \quad \text{(dB)}$$

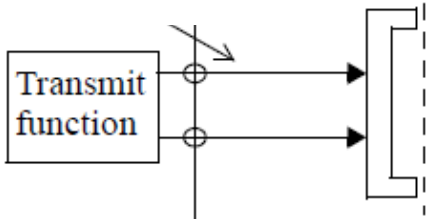
for 0.01 GHz $\le f \le$ 19 GHz.

where

f is the frequency in GHz
$IL_{PCB}(f)$ is the insertion loss for the transmitter and receiver PCB
$IL_{PCBmin}(f)$ is the minimum insertion loss for the transmitter and receiver PCB

IL @ 12.89 GHz = 1.17 dB
IL @ 13.28 GHz = 1.20 dB

IL @ 12.89 GHz = Max 6.81 dB
= Min 1.17 dB



Test fixtures PCB insertion loss

$$IL_{tfref}(f) = -0.00144 + 0.13824\sqrt{f} + 0.06624\,f \quad \text{(dB)}$$

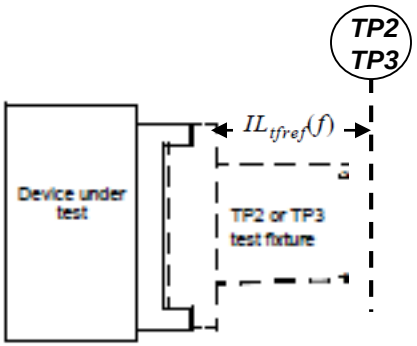
for $0.01 \le f \le 25$ GHz

where

f is the frequency in GHz

$IL_{tfref}(f)$ is the reference test fixture PCB insertion loss at frequency f

IL @ 12.89 GHz = 1.35 dB
IL @ 13.28 GHz = 1.38 dB



$$IL_{catf}(f) = -0.00125 + 0.12\sqrt{f} + 0.0575f \quad \text{(dB)}$$

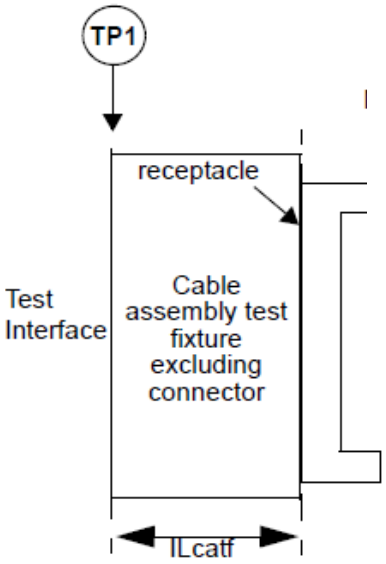
for 0.01 GHz $\le f \le$ 25 GHz

where

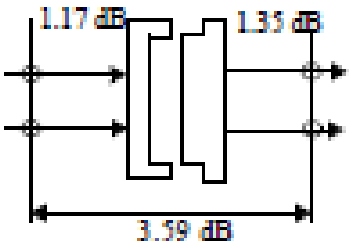
f is the frequency in GHz

$IL_{catf}(f)$ is the reference test fixture printed circuit board insertion loss at frequency f

IL @ 12.89 GHz = 1.17 dB
IL @ 13.28 GHz = 1.20 dB

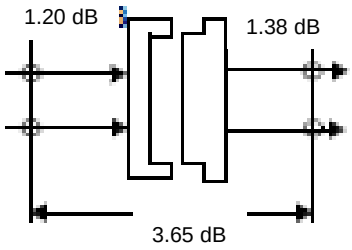


IL @ 12.89 GHz



Mated cable assembly and test point test fixture

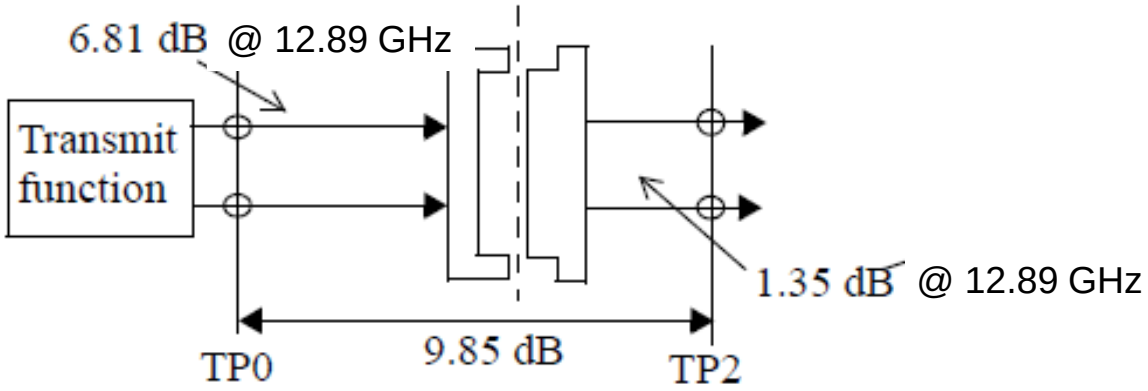
IL @ 13.28 GHz



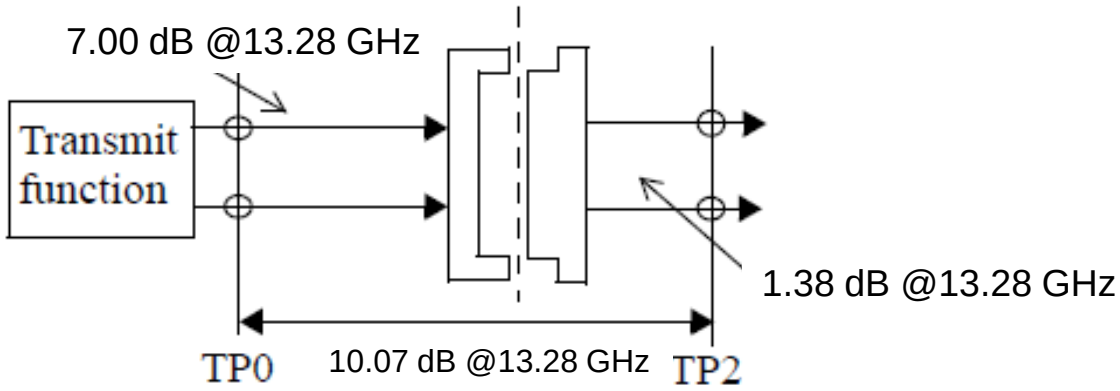
Mated cable assembly and test point test fixture

NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Host Channel – Baseline Proposal



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin. IL host connector @ 12.89 GHz = 9.85-6.81-1.35= 1.69 dB



Host Tx and Rx PCB losses

- Transmitter and receiver differential printed circuit board trace loss

GHz	dB/in
1	0.1856
6.5	0.8971
7	0.9557
12.89	1.5924
14	1.702

Attenuation* (dB/in) at:	1 GHz	6.5 GHz	7 GHz	12.89 GHz	14 GHz
Meg6_LowSR – Wide	0.0951	0.4159	0.4433	0.7562	0.8127
Meg6_LowSR – Narrow	0.1466	0.5849	0.6205	1.0152	1.0847
Meg6_HighSR – Wide	0.1175	0.5960	0.6367	1.0891	1.1688
Meg6_HighSR – Narrow	0.1856	0.8971	0.9557	1.5924	1.7020
ImpFR4_LowSR – Wide	0.1202	0.6096	0.6541	1.1772	1.2734
ImpFR4_LowSR – Narrow	0.1717	0.7794	0.8323	1.4410	1.5512
ImpFR4_HighSR – Wide	0.1427	0.7904	0.8484	1.5158	1.6367
ImpFR4_HighSR – Narrow	0.2106	1.0930	1.1692	2.0283	2.1813

*using Algebraic Model v2.02a – see backup slides for values entered in Model

PROPOSED PARAMETERS; GRAPHS ON PREVIOUS SLIDE

Proposal for Defining Material Loss
26-Jan 12

Elizabeth Kochuparambil
Joel Goergen

Cisco

http://www.ieee802.org/3/bj/public/jan12/kochuparambil_01a_0112.pdf

Channel Insertion Loss

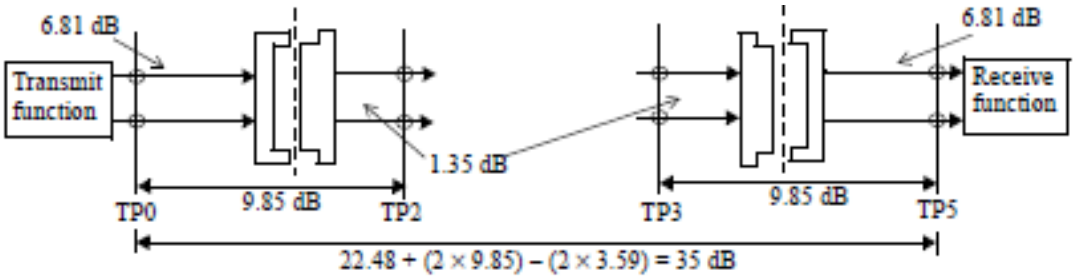
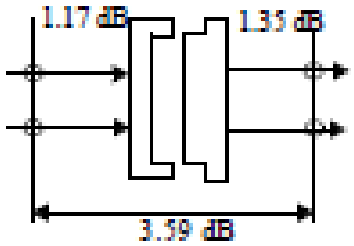


Table 110A–1—Cable insertion loss budget values at 12.8906 GHz

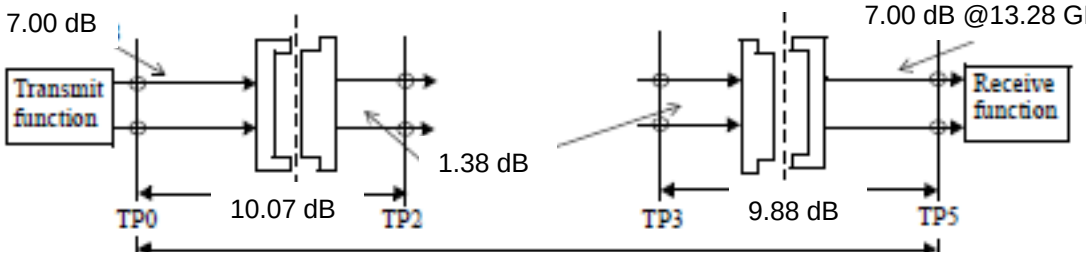
Parameter	CA-25G-L	CA-25G-S	CA-25G-N	Units
IL_{Chmax}	35	29	28.02	dB
IL_{Camax}	22.48	16.48	15.50	dB
$IL_{Ch0.5m}$	20.52			dB
IL_{Camin}	8			dB
IL_{Host}	9.85			dB
$IL_{MatedITF}$	3.59			dB

Channel IL @12.89 GHz = Cable assembly IL-(2*9.85)+(2*3.59)

IL @ 12.89 GHz

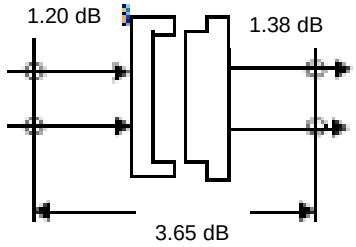


Mated cable assembly and test point test fixture



Channel IL @13.28 GHz = Cable assembly IL-(2*10.07)+(2*3.65)

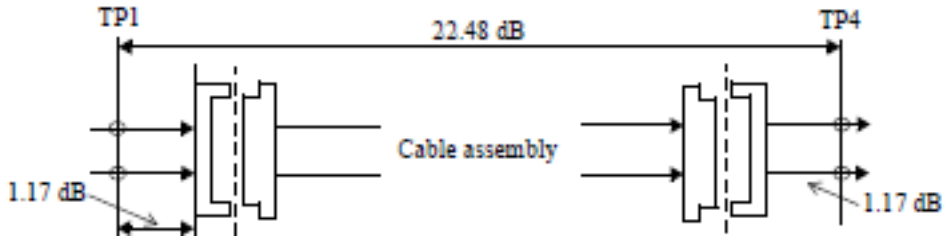
IL @ 13.28 GHz



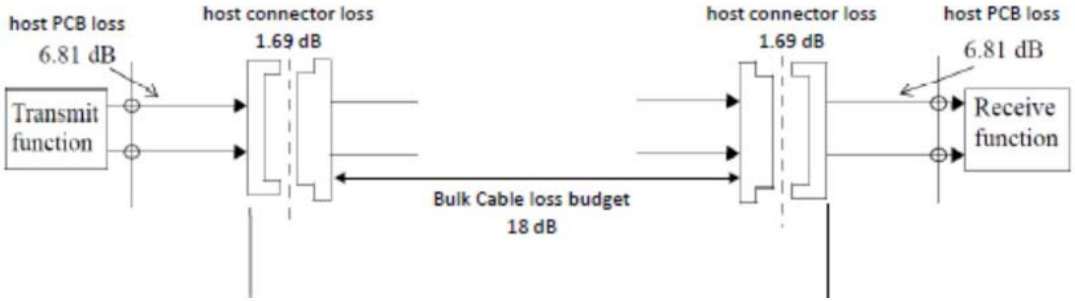
Mated cable assembly and test point test fixture

NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Cable Assembly Insertion Loss



Bulk cable assumed = Cable assembly IL-(2*1.17)+(2*1.07)



Bulk cable assumed = Channel IL- (2*6.81)+(2*1.69)

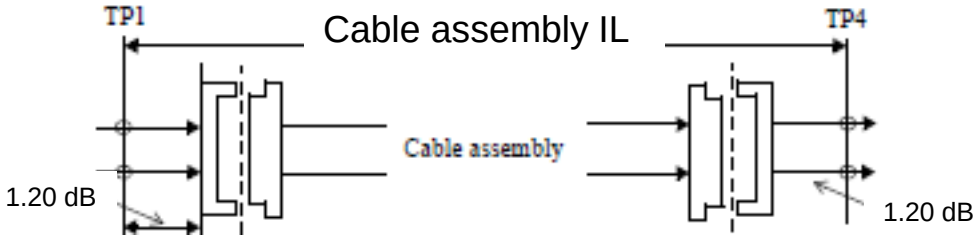
NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Channel IL (dB)@ 12.98 GHz	Cable assembly IL (db)@ 12.89 GHz	Bulk cable dB @ 12.89 GHz
27.0	14.48	10.00
27.5	14.98	10.50
28.0	15.48	11.00
28.02	15.50	11.02
28.5	15.98	11.50
29.0	16.48	12.00
29.5	16.98	12.50
30.0	17.48	13.00
30.5	17.98	13.50
31.0	18.48	14.00
31.5	18.98	14.50
32.0	19.48	15.00
32.5	19.98	15.50
33.0	20.48	16.00
33.5	20.98	16.50
34.0	21.48	17.00
34.5	21.98	17.50
35.0	22.48	18.00

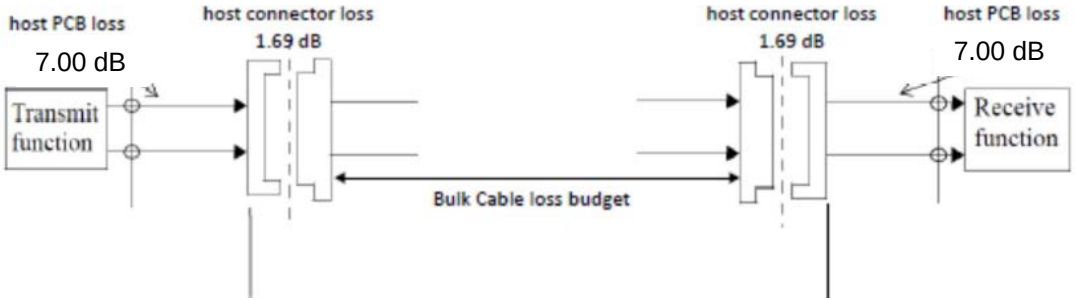
Table 110A–1—Cable insertion loss budget values at 12.8906 GHz

Parameter	CA-25G-L	CA-25G-S	CA-25G-N	Units
IL_{Chmax}	35	29	28.02	dB
IL_{Camax}	22.48	16.48	15.50	dB
$IL_{Ch0.5m}$	20.52			dB
IL_{Camin}	8			dB
IL_{Host}	9.85			dB
$IL_{MatedTF}$	3.59			dB

Baseline Proposal - starting point (3 m cable assembly)



Bulk cable assumed @13.28 GHz = Cable assembly IL-(2*1.20)+(2*1.07)

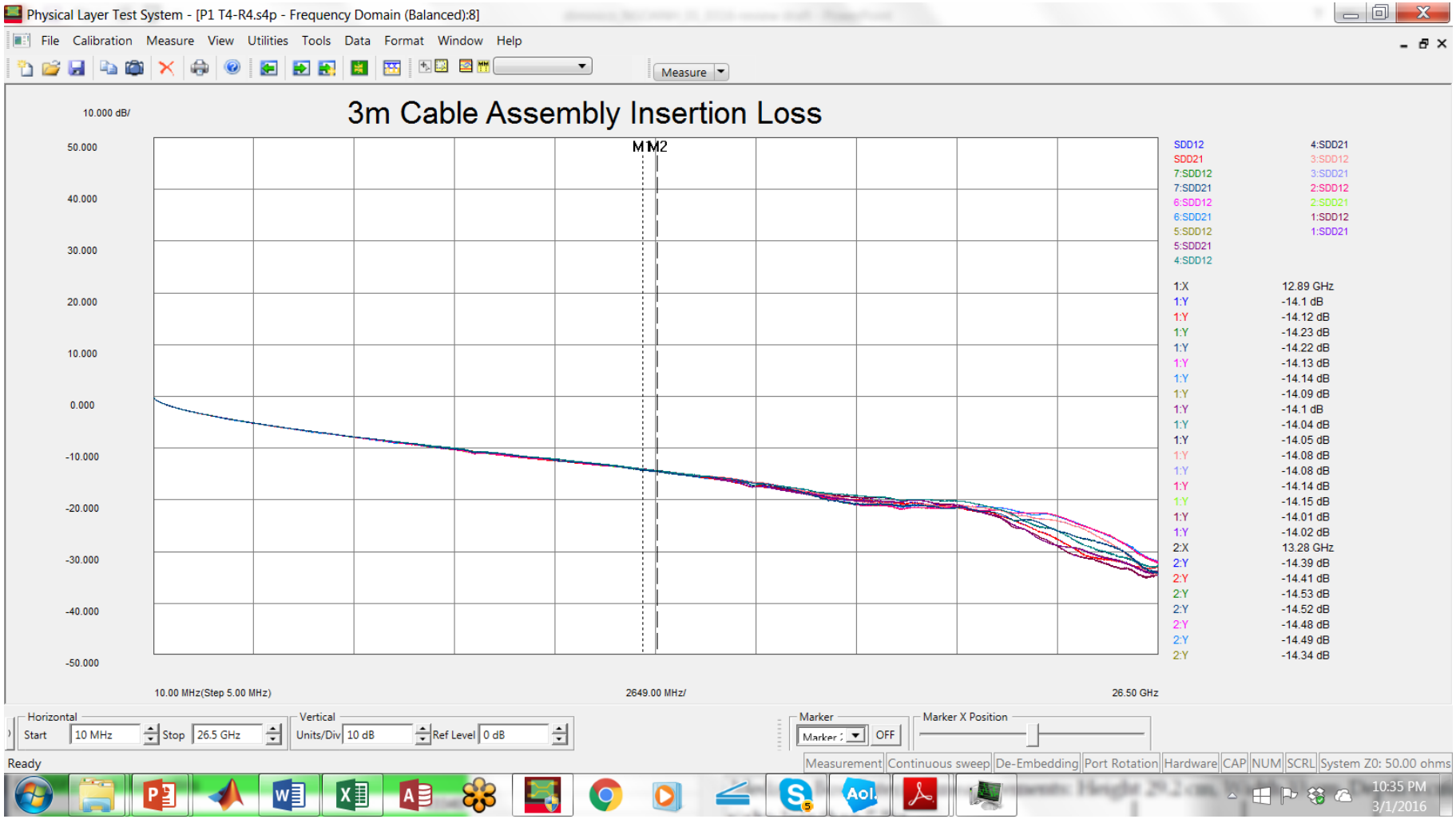


Bulk cable assumed @13.28 GHz = Channel IL- (2*7)+(2*1.69)

NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Channel IL (dB) @ 13.28 GHz	Cable assembly IL (db) @ 13.28 GHz	Bulk cable dB @ 13.28 GHz
27.0	14.16	9.62
27.5	14.66	10.12
28.0	15.16	10.62
28.5	15.66	11.12
29.0	16.16	11.62
29.5	16.66	12.12
30.0	17.16	12.62
30.5	17.66	13.12
31.0	18.16	13.62
31.5	18.66	14.12
32.0	19.16	14.62
32.5	19.66	15.12
33.0	20.16	15.62
33.5	20.66	16.12
34.0	21.16	16.62
34.5	21.66	17.12
35.0	22.16	17.62

NGOATH Contributed Channel Data



http://www.ieee802.org/3/50G/public/channel/index.html

Molex_zQSFP-zQSFP_3m_26awg

Cable Assembly – Baseline Proposal

- Cable assembly - consistent with CL92 and CL110 – referenced parameters @ 13.28 GHz

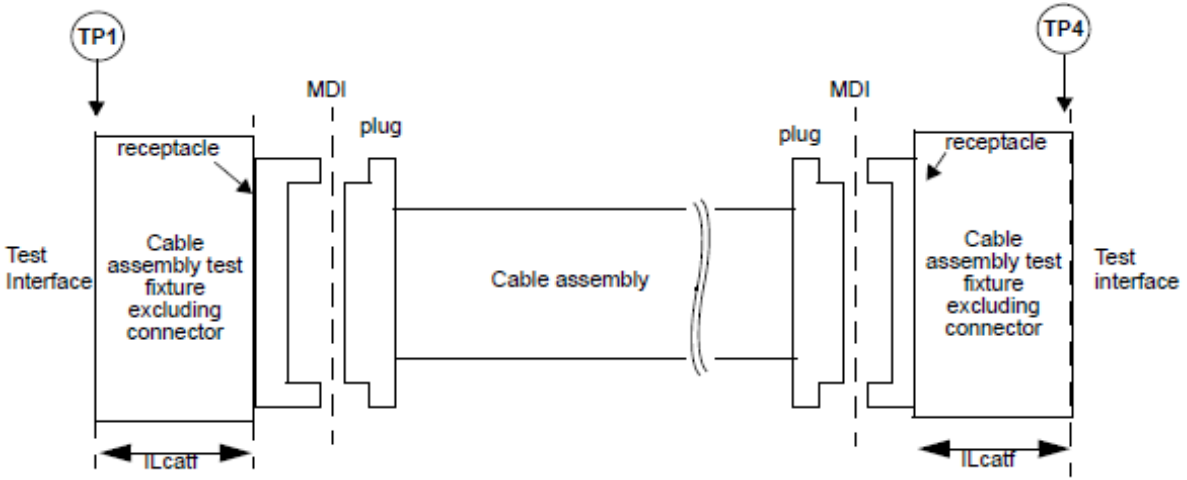
Table 92–10—Cable assembly differential characteristics summary

Description	Reference	Value	Unit
Maximum insertion loss at 12.8906 GHz	92.10.2	22.48	dB
Minimum insertion loss at 12.8906 GHz	92.10.2	8	dB
Minimum return loss at 12.8906 GHz	92.10.3	6	dB
Differential to common-mode return loss	92.10.4	Equation (92–28)	dB
Differential to common-mode conversion loss	92.10.5	Equation (92–29)	dB
Common-mode to common-mode return loss	92.10.6	Equation (92–30)	dB

Table 110–10—Cable assembly characteristics summary

Description	Reference	CA-25G-L	CA-25G-S	CA-25G-N	Unit
Maximum insertion loss at 12.8906 GHz	110.10.2	22.48	16.48	15.5	dB
Minimum insertion loss at 12.8906 GHz	110.10.2	8			dB
Minimum differential return loss at 12.8906 GHz	110.10.3	6			dB
Differential to common-mode return loss	110.10.4	Equation (92–28)			dB
Differential to common-mode conversion loss	110.10.5	Equation (92–29)			dB
Common-mode to common-mode return loss	110.10.6	Equation (92–30)			dB
COM	110.10.7	See Table 110–11			dB

from [0.01/0.05/0.2] ≤ f ≤ 19 GHz



COM- Baseline Proposal

- COM - consistent with methodology CL92 and CL110
- COM parameter values TBD

Table 110–11—COM parameter values

Parameter	Symbol	CA-25G-N	CA-25G-S	CA-25G-L[a]	Units
Signaling rate	f_b	25.78125			GBd
Maximum start frequency	f_{min}	0.05			GHz
Maximum frequency step[b]	Δf	0.01			GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface	 C_d z_p z_p C_p	 2.5×10^{-4} 12 30 2.5×10^{-4}			 nF mm mm nF
Single-ended reference resistance	R_0	50			Ω
Single-ended termination resistance	R_d	55			Ω
Receiver 3 dB bandwidth		$0.75 \times f_b$			GHz
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.62			
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 −0.18 0 0.02			
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 −0.38 0 0.02			
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 −16 0 1	 −12 0 1	 −12 0 1	 dB dB dB
Continuous time filter, zero frequency	f_z	$f_b / 4$			GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b / 4$ f_b			GHz

TBD

Table 110–11—COM parameter values *(continued)*

Parameter	Symbol	CA-25G-N	CA-25G-S	CA-25G-L[a]	Units
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.6 0.6			 V V V
Number of signal levels	L	2			
Level separation mismatch ratio	R_{LM}	1			
Transmitter signal-to-noise ratio	SNR_{TX}	2[c]	27	27	dB
Number of samples per unit interval	M	3			
Decision feedback equalizer (DFE) length	N_b	3			
Normalized DFE coefficient magnitude limit, for $n = 1$ to N_b	$b_{max}(n)$	0.35	0.5	1	—
Random jitter, RMS	σ_{RJ}	0.01			UI
Dual-Dirac jitter, peak	A_{DD}	0.05			UI
One-sided noise spectral density	η_0	5.2×10^{-8}			V^2/GHz
Target detector error ratio	DER_0	10^{-12}	10^{-8}	10^{-5}	—
Channel Operating Margin (min.)	COM	3[c]	3	3	dB

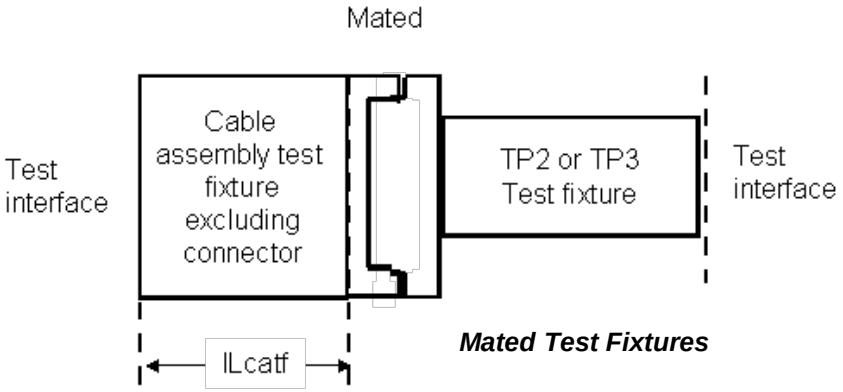
[a] The parameters for CA-25G-L are the same as those for 100GBASE-CR4 (Table 93–8), except for A_{fe}.
[b] For cable lengths greater than 4 m, a frequency step (Δf) no larger than 5 MHz is recommended.
[c] For CA-25G-N cable assemblies with insertion loss at 12.8906 GHz greater than 12 dB, the minimum COM is relaxed to 2.2 dB.

TBD

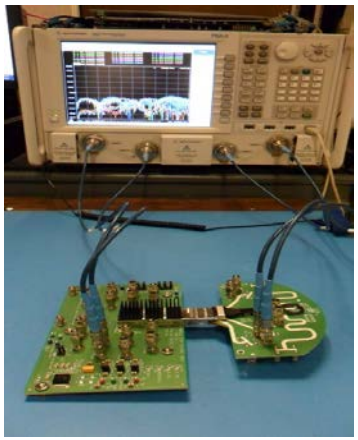
Consider: config_com_ieee8023_93a=CDAUI-8-C2C_D1p1_mellitz_01_0116.xls

Test Fixtures

- Test Fixture specifications - consistent with CL92 and CL110
- Test fixtures specified in a mated state used for testing the transmitter, the receiver and cable assembly measurements
- The TP2/TP3 test fixture also known in the industry as Host Compliance Board (HCB) is required for measuring the transmitter specifications at TP2 and the receiver return loss at TP3.
- The cable assembly test fixture also known in the industry as Module Compliance Board (MCB) is required for measuring the cable assembly specifications at TP1 and TP4.



Mated Test Fixtures



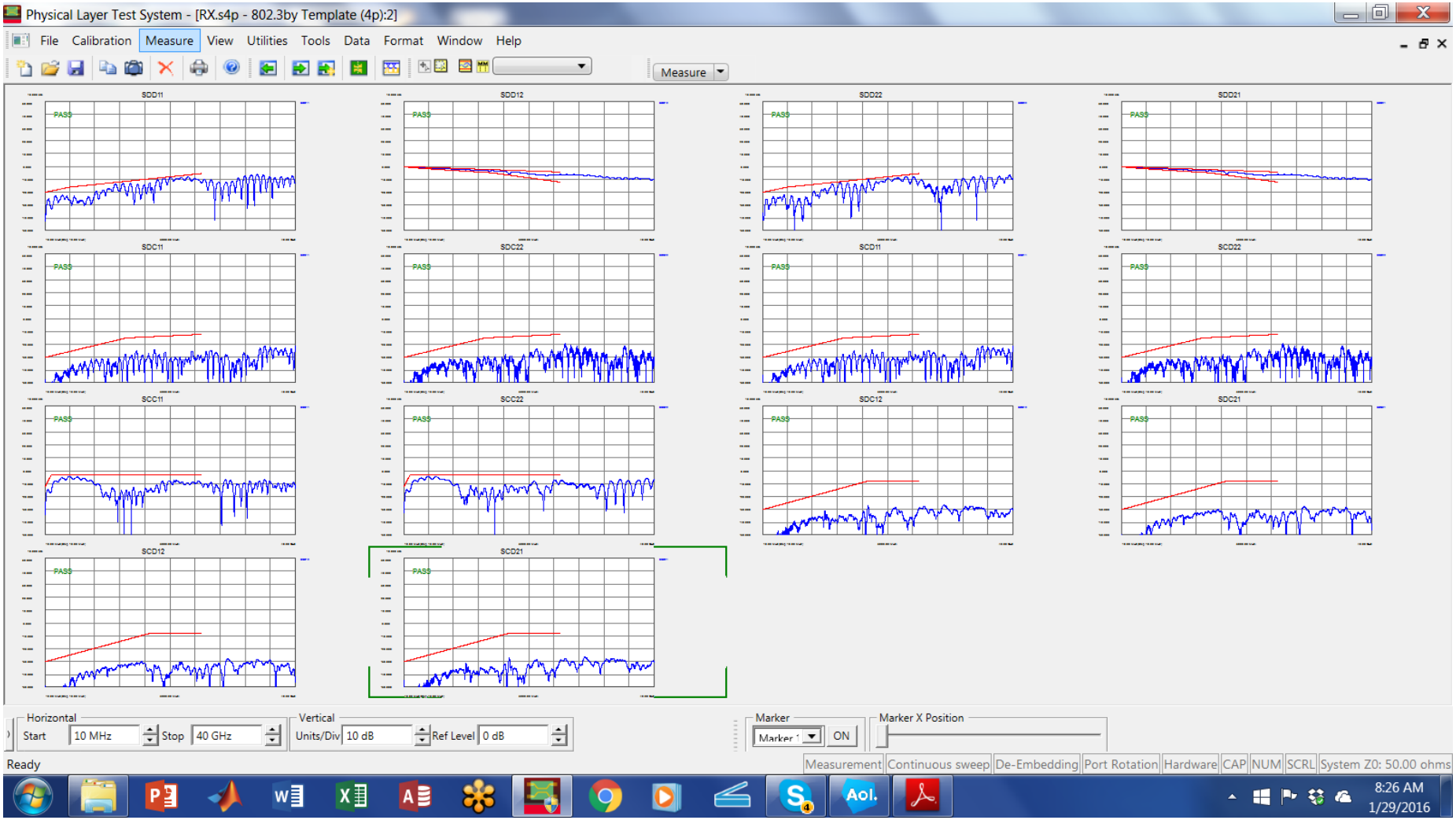
Test Fixtures - Baseline Proposal

- Test Fixture specifications - consistent with CL92 and CL110

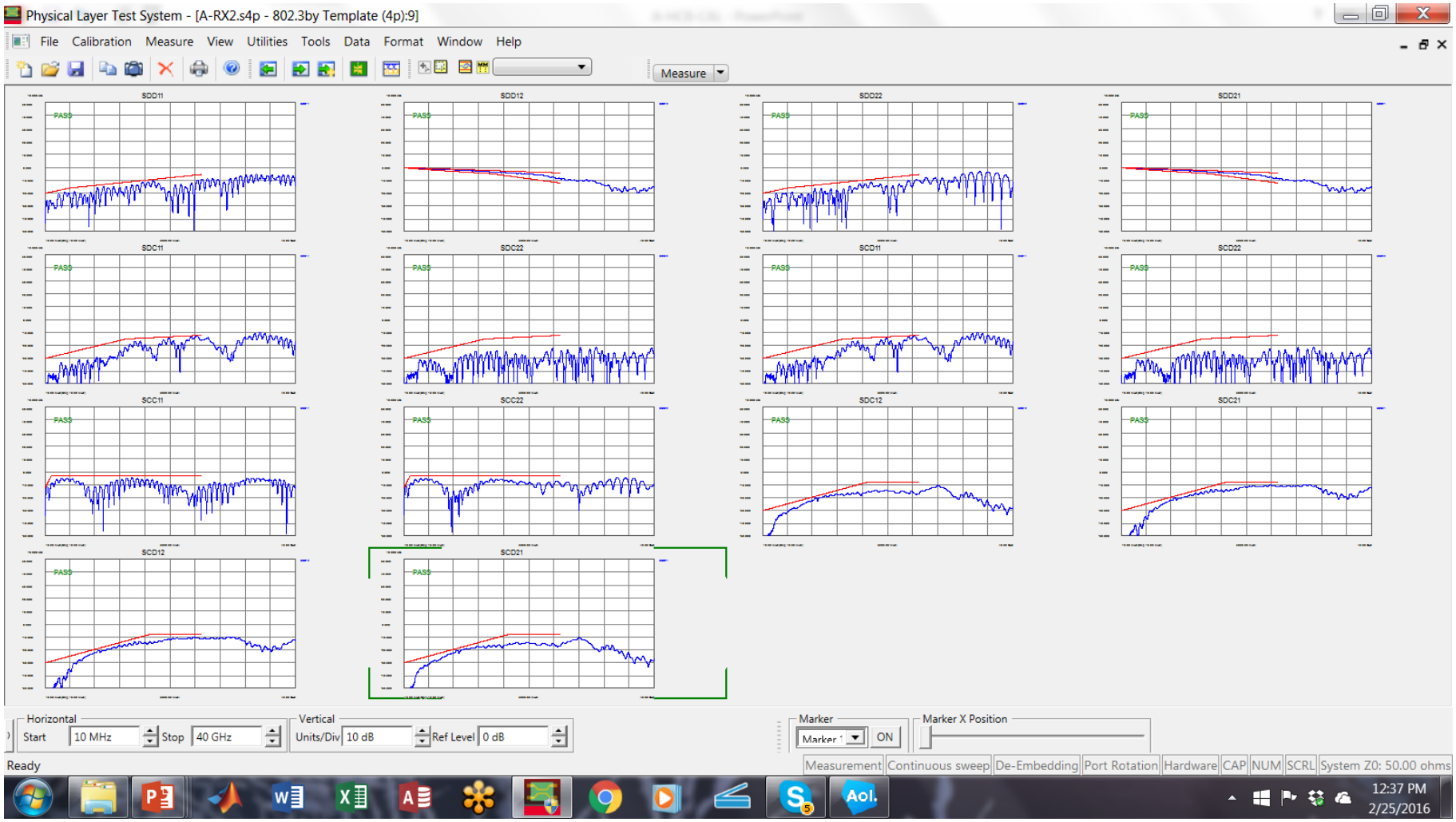
Mated test fixtures parameters

Parameter description	f(GHz)	Unit
Maximum insertion Loss	0.01≤f≤25	dB
Minimum Insertion Loss	0.01≤f≤25	dB
Minimum Return Loss	0.01≤f≤25	dB
Common-mode conversion insertion loss	0.01≤f≤25	dB
Common-mode return loss	0.01≤f≤25	dB
Common-mode to differential –mode return loss	0.01≤f≤25	dB
Integrated crosstalk noise		

SFP28-Mated Test Fixture – 802.3bj/802.3by Specification



QSFP28-Mated Test Fixture – 802.3bj/802.3by Specification



BACKUP

CAUI-4/CDAUI-10 chip-to-module interfaces

- CAUI-4 signaling rate for each lane is 25.78125 GBd[1].

$$Insertion\_loss(f) \le \begin{cases} 1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \le f < 14 \\ 1.076(-18 + 2f) & 14 \le f < 18.75 \end{cases} \quad \text{(dB)} \qquad \text{(83E–1)}$$

where

f	is the frequency in GHz
Insertion_loss(f)	is the CAUI-4 chip-to-module insertion loss

- CDAUI-8 signaling rate for each lane is 26.5625 GBd[2]

$$Insertion\_loss(f) \le 1.076(0.0801 + 0.5736\sqrt{f} + 0.6046f) \quad \text{(dB)} \qquad \text{(120E–1)}$$

for $0.01 \le f \le 28.05$

where

f	is the frequency in GHz
Insertion_loss(f)	is the CDAUI-8 chip-to-module insertion loss

[1] using spec similar to CEI-28G-VSR, [2] using spec similar to CEI-56G-VSR-PAM

CAUI-4/CDAUI-10 chip-to-module interfaces