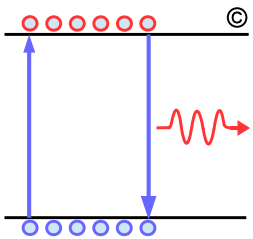

PCS Consideration for 50 GbE and NG 100 GbE

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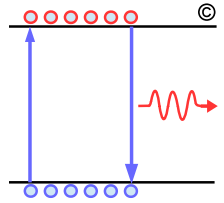
NGOATH AdHoc Meeting

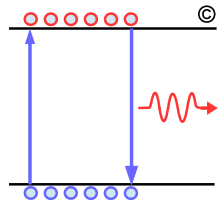
Feb 23, 2016

50 GbE and NG 100 GbE should Support AUI based on 25G I/O

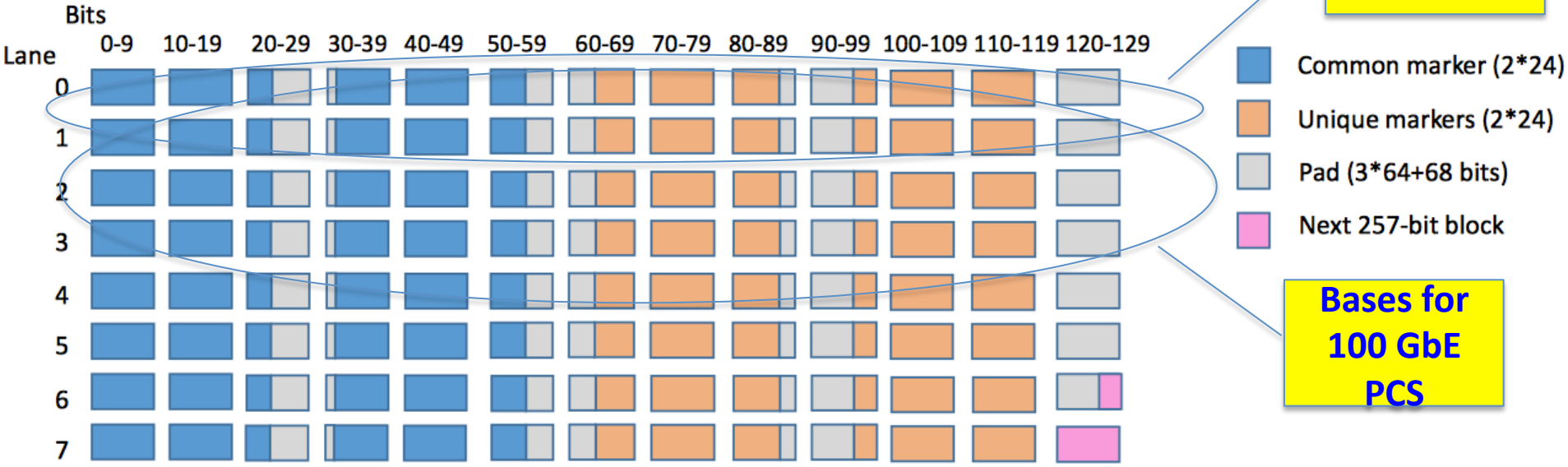


- **25G MSA does have a 50 GbE mode of operation http://25gethernet.org**
  - 25G MSA specification is not public but there is a public overview
    - http://25gethernet.org/sites/default/files/25G%20and%2050G%20Specification%20Overview.pdf
  - 50 GbE is implemented over 2 lanes of 25G as illustrated by
    - http://www.ieee802.org/3/50G/public/adhoc/archive/stone_021716_50GE_NGOATH_adhoc-v2.pdf
  - IEEE 50 GbE to support legacy implementation would require 50GAUI-2 PMA
- **Transition to 50G/lane optics may happen faster than migration to ASICs to 50G IO**
  - 50 GbE or NG 100 GbE implementation may take advantage of 400 GbE hardware which supports 16x25G electrical but 50G/lane or 100G/lane optics
  - To support flexible migration the 50 GbE PCS and NG 100 GbE PCSs should support respectively 2 and 4 lanes PMAs
- **Full backward compatibility could be provided by a PMA-PMA device as long as the objective support the following:**
  - 50 GbE need to supports PCS and 50GAUI-2/1
  - NG 100 GbE need to supports PCS and CAUI-4/2.

Option I: 50 GbE and NGOATH 100 GbE PCS

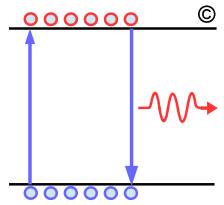


- **Based on 25G PCS lanes as proposed 200 GbE PCS format**
  - http://www.ieee802.org/3/bs/public/adhoc/logic/feb9_16/gustlin_01_0216_logic.pdf



- 50 GbE can be based on 1x257b blocks, pad is filled with free running PRBS9
- 100 GbE can be based on 2x257b blocks, pad is filled with free running PRBS9
  - To provide backward compatibility with 100 GbE per CL82 require more complex PMA-PMA chip
- Implementation will support 50GAUI-2/1 and CAUI-4/2

Option II: Possible 50 GbE and 100 GbE PCS Format



- **Based on 5G PCS lanes per CL82**
  - For 50 GbE use half number of PCS lanes as was proposed:
    - http://www.ieee802.org/3/50G/public/adhoc/archive/gustlin_020316_50GE_NGOATH_adhoc.pdf
  - May support 25 GbE MSA implementation with simpler PMA chip
  - Implementation will support 50GAUI-2/1 and CAUI-4/2
  - If RS-FEC (544,514) is required is there value to preserve 5G PCS lane over synergy with .bs PCS?

FEC Lane	Reed-Solomon symbol index (10 bit symbols 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33					
0	AM0 (0 63)	AM4	AM8	AM12	AM16	
1	AM0	AM5	AM9	AM13	AM16	
2	AM0	AM6	AM10	AM14	AM16	
3	AM0	AM7	AM11	AM15	AM16	

Bases for 50 GbE PCS With 50GAUI-2

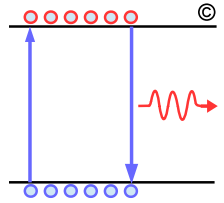
5b pad

Existing 100GbE FEC(528,514)

Bases for 100 GbE PCS with CAUI-2

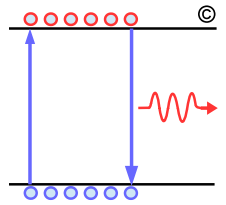
FEC Lane	Reed-Solomon symbol index (10 bit symbols 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31									
0	AM0 (0 63)	AM0	AM4	AM6	AM8	AM10	AM12	AM14	AM16	AM18
1	AM0	AM0	AM5	AM7	AM9	AM11	AM13	AM15	AM17	AM19

Option III: Possible 50 and 100 GbE PCS Format



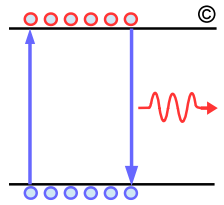
- **Follow CL49 10GBase-R PCS without any AM**
  - No clear advantage
  - No synergy with 100, 200, 400 GbE
  - Will only support CAUI-1 which is not currently under consideration
  - Will not support 50GAUI-2
- **CL49 does not offer viable PCS solution!**

FEC and Frame Format

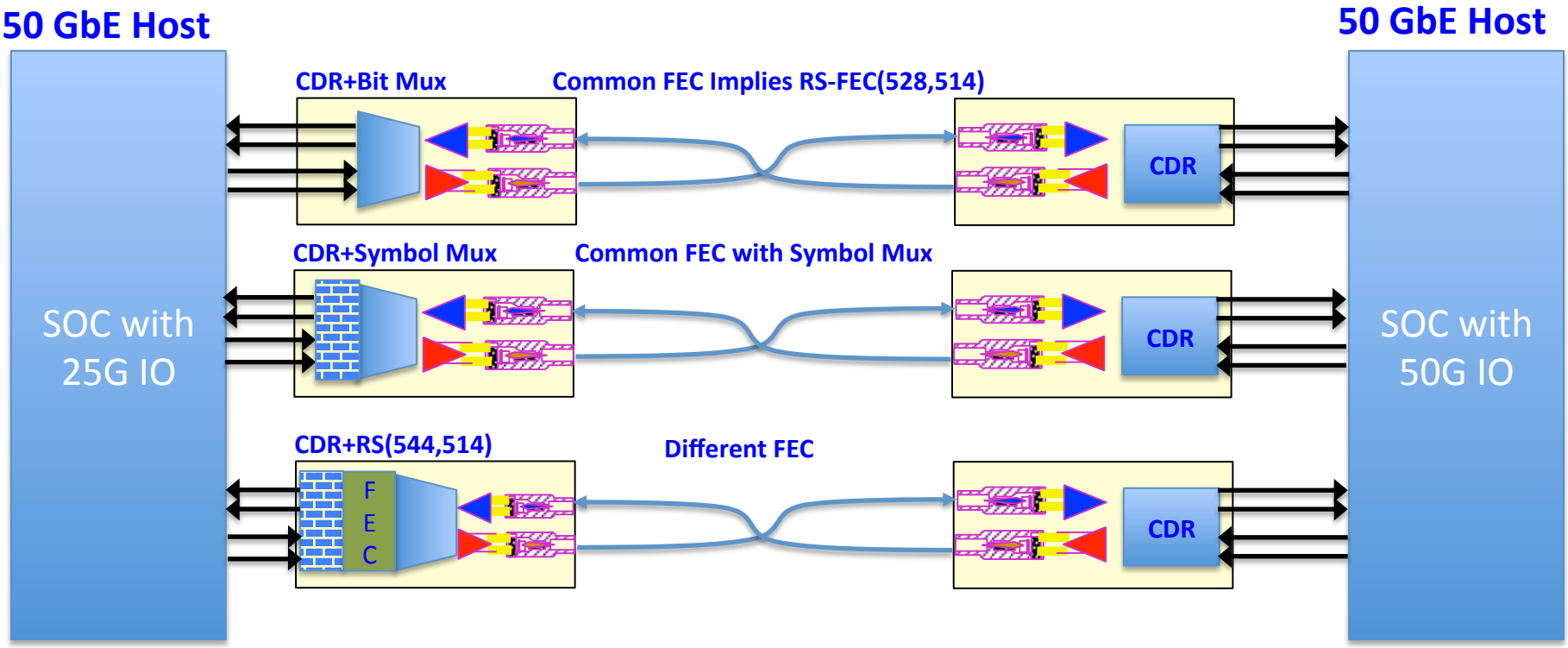


- **During the study group need to investigate ideally a common FEC addressing all 50 GbE PMDs with likely choices:**
  - RS-FEC (528,514)
  - RS-FEC (544,514)
- **During the study group need to investigate if RS-FEC (528,514) can address 100 GbE PMDs under consideration:**
  - If RS-FEC (528,514) can meet PMD requirement then there is stronger case to preserve 5G PCS lane to address backward compatibility
  - If NG 100GbE PMD require RS-FEC (544,514) then preserving 5G PCS lane is not as much a value
- **Frame format after FEC code and gain are determined then can determine how to form the FEC frame**
  - Bit mux would be preferable but have a penalty under burst error
  - Symbol mux has no penalty for using data from two logical lanes.

Possible 50 GbE Implementations

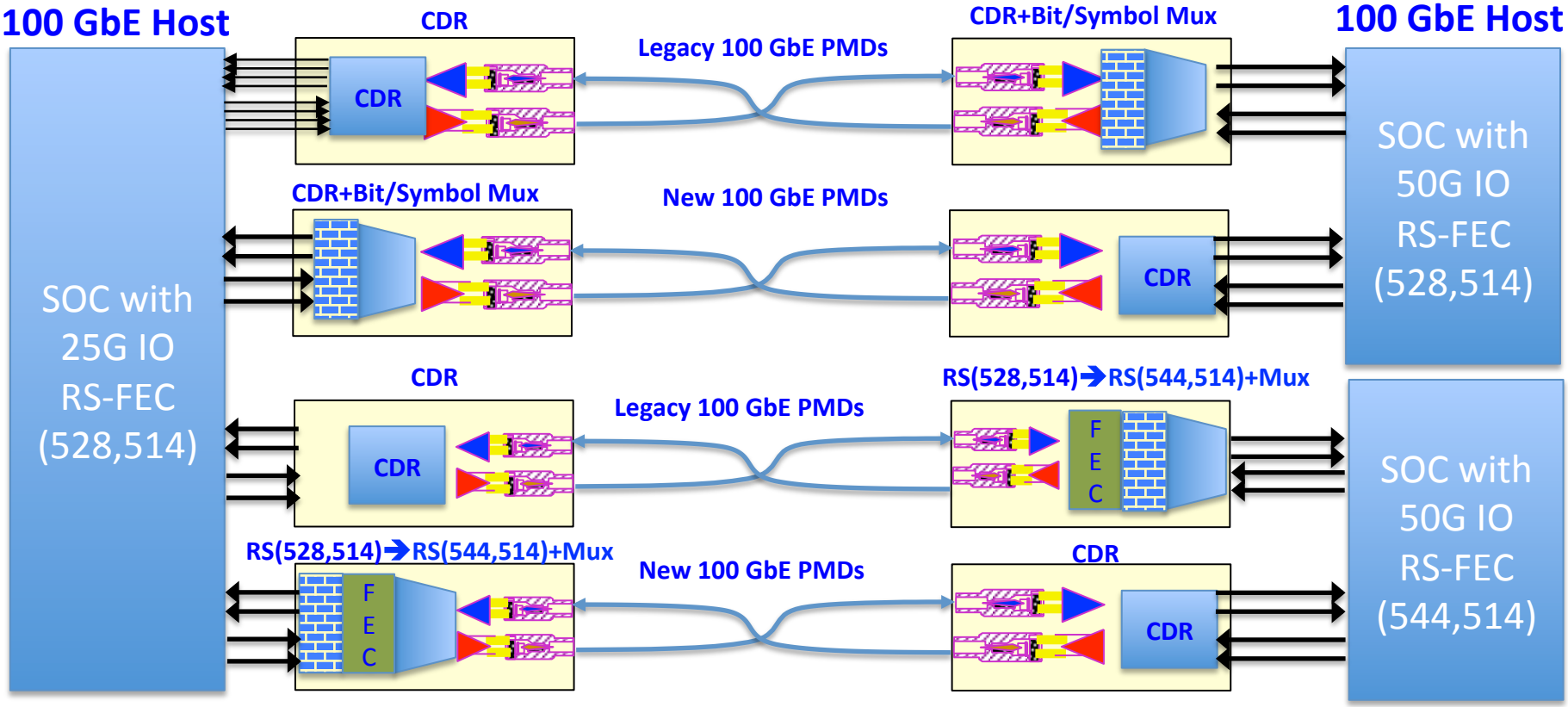


- The key to supporting any existing 50 GbE or early implementation of 50 GbE is to support 50GAUI-2
- PMA-PMA device can provide compatibility

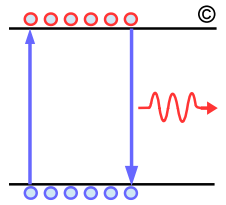


Possible 100 GbE Implementations

- **During the study group we need to balance ease of backward compatibility with synergy and if the PMD under consideration will have sufficient performance with RS-FEC (528,514)**
- **PMA-PMA device can provide compatibility**
  - PMA-PMA+FEC device can be placed in module or on the line card.



Summary



- **The 50 GbE Objective need to specify support for 50GAUI-2/1**
  - Specific implementation should be left to the task force
  - As long as the PCS supports 50GAUI-2 then a PMA-PMA device may form the 50GAUI-1 and provide backward compatibility
  - Need to investigate RS-FEC(528,514) and (544,514)
  - FEC lanes could be formed with simple bit mux or symbol mux
  - Level of support of 25GbE MSA implementation of 50 GbE
  - However full backward compatibility to the MSA should not come at expense of sacrificing 50 GbE PMD performance as the backward compatibility can always be solved with the PMA-PMA device.
- **The 100 GbE Objective need to specify support for 100GAUI-4/2**
  - Specific implementation should be left to the task force
  - Need to investigate RS-FEC(528,514) and (544,514)
  - FEC lanes could be formed with simple bit mux or symbol mux
  - Need to consider backward compatibility with 100 GbE PMDs as well as CL82 PCS
  - However full backward compatibility should not come at expense of sacrificing NG 100 GbE PMD performance as the backward compatibility can always be solved with the PMA-PMA device.