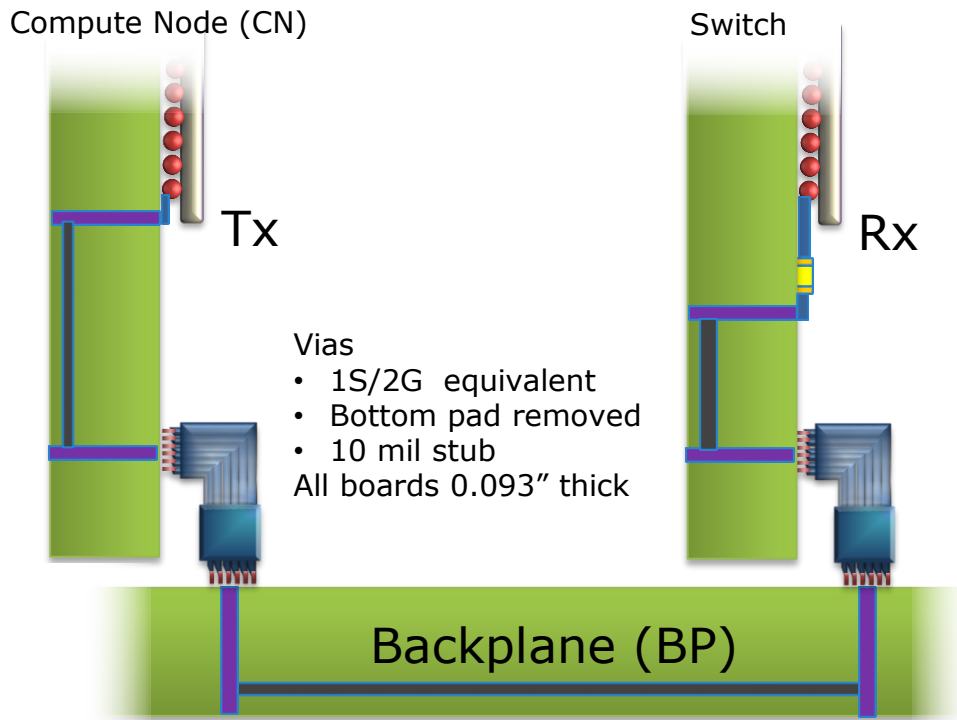


Backplane Channels: BGA ball to BGA ball with manufacturing considerations

Richard Mellitz, Intel Corporation

Approximate Topology



IL @ 13.28 GHzzzzzz	Switch Len	BP Len	CN Len
-10 dB	2"	2.1"	0.9"
-15 dB	3"	3.25"	2"
-20 dB	3"	8.25"	2"
-25 dB	3"	13.5"	2"
-30 dB	3"	18.7"	2"

Backplane Material loss
0.94dB/in @ 12.89GHz

CN and Switch Material Loss
1.81dBz/in @ 12.89GHz

Results (using parameters in oif2015 336 00_LR_sim_q415*)

*Channel Operating Margin (COM) for 56G-LR Proposal Update, October 2015, Shangha, Cathy Liu & Adam Healey

Loss	Corner	COM (dB) Long PKG	
		100 Ohm	85 Ohm
10dB	HZLzHz	4.5	5.5
10dB	LzHzLz	3.5	5.5
10dB	Nom	4.4	6.3
15dB	HZLzHz	5.0	5.8
15dB	LzHzLz	4.7	5.8
15dB	Nom	5.2	6.6
20dB	HZLzHz	4.5	5.3
20dB	LzHzLz	4.5	5.4
20dB	Nom	5.0	5.9
25dB	HZLzHz	3.3	4.1
25dB	LzHzLz	3.3	4.2
25dB	Nom	3.8	4.6
30dB	HZLzHz	1.3	2.0
30dB	LzHzLz	1.3	2.2
30dB	Nom	1.4	2.3

Loss	Corner	COM (dB) Short PKG	
		100 Ohm	85 Ohm
10dB	HZLzHz	4.4	5.5
10dB	LzHzLz	3.3	5.2
10dB	Nom	4.3	6.3
15dB	HZLzHz	5.6	6.1
15dB	LzHzLz	5.2	6.1
15dB	Nom	5.2	6.6
20dB	HZLzHz	4.8	5.6
20dB	LzHzLz	5.1	5.8
20dB	Nom	5.4	6.3
25dB	HZLzHz	4.0	4.7
25dB	LzHzLz	4.3	5.0
25dB	Nom	4.5	5.3
30dB	HZLzHz	2.8	3.2
30dB	LzHzLz	2.8	3.4
30dB	Nom	2.8	3.5

Nom – all board at target impedance

HZLzHz – line cards 10% higher than target, backplane 10% lower than target

LzHzLz – line cards 10% lower than target, backplane 10% Higher than target

COM table used

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	26.5625	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[2.5e-4 2.5e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30]	mm	[test cases]
z_p (NEXT)	[12 12]	mm	[test cases]
z_p (FEXT)	[12 30]	mm	[test cases]
z_p (RX)	[10 30]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[55 55]	Ohm	[TX RX]
f_r	0.75	*fb	
c(0)	0.6		min
c(-2)	[0:0.02:0.1]		
c(-1)	[-0.3:0.05:0]		[min:step:max]
c(1)	[-0.3:0.05:0]		[min:step:max]
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	10.625	GHz	
f_p1	10.625	GHz	
f_p2	1.00E+99	GHz	
A_v	0.43	V	
A_fe	0.43	V	
A_ne	0.65	V	
L	4		
M	32		
N_b	12	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	2.60E-08	V ² /GHz	
SNR_TX	31	dB	
R_LM	0.95		
DER_0	1.00E-04		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2
g_DC_HP	[-4:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

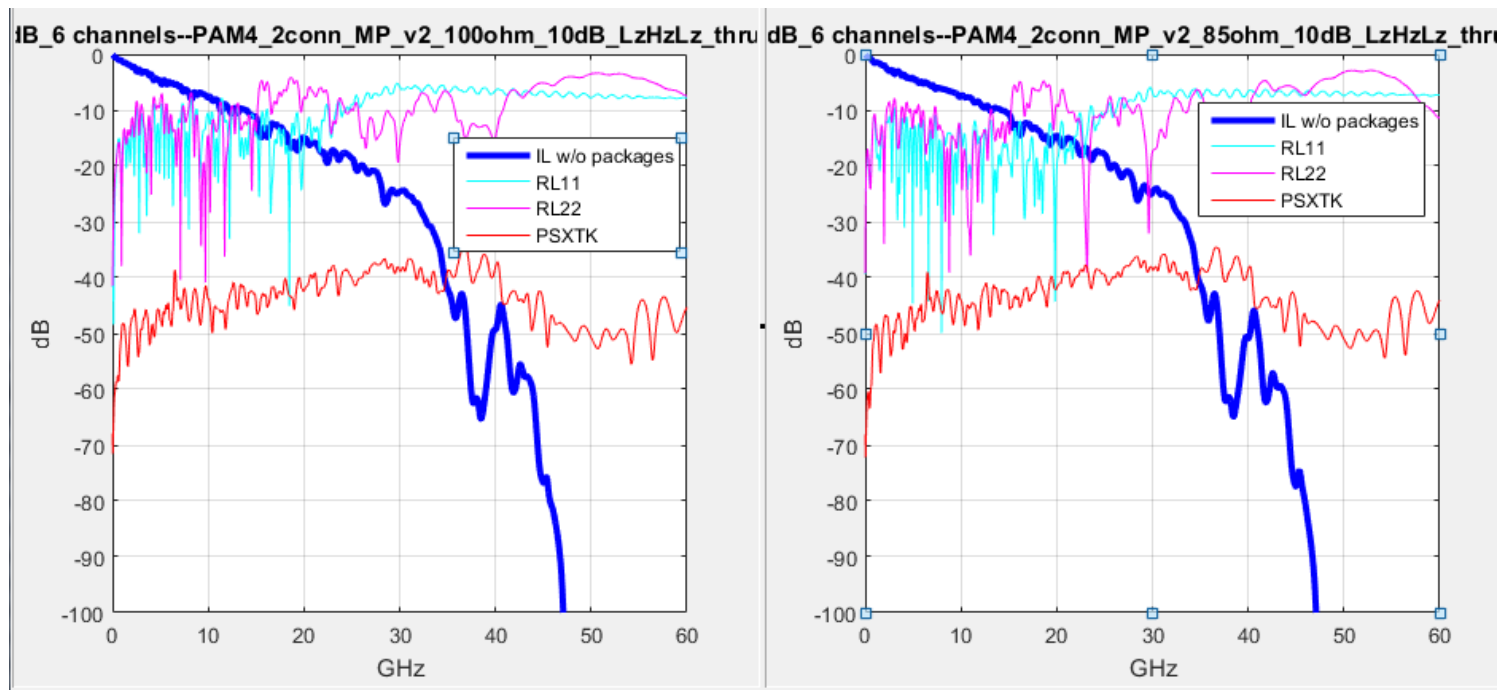
I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
Display frequency domain	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\COM50_{date}\	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	_CDAUI-8	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_TX_TERM	0	logical
T_r	1.20E-02	ns
T_r_filter_type	0	logical
T_r_meas_point	0	logical

Non standard control options		
INC_PACKAGE	1	logical
IDEAL_RX_TERM	0	logical
INCLUDE_CTL	1	logical
INCLUDE_TX_RX_FILTER	1	logical
COM_CONTRIBUTION	0	logical

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm

Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

Example of Data 10 dB channel



Example of Data 30 dB channel

