Continued thoughts on PCS/FEC baseline

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IEEE 802.3cd ad-hoc conference call, June 22 2016

Background

- At the 802.3cd TF Meeting in Whistler it was agreed to adopt nicholl_3cd_01a_0516 as the basis for the 50GbE and 100GbE PCS and FEC architecture, with the exception of leaving the FEC lane count / distribution as TBD.

Motion #4: 1:42 p.m.
Move to adopt nicholl_3cd_01a_0516 as the basis for the 50GbE and 100GbE PCS and FEC architecture, with the exception of leaving the FEC lane count / distribution as TBD

- M: Gary Nicholl
- S: Dave Ofelt
- Technical (>=75%),
- Y: 67 N: 1 A: 12
- Results: passes 1:52 p.m.

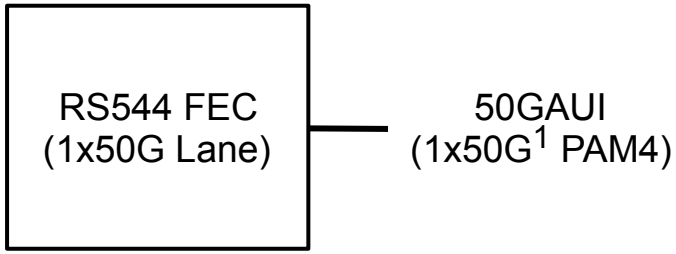
- We need to make a decision on the FEC lane count and distribution method in order to have a complete baseline proposal

FEC Options

- The FEC decision really comes down to whether we want to be able to run the RS544 FEC over 25Gb/s electrical (AUI) interfaces as well as 50Gb/s electrical (AUI) interfaces.
- The options being considered (using 50GbE as an example) are:
    1. 1x50G FEC lane (original nicholl_01a_0516 proposal)
    2. 2x25G FEC lanes /w bit muxing
    3. 2x25G FEC lanes /w symbol muxing
- Based on recent discussions there appears to be very little support for symbol muxing, so the decision we need to make is essentially between (1) and (2)
- A comparison between the different FEC options was provided in nicholl_3cd_02_0516

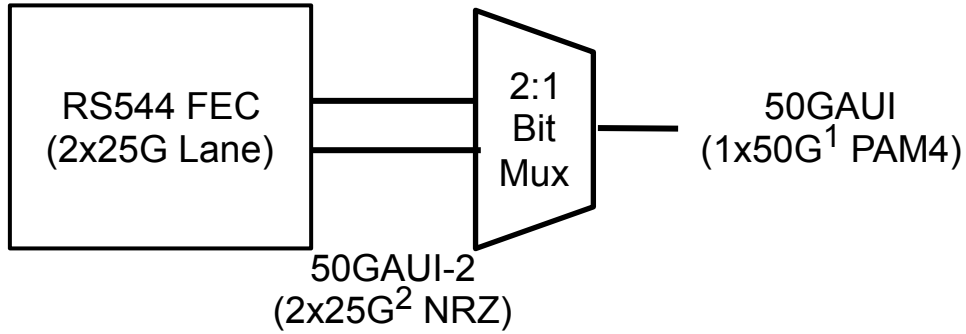
Note: All PMA blocks not shown for clarity.

FEC comparison re-cap



(1) 1x50G FEC Lane

- simplest architecture
- optimized for the volume application (single 50Gb/s lane end-to-end)
- can only be supported in chips with 50Gb/s serdes (may restrict some implementation choices in the short term)



(2) 2x25G FEC Lanes /w bit mux

- slightly more complex architecture (see backup), but not enough to be a deciding factor.
- may lock in permanent FEC performance hit in presence of burst errors (currently being analyzed, pre-coding may help)
- enables a broader range of implementation choices (e.g. FPGAs with 25Gb/s serdes)
- requires definition of additional 50GAUI-2 interface

1 = 53.125 Gb/s, 2 = 26.5625Gb/s

Summary

- The FEC choice essentially boils down to:
    1. 1x50G FEC lane
    2. 2x25G FEC lanes /w bit muxing
- Option (1) is the simpler of the two options, and the one that is optimized for the long term volume application (which is assumed to be based on a a single 50G lane end-to-end)
- Option (2) does enable a broader range of (short term) implementation options, if the impact of the bit muxing on the FEC performance can be addressed. However it adds a little more complexity (probably not a gating factor in itself), and requires the definition of new 25Gb/s AUIs running at the RS544 FEC rate.

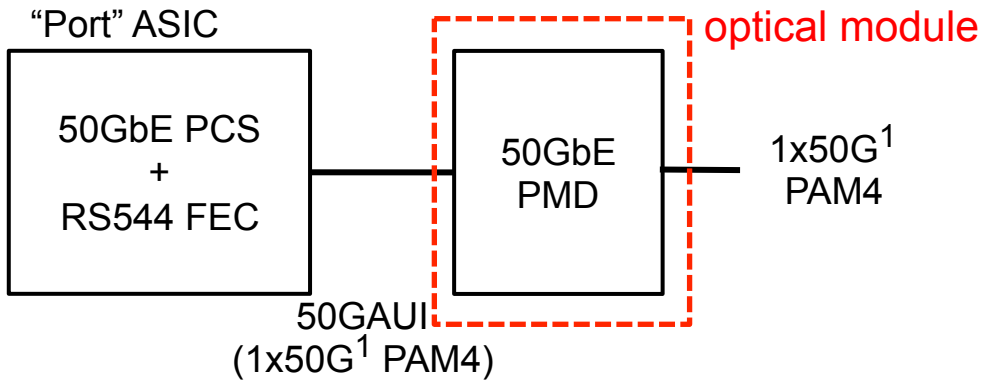
Backup

Ref: nicholl_3cd_01a_0516

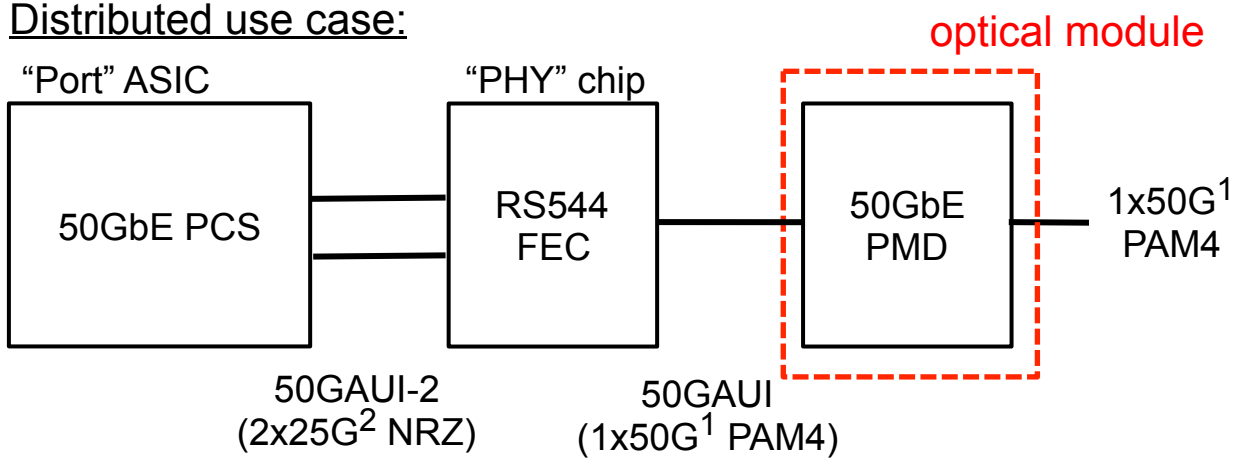
Note: PMA blocks not shown for clarity.

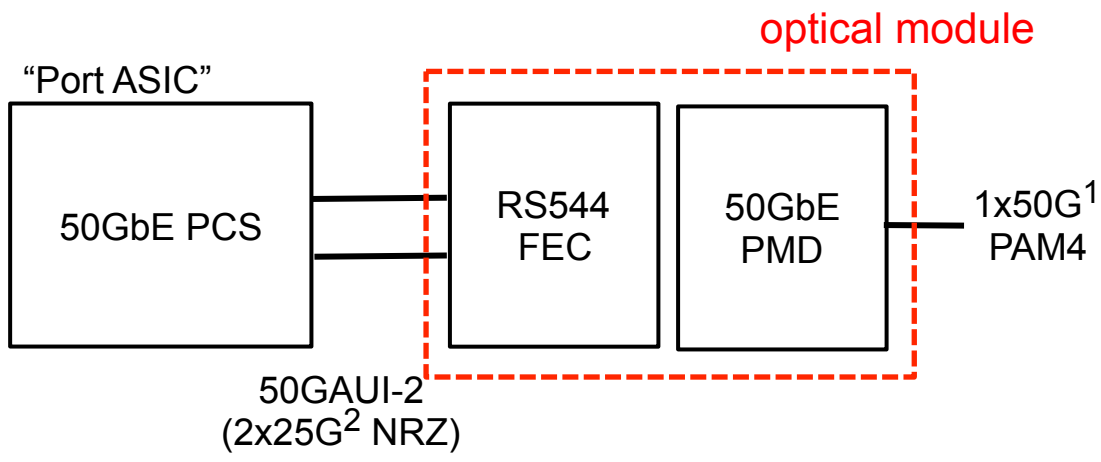
50GbE Use Cases (1x50G FEC lane architecture)

Integrated use case (long term, single lane optimized):



Distributed use case:

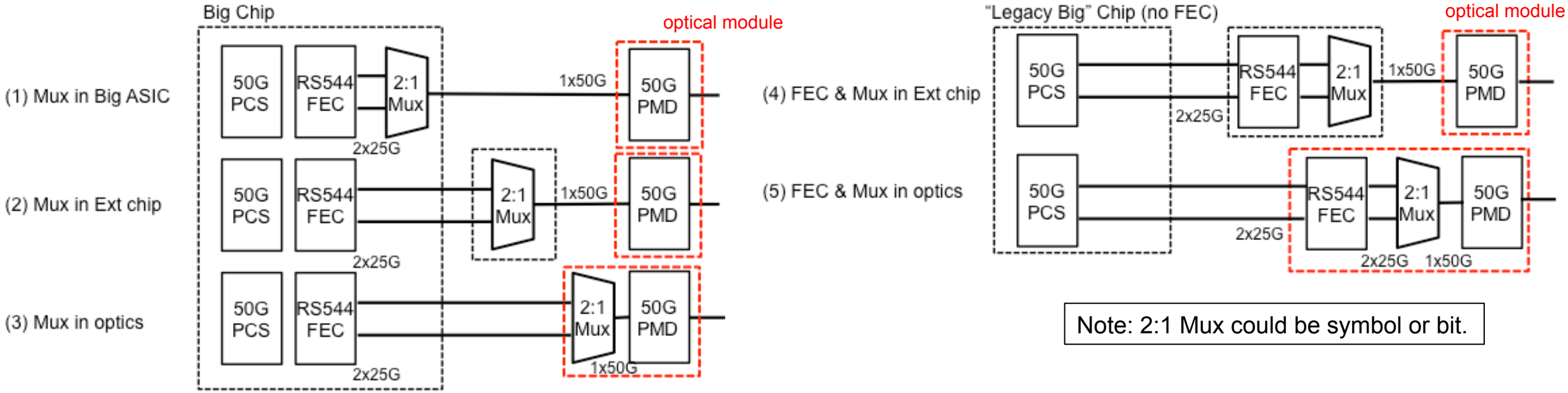




1 = 53.125 Gb/s, 2 = 25.78125Gb/s

Note: All PMA blocks not shown for clarity.

50GbE Use Cases (2x25G Lane FEC Architecture)

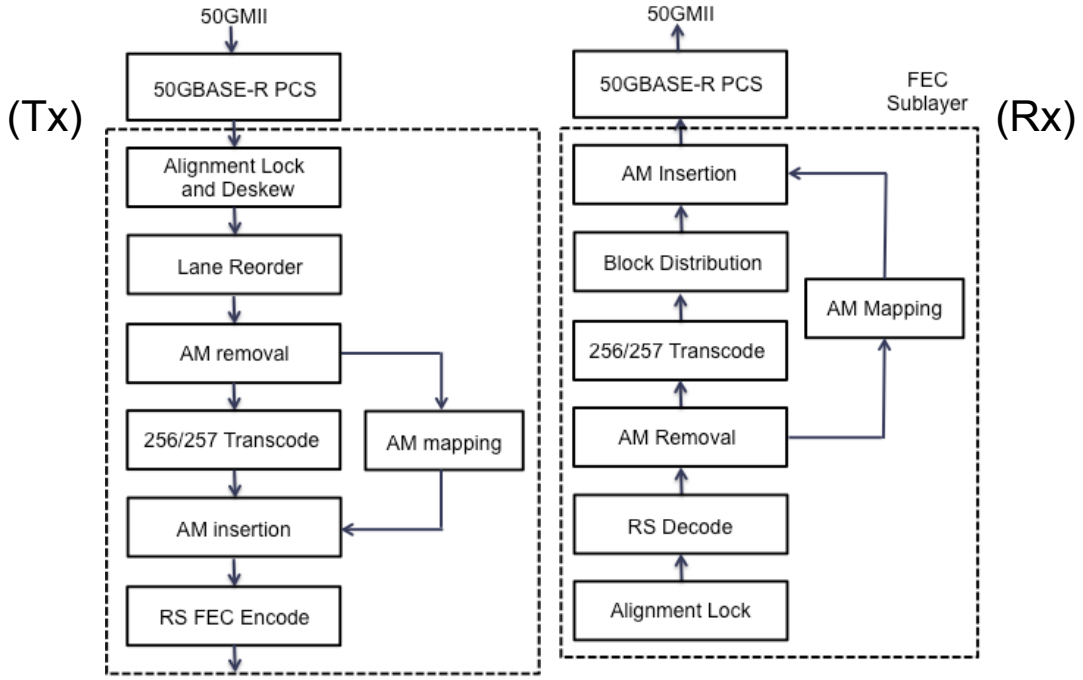


Note: 2:1 Mux could be symbol or bit.

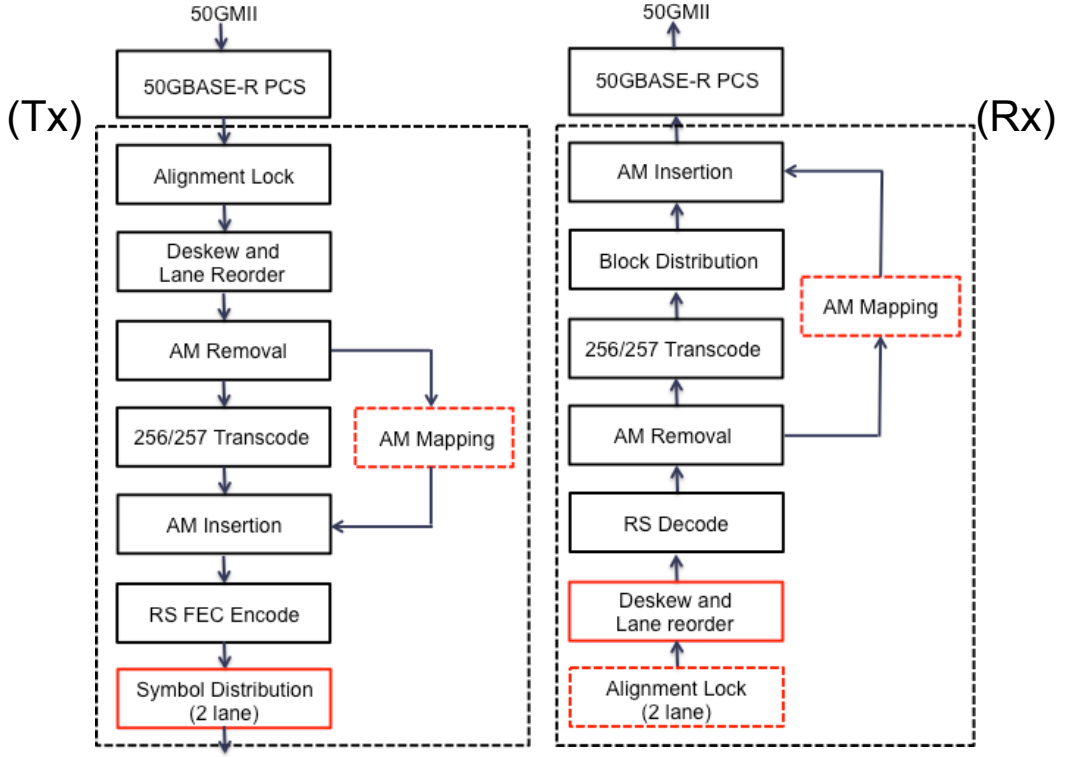
- (1) is the long term volume application, (2)-(5) are all transitory
- (1) contains distribution/deskew in the FEC and a 2:1 mux that is not technically necessary
- Use cases (2) and (3) are enabled by this 2x25G lane FEC architecture
- However it doesn't eliminate the need for an External FEC chip or FEC in optics - use cases (4) and (5)
  - in this regard it is no different to nicholl_3cd_01_0516

Changes to PCS/FEC (1x50G versus 2x25G FEC Lanes)

nicholl_3cd_01_0516 (1x50G FEC Lane)



2x25G FEC Lane Architecture



- No change to PCS. Minor changes to FEC sub-layer
- Changes are independent of symbol versus bit muxing
- No impact to latency
- Note: Changes to FEC sub-layer may be even less for 100GbE

Added functionality

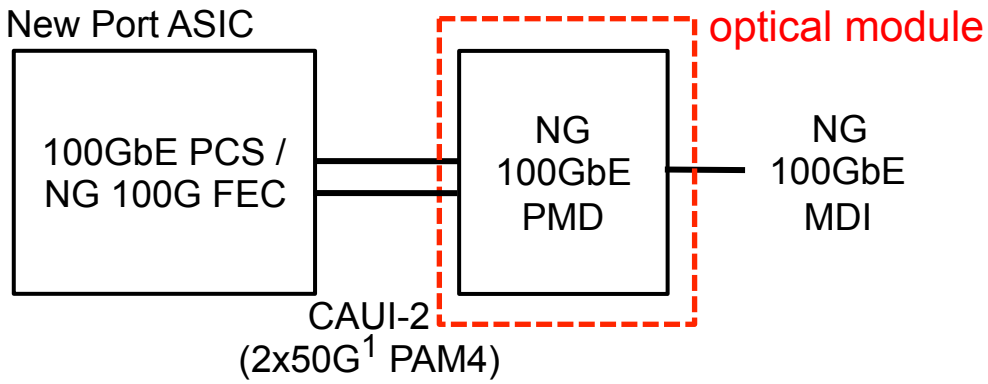
Changed functionality

Ref: nicholl_3cd_01a_0516

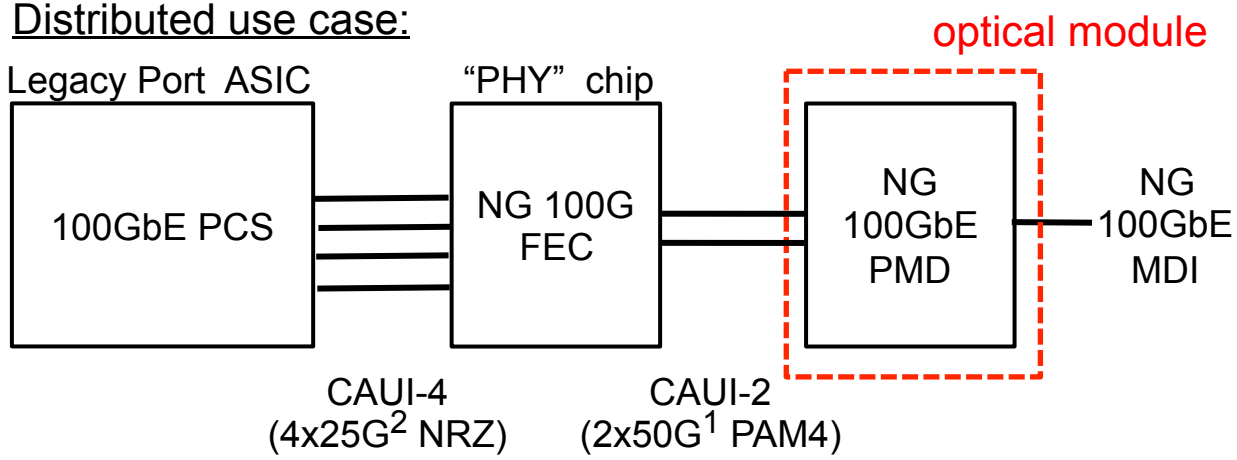
Note: PMA blocks not shown for clarity.

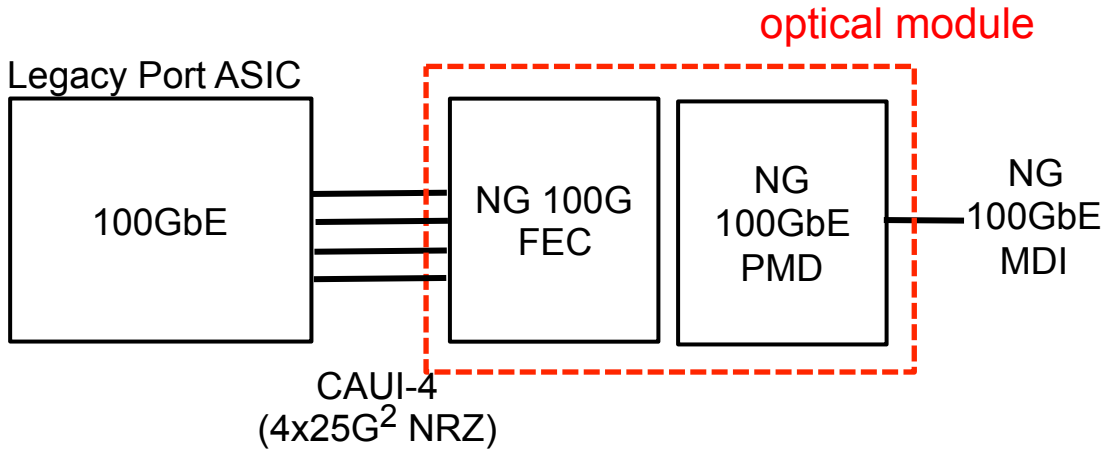
NG 100GbE Use Cases (2x50G Lane FEC architecture)

Integrated use case (long term, 2x50G lane optimized):



Distributed use case:

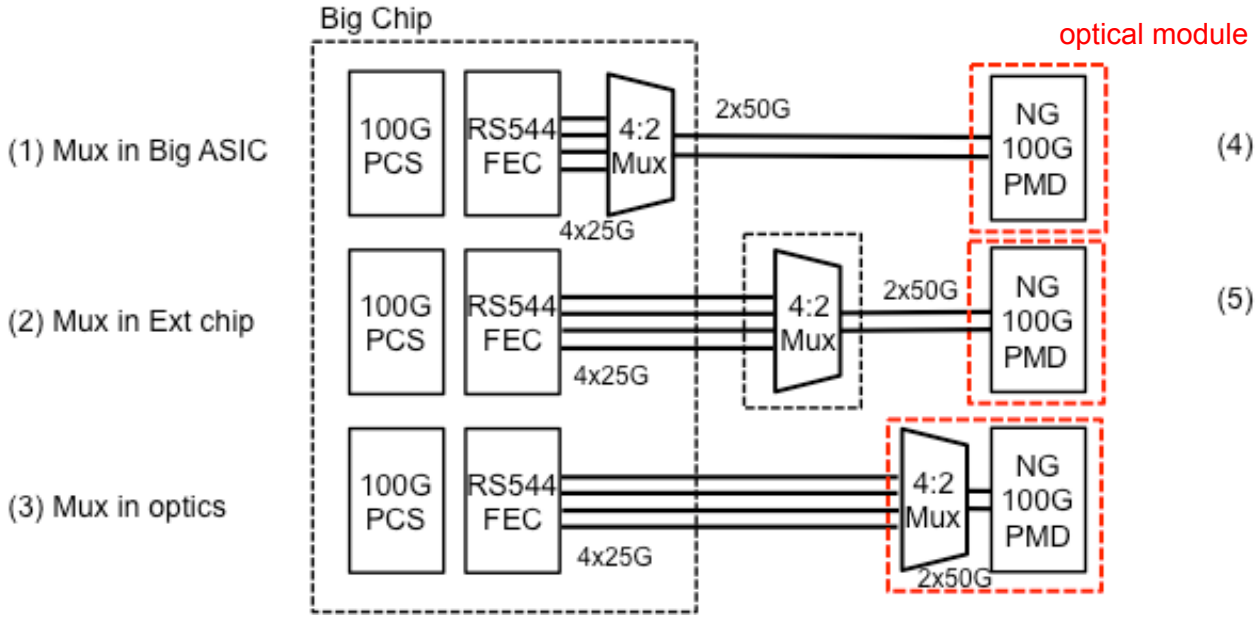


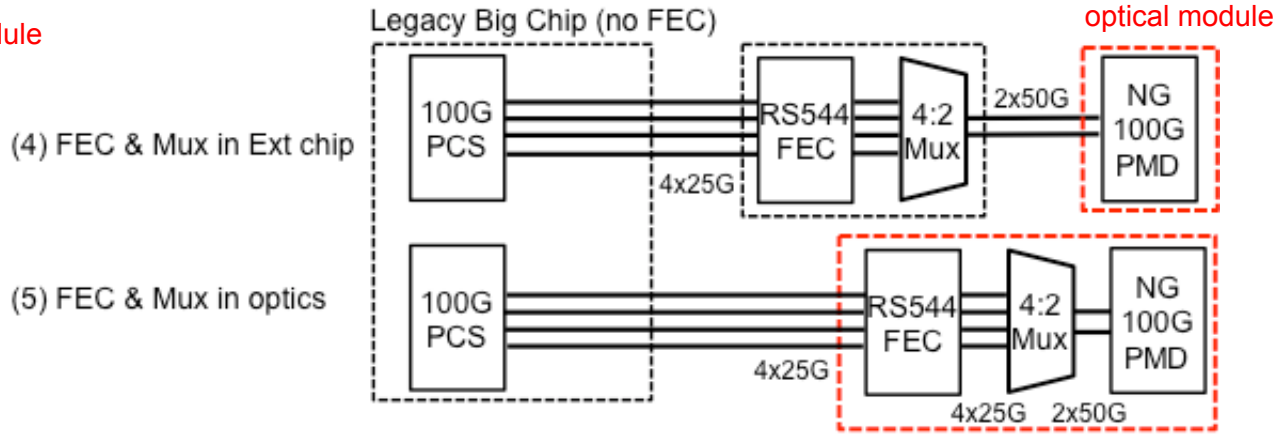


1 = 53.125 Gb/s, 2 = 25.78125Gb/s

Note: All PMA blocks not shown for clarity.

100GbE Use Cases (4x25G Lane FEC Architecture)



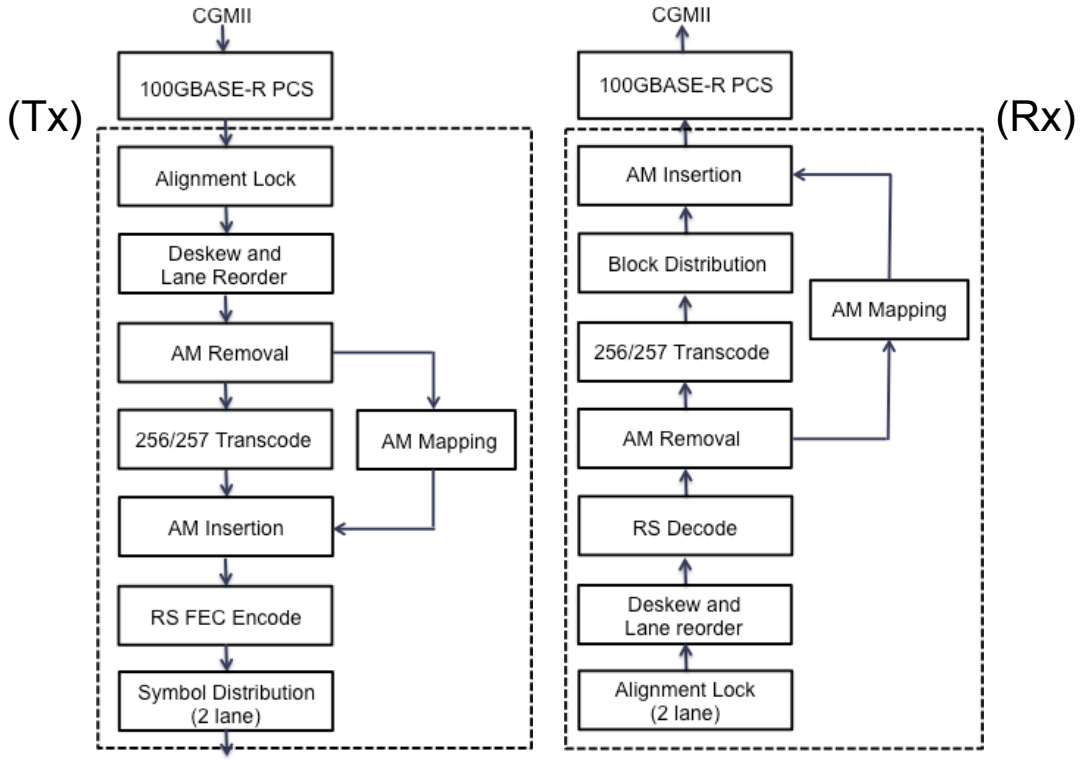


Note: 4:2 Mux could be symbol or bit.

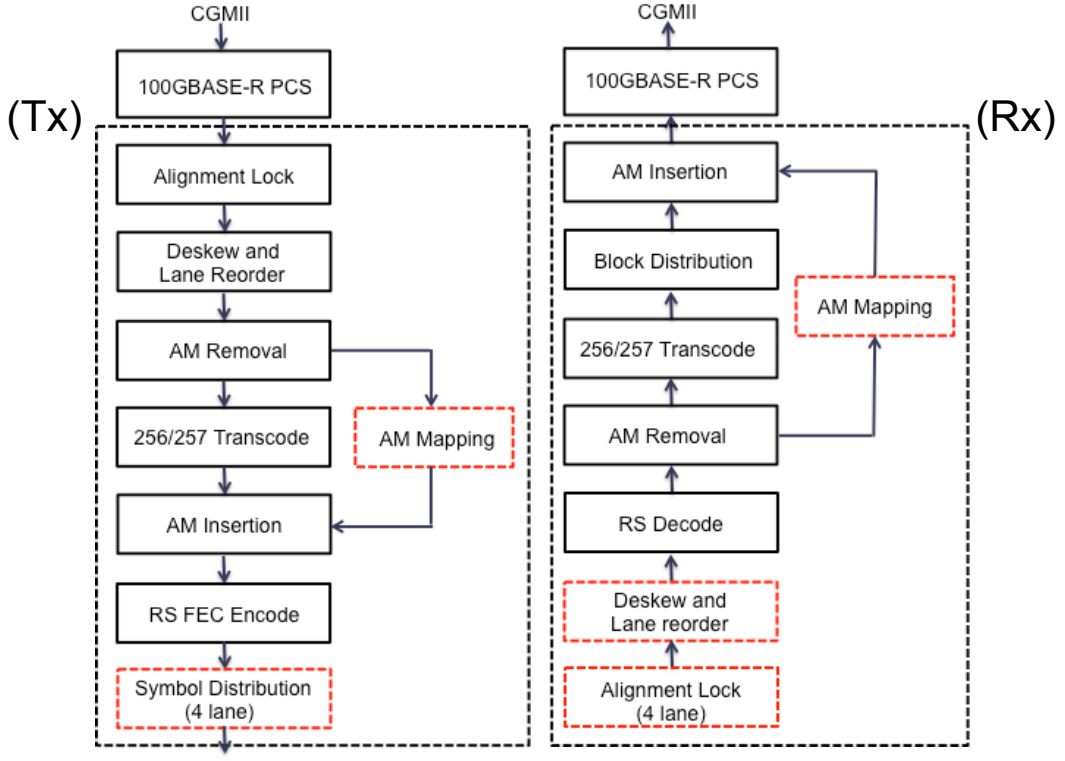
- (1) is the long term, volume application, (2)-(5) are all transitory
- (1) contains distribution/deskew in the FEC and a 4:2 mux that is not technically necessary
- Use cases (2) and (3) are enabled by this 4x25G lane FEC architecture
- However it doesn't eliminate the need for an External FEC chip or FEC in optics - use cases (4) and (5)
  - in this regard it is no different to nicholl_3cd_01_0516

Changes to 100G PCS/FEC (2x50G versus 4x25G FEC Lanes)

nicholl_3cd_01_0516 (2x50G FEC Lane)



4x25G FEC Lane Architecture



- Similar comments to 50GbE
- However in this case 4x25G FEC sub-layer is identical to 802.3bj Clause 91 !

Added functionality

Changed functionality