After alignment marker lock is achieved the two FEC lanes, all inter-lane Skew is removed as specified by the FEC alignment state diagram shown in Figure 91–9. The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns.

134.5.3.2 FEC Lane reorder

FEC lanes can be received on different lanes of the service interface from which they were originally transmitted. The FEC receive function shall order the FEC lanes according to the FEC lane number (see 134.5.2.6). The FEC lane number is defined by the sequence of alignment markers that are mapped to each FEC lane.

After all FEC lanes are aligned, deskewed, and reordered, the FEC lanes are multiplexed together in the proper order to reconstruct the original stream of FEC codewords.

134.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols.

The RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-6}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder shall indicate errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors that were not corrected, it ensures that for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure that rx_coded_0<1:0> corresponding to the second 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11. Setting rx_coded_0<1:0> to 11 as described causes the PCS to assign R_BLOCK_TYPE=E to the 66-bit block and decode its content as EBLOCK_R (see 49.2.13.2.1 and 49.2.13.2.3). This causes the PCS to discard all frames 64 bytes and larger that are fully or partially contained within the codeword.

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 134.6.6). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 134.6.1).

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds 6380, the Reed-Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms. As a result, the PCS sets hi_ber = true, which inhibits the processing of received packets. When Auto-Negotiation is supported and enabled, assertion of hi_ber causes Auto-Negotiation to restart.

The Reed-Solomon decoder may optionally provide the ability to signal a degradation of the received signal. The presence of this option is indicated by the assertion of the FEC_degraded_SER_ability variable (see 134.6.8). When the option is provided it is enabled by the assertion of the FEC_degraded_SER_enable variable (see 134.6.2).

When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the FEC. The Reed-Solomon decoder counts the total number of symbol errors detected in consecutive non-overlapping blocks of FEC_degraded_SER_interval (see 134.6.5) codewords. If the decoder determines that a codeword is uncorrectable, the number of symbol errors detected is increased by 16. When the number of symbol errors exceeds the threshold set in FEC_degraded_SER_activate_threshold (see 134.6.3), the FEC_degraded_SER bit (see 134.6.9) is set. At the end of each interval, if the number of symbol errors is less than the threshold set in FEC_degraded_SER_deactivate_threshold (see 134.6.4), the FEC_degraded_SER bit is cleared. If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is de-asserted then the FEC_degraded_SER bit is cleared.

134.5.3.4 Alignment marker removal

The first 257 message bits in every 1024th codeword is the vector am_rxmapped<256:0> where bit 0 is the first bit received. The specific codewords that include this vector are indicated by the alignment lock and deskew function (see 134.5.3.1).

The vector am_rxmapped shall be removed prior to transcoding.

134.5.3.5 256B/257B to 64B/66B transcoder

The 256B/257B to 64B/66B transcoder is identical to the transcoder for the 100GBASE-R RS-FEC sublayer defined in 91.5.3.5.

134.5.3.6 Block distribution

After the data has been transcoded, it shall be distributed to four PCS lanes, one 66-bit block at a time in a round robin distribution from the lowest to the highest numbered PCS lanes. The distribution process is shown in Figure 82–6.

134.5.3.7 Alignment marker mapping and insertion

The alignment marker mapping function compensates for operation of the lane reorder function (see 134.5.2.3) to derive the PCS lane alignment markers, am_rx_x<65:0> for x=0 to 3, from am_rxmapped<256:0> (see134.5.3.4).

The alignment markers shall be derived from am_rxmapped<256:0> in a manner that yields the same result as the following process.

Given i=0 to 1, k=0 to 12, and y=i+2k, am_rxpayloads is constructed from am_rxmapped as follows:.

— If (y < 25) then am_rxpayloads<i, (10k+9):10k> = am_rxmapped<(10y+9):10y>
— am_rxpayloads<1, 125:120> = am_rxmapped<255:250>

The one bit pad am_rxmapped<256> is ignored by the receiver.

For x=0 to 3, amp_rx_x<63:0> is constructed from am_rxpayloads as follows:

— amp_rx_0<63:0> = am_rxpayloads<0, 63:0>
— amp_rx_1<63:0> = am_rxpayloads<1, 63:0>
— amp_rx_2<63:0> = am_rxpayloads<0, 127:64>
— amp_rx_3<55:0> = am_rxpayloads<1, 119:64>
— amp_rx_3<57:56> = am_rxpayloads<0, 129:128>
— amp_rx_3<63:58> = am_rxpayloads<1, 125:120

amps_lock<*x*>
: Boolean variable that is set to true when the receiver has detected the location of the alignment marker payload sequence for a given lane on the PMA service interface, where *x* = 0:1.

fec_lane
: A variable that holds the FEC lane number (0 to 1) received on lane *x* of the PMA service interface when amps_lock<*x*> = true. The FEC lane number is determined by the alignment marker payloads in the 2nd position of the sequence based on the mapping defined in 134.5.2.6. The 48 bits that are in the positions of the known bits in the received alignment marker payload are compared to the expected values for a given payload position and FEC lane on a nibble-wise basis (12 comparisons). If no more than 3 nibbles in the candidate block fail to match the corresponding known nibbles on a given FEC lane, then the FEC lane number is assigned accordingly.

fec_lpi_fw
: Boolean variable that controls the behavior of the Transmit LPI and Receive LPI state diagrams. This variable is set to true when the local PCS is configured to use the fast wake mechanism and set to false otherwise. This variable shall always be set to true.

fec_optional_states
: Boolean variable that is always set to true to indicate that the optional states in the FEC synchronization state diagram in Figure 91–8 are implemented.

134.5.4.2.2 Functions

The functions are identical to those defined in 91.5.4.2.2.

134.5.4.2.3 Counters

This following counters are redefined from what is described in 91.5.4.2.3:

amp_counter
: This counter counts the 1 024 FEC codewords that separate the ends of two consecutive normal alignment marker payload sequences. A FEC codeword is 2 720 bits per FEC lane

134.5.4.3 State diagrams

The state diagrams are identical to those defined in 91.5.4.3.

134.6 RS-FEC MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the RS-FEC. If MDIO is implemented, it shall map MDIO control bits to RS-FEC control variables as shown in Table 134–1, and MDIO status bits to RS-FEC status variables as shown in Table 134–2, and if a separated PMA (see 45.2.1) is connected to the FEC service interface (e.g., if the RS-FEC and PCS are separated via a LAUI-2 interface) it shall map additional MDIO status bits to additional RS-FEC status variables as shown in Table 134–3.

The following subclauses define variables that are not otherwise defined, e.g., for use by state diagrams.

134.6.1 FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 91.5.3.3) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.101 (1.200.1).

Table 134–1—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable
FEC degraded SER enable	RS-FEC control register	1.200.4	FEC_degraded_SER_enable
FEC degraded SER activate threshold	RS-FEC degraded SER activate threshold register	1.284,1.285	FEC_degraded_SER_activate_threshold
FEC degraded SER deactivate threshold	RS-FEC degraded SER deactivate threshold register	1.286,1.287	FEC_degraded_SER_deactivate_threshold
FEC degraded SER interval	RS-FEC degraded SER interval register	1.288,1.289	FEC_degraded_SER_interval

Table 134–2—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	hi_ser
FEC degraded SER ability	RS-FEC status register	1.201.3	FEC_degraded_SER_ability
FEC degraded SER	RS-FEC status register	1.201.4	FEC_degraded_SER
FEC AM lock *x*, *x*=0 to 1	RS-FEC status register	1.201.8:9	amps_lock<*x*>
RS-FEC align status	RS-FEC status register	1.201.14	fec_align_status
FEC corrected codewords	RS-FEC corrected codewords counter register	1.202, 1.203	FEC_corrected_cw_counter
FEC uncorrected codewords	RS-FEC uncorrected codewords counter register	1.204, 1.205	FEC_uncorrected_cw_counter
FEC lane *x* mapping	RS-FEC lane mapping register	1.206	FEC_lane_mapping<*x*>
FEC symbol errors, FEC lanes 0 to 1	RS-FEC symbol error counter register, FEC lanes 0 to 1	1.210 to 1.213	FEC_symbol_error_counter_*i*

134.6.2 FEC_degraded_SER_enable

This variable enables the FEC decoder to signal the presence of a degraded SER when the ability is supported. When set to a one, this variable enables degraded SER signaling. When set to a zero, degraded SER signaling is disabled. Writes to this bit are ignored and reads return a zero if the FEC does not have the ability to signal the presence of a degraded SER. This variable is mapped to the bit defined in "Clause 45 Ref TBA" (1.200.4).

134.6.3 FEC_degraded_SER_activate_threshold

This variable controls the threshold used to set the FEC_degraded_SER as defined in 134.5.3.3. It is mapped to the registers defined in "Clause 45 Ref TBA" (1.284, 1.285).

Table 134–3—MDIO/RS-FEC status variable mapping for separated PMA

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
PCS align status	RS-FEC status register	1.201.15	align_status
BIP errors, PCS lanes 0 to 3	RS-FEC BIP error counter register, PCS lanes 0 to 3	1.230 to 1.233	BIP_error_counter_*i*
PCS lane *x* mapping	PCS lane *x* mapping register	1.250 to 1.253	lane_mapping<*x*>
Block *x* lock	RS-FEC PCS alignment status 1 register	1.280	block_lock<*x*>
Lane *x* aligned	RS-FEC PCS alignment status 3 register	1.282	am_lock<*x*>

134.6.4 FEC_degraded_SER_deactivate_threshold

This variable controls the threshold used to clear the FEC_degraded_SER as defined in 134.5.3.3. It is mapped to the registers defined in "Clause 45 Ref TBA" (1.286, 1.287).

134.6.5 FEC_degraded_SER_interval

This variable controls the interval used to set and clear the FEC_degraded_SER bit as defined in 134.5.3.3. It is mapped to the registers defined in "Clause 45 Ref TBA" (1.288, 1.289).

134.6.6 FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.102 (1.201.1).

134.6.7 hi_ser

This variable is defined when the FEC_bypass_indication_ability variable is set to one. When FEC_bypass_indication_enable is set to one, this bit is set to one if the number of RS-FEC symbol errors in a window of 8 192 codewords exceeds the threshold (see 91.5.3.3) and is set to zero otherwise. This variable is mapped to the bit defined in 45.2.1.102 (1.201.2).

134.6.8 FEC_degraded_SER_ability

The FEC decoder may have the option to signal the presence of a degraded SER (see 134.5.3.3). This variable is set to one to indicate that the FEC decoder has the ability to signal the presence of a degraded SER. This variable is set to zero if this ability is not supported. It is mapped to the register bit defined in "Clause 45 Ref TBA" (1.201.3).

134.6.9 FEC_degraded_SER

When FEC_degraded_SER_enable is asserted, this variable signals the presence of a degraded SER as defined in 134.5.3.3. This variable is mapped to the register bit defined in "Clause 45 Ref TBA" (1.201.4)

134.7 Protocol implementation conformance statement (PICS) proforma for Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs[7]

134.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

134.7.2 Identification

134.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1— Required for all implementations. NOTE 2— May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

134.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	

[7] *Copyright release for PICS proformas*: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

134.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
RS-FEC	Supports 50GBASE-R RS-FEC functionality	134.1.1		M	Yes [ ]
*MD	MDIO capability	45, 134.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	134.5.3.3	Capability is supported	O	Yes [ ] No [ ]
*FDD	Support for optional FEC degraded SER detection	134.5.3.3	FEC decoder can optionally detect a FEC degraded SER at a programmable threshold	O	Yes [ ] No [ ]

134.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sub-layer for 50GBASE-R PHYs

134.7.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	Skew tolerance	134.5.2.2	Maximum Skew of 49 ns between PCS lanes and a maximum Skew Variation of 400 ps.	M	Yes [ ]
TF2	Lane reorder	134.5.2.3	Order the PCS lanes according to the PCS lane number	M	Yes [ ]
TF3	64B/66B to 256B/257B transcoder	134.5.2.5	tx_xcoded<256:0> constructed per 134.5.2.5	M	Yes [ ]
TF4	257-bit block transmission order	134.5.2.5	First bit transmitted is bit 0	M	Yes [ ]
TF5	Alignment maker mapping	134.5.2.6	Map to am_txmapped<256:0> per 134.5.2.6	M	Yes [ ]
TF6	Pad value	134.5.2.6	Set to 0 or 1 in an alternating pattern	M	Yes [ ]
TF7	Alignment marker insertion	134.5.2.6	First 256 message bits to be transmitted from every 1024th codeword	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
TF8	Alignment marker insertion point	134.5.2.6	First 257-bit block inserted after am_txmapped corresponds to the four 66-bit blocks received on PCS lanes 0, 1, 2, and 3 that immediately followed the alignment marker on each respective lane	M	Yes [ ]
TF9	Reed-Solomon encoder	134.5.2.7		M	Yes [ ]
TF10	Symbol distribution	134.5.2.8	Distributed to 2 FEC lanes, one 10-bit symbol at a time in a round robin distribution from the lowest to the highest numbered FEC lane	M	Yes [ ]

134.7.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	134.5.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder	134.5.2.3	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	Reed-Solomon decoder for RS(544,514)	134.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword.	M	Yes [ ]
RF4	Reed-Solomon decoder	134.5.3.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error indication function	134.5.3.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords.	M	Yes [ ]
RF6	Error monitoring while error indication is bypassed	134.5.3.3	When the number of symbols errors in a block of 8 192 codewords exceeds K, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]
RF7	Symbol error threshold for RS(544,514)	134.5.3.3	K=6380	BEI:M	Yes [ ] N/A [ ]
RF8	FEC degraded SER detection	134.5.3.3	FEC decoder can optionally detect a FEC degraded SER at a programmable threshold	FDD:M	Yes [ ] N/A [ ]
RF9	Alignment marker removal	134.5.3.4	am_rxmapped removed prior to transcoding	M	Yes [ ]
RF10	256B/257B to 64B/66B transcoder	134.5.3.5	rx_coded_j<65:0>, j=0 to 3 constructed per 134.5.3.5	M	Yes [ ]