Jitter considerations for 100GAUI-2 with 100GBASE-DR

(comments i-61 and i-115)

Adee Ran, Intel

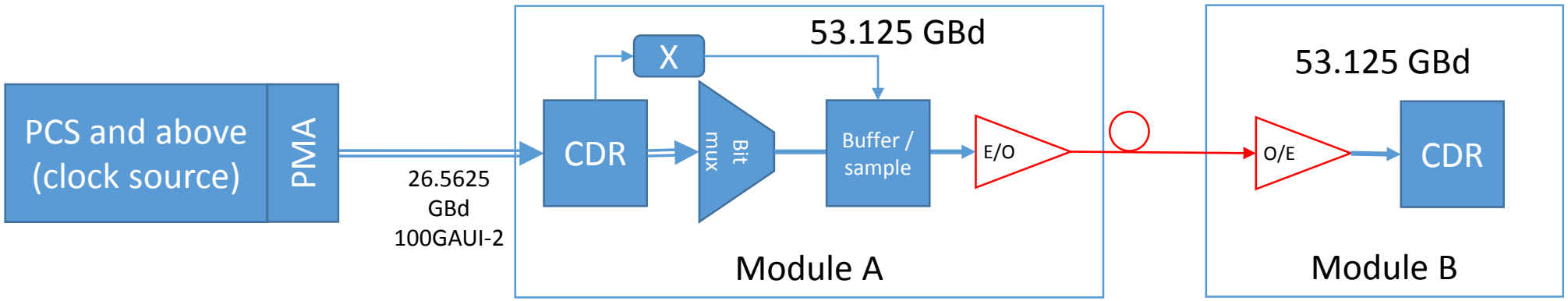
Piers Dawe, Mellanox

Supporters

… Not a simple problem

- Involves low frequency jitter which is seldom measured
- And a combination of high-end components from multiple vendors, not readily available for testing and showing the problem
- Effects may take a long time to occur

The system in question



So far we have discussed two cases:

1. Module A has a simple “clock forward” in box X – no buffering, optical samples have the same time jitter as electrical samples
2. Module A has a “cleaning PLL” in box X that reduces jitter on optical signal; jitter in electrical signal is tracked; frequency difference handled by buffering

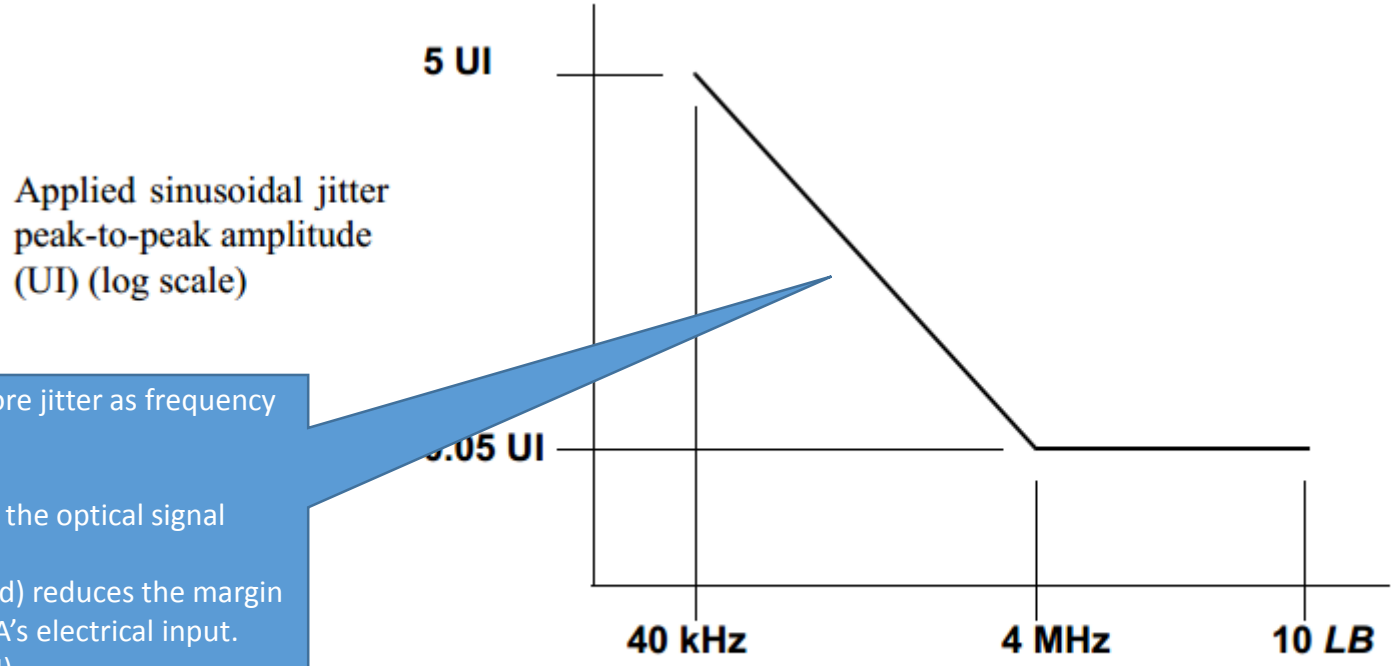
What is the maximum LF jitter we can expect?

- The PCS signaling rate is bounded within ±100 PPM from the nominal value
- Drifting between edges of the ±100 PPM region is technically allowed
- Due to integration, frequency of drift affects phase jitter per the jitter mask (20 dB/decade)
  - So slower drift causes larger jitter in UI
  - If frequency drift is sinusoidal with period T, then the maximum drift in UI is

$$\int_0^{T/2} \Delta f_{max} \sin\left(2\pi \frac{t}{T}\right) dt = \frac{\mathrm{T} \cdot \Delta f_{max}}{\pi}$$

- Numerical example (with 26.5625 GBd)
  - ±100 PPM at 4 MHz causes ~0.2 UI PtP
  - ±100 PPM at 4 kHz causes ~200 UI PtP
- Note that this is 4x of the SRS value at this frequency – so can be viewed as an extreme case… we don't know if it actually happens

Jitter tolerance stress



Module A's CDR is expected to track more jitter as frequency decreases…

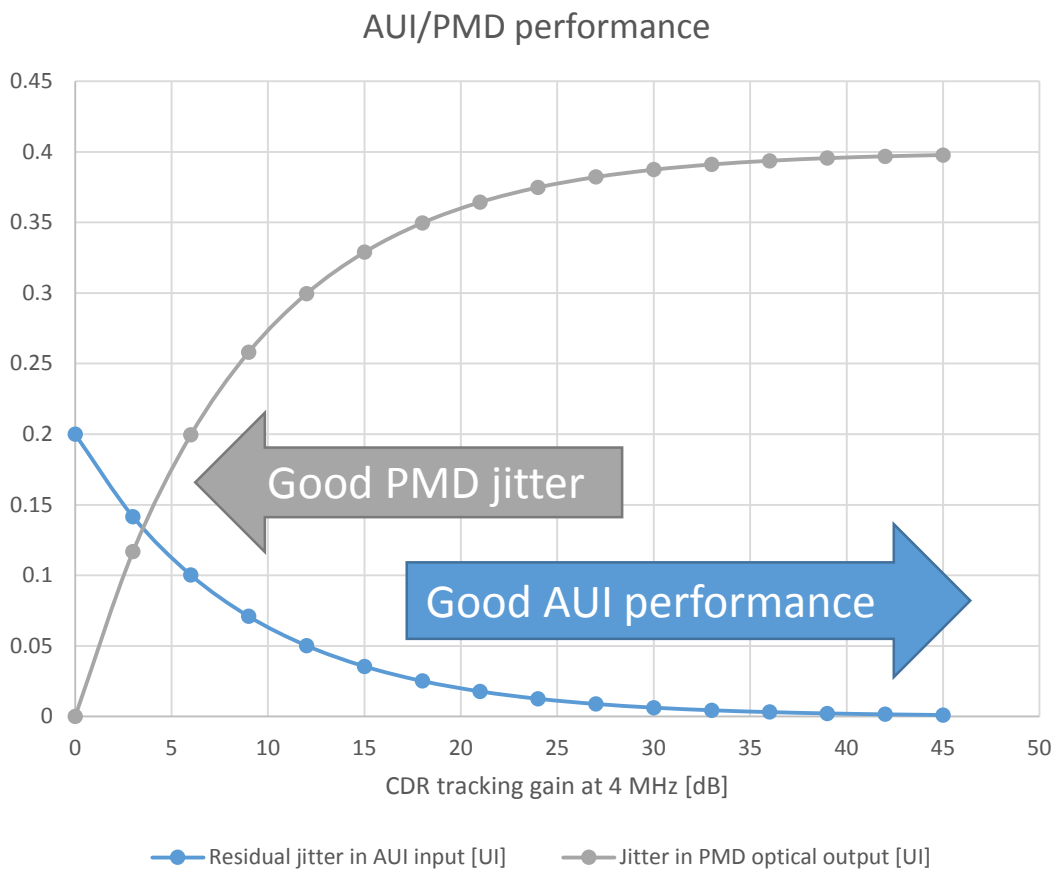
Whatever is tracked is passed on to the optical signal

The residual jitter (whatever isn't tracked) reduces the margin for correct data recovery in module A's electrical input.
(so must be << 1 UI)

Figure 121–7—Illustration of the mask of the sinusoidal component of jitter tolerance

How does module A handle jitter?

- Module A CDR is assumed to track -3 dB at 4 MHz ➔ jitter on its clock is ~29%*0.2=0.06 UI. But at the optical side every UI is half the time ➔ 0.2*0.29*2 ≈ 0.117 UI at 53.125 GBd.
- In lower frequencies/larger jitter combinations, module A will pass almost all of the jitter to the optical signal.
  - For example, almost the full 200 UI PtP at 4 KHz!
  - Note that the output jitter measured with a 4 MHz CRU will be similar across frequencies
- If module A has CDR bandwidth much larger than assumed, and no cleaning PLL, it may track all the jitter!
  - In that case it will have up to 0.4 UI of jitter on the optical signal at 4 MHz (twice of the incoming jitter)
  - In lower frequencies the tracking will be almost the same ➔ 2x the input jitter after CRU filtering
  - It may be difficult to pass TDECQ this way… perhaps discouraging large BW (tradeoff between AUI sensitivity and PMD output jitter)



Can a “cleaning PLL” help?

- If the recovered clock (tracking -3 dB) is used to drive the PMD, it will cause ~0.117 UI of optical jitter at 4 MHz – still above SRS value and burdening TDECQ
- If the module includes a “cleaning PLL”, it could reduce the optical jitter, but require buffering of incoming bits.
  - Required buffer length is theoretically infinite! ➔Passing TDECQ with any compliant input jitter is impossible
  - Implementations may handle this in various ways; likely not test TDECQ with all the LF jitter allowed
  - Low enough frequency jitter will be passed to module B with 2x the UI value

How does module B handle jitter?

- The CDR on the optics side of Module B is also assumed to track -3 dB at 4 MHz.
- Faced with 0.117 UI of jitter at 4 MHz (more stress than in SRS) it will track 0.034 UI, leaving 0.083 UI as residual jitter.
  - In lower frequencies it will track better, leaving the same residual jitter.
- Faced with 0.4 UI of jitter at 4 MHz (if Module A has higher bandwidth) it will track 0.117 UI and leave 0.283 UI as residual jitter.
- The biggest issue for module B is when module A has both *high CDR BW* and *large jitter on its AUI input signal*, which is then fed through.
  - This can happen!
  - The effect is bounded at 0.283 UI of residual jitter, which is a lot (more than SRS)
- At lower frequencies, both input jitter and tracking gain scale together
  - Residual jitter stays the same

How will this problem manifest itself?

- Say module A has very high AUI CDR bandwidth
  - There is no specification preventing this
- If that module's optical output is tested without full jitter stress on the AUI, it may pass TDECQ
  - Note that TDECQ does not specify minimum length of measurement, so may be agnostic to changes in frequency
- If that module is plugged into a host with high jitter, it will pass that jitter to module B
- With strong input jitter, module B will have high residual jitter
- Residual jitter has low enough frequency that it may affect a whole codeword
  - This will significantly reduce coding gain and make uncorrectable errors more common

How can this problem be solved?

- Reduce host low frequency jitter
  - Will improve both optical jitter and AUI sensitivity
  - For that, we need to limit the host's AUI output jitter by using a lower frequency CRU
- Alternative (implicitly assumed in another comment): require a cleaning PLL in the module
  - Not obvious from the standard text
  - Difficult to implement; may break link if jitter is too high
  - Difficult to verify with current tests
- Alternative: do nothing
  - Ignore a complex problem that may cause intermittent errors in the field

Summary

- The problem does not require cleaning PLL
  - Although it could be used for improving PMD jitter, mitigating the problem
- The problem is not specific to low frequency jitter
  - It is simple to demonstrate at 4 MHz
  - And its effect is bounded
- The problem may cause degradation of FEC performance
- Module A has a tradeoff between AUI input performance and optical jitter/TDECQ
  - The tradeoff would be less painful if the AUI CDR tracking requirements are loosened
- Changing the CRU BW in the host AUI measurement seems to be simplest and safest