Feasibility of 50GE Low-latency Schemes

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Introduction

- **50GE low-latency link have been discussed in multiple presentations:**
  - [1] 50G, 100G & 200G SERVER CONNECTIVITY
  - [2] Breakout applications and impacts on objectives for 50/200G Ethernet
  - [3] No-FEC Link for 50GE
  - [4] Low-latency Schemes for 50GE
- **[4] described two potential schemes:**
  - No-FEC C2M and C2C
  - Lower-latency FEC

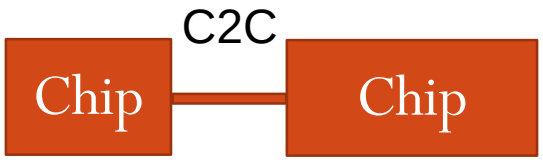
  This presentation is to provide some updates on these schemes.

No-FEC C2M and C2C Review

- What does this mean?
  - BER is lower than 1e-12 for short-reach C2M/C2C, so no FEC is needed.
- What does it look like?
  - With active cables:

  - With repeaters:

  - Short-reach chip to chip:



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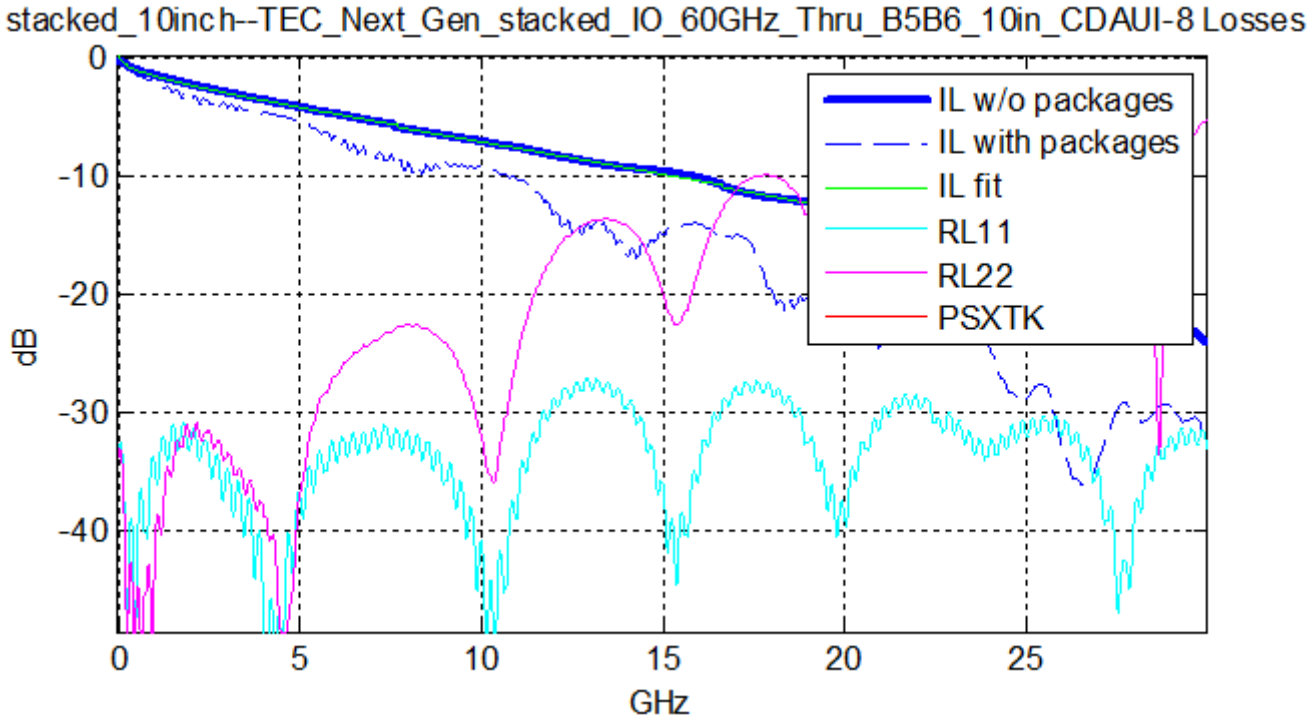
No-FEC C2M and C2C

- Is no-FEC feasible?
  - Quickly tried a simulation.
  - Not meant to discuss PMD architecture, qualify channels, or define PMD parameters in study group.
  - The purpose is to share some preliminary simulation results by using a common tool so the study group can have basic ideas **whether low-latency/no-FEC is technically feasible**.
- Setup:
  - COM tool for 802.3bs C2C.

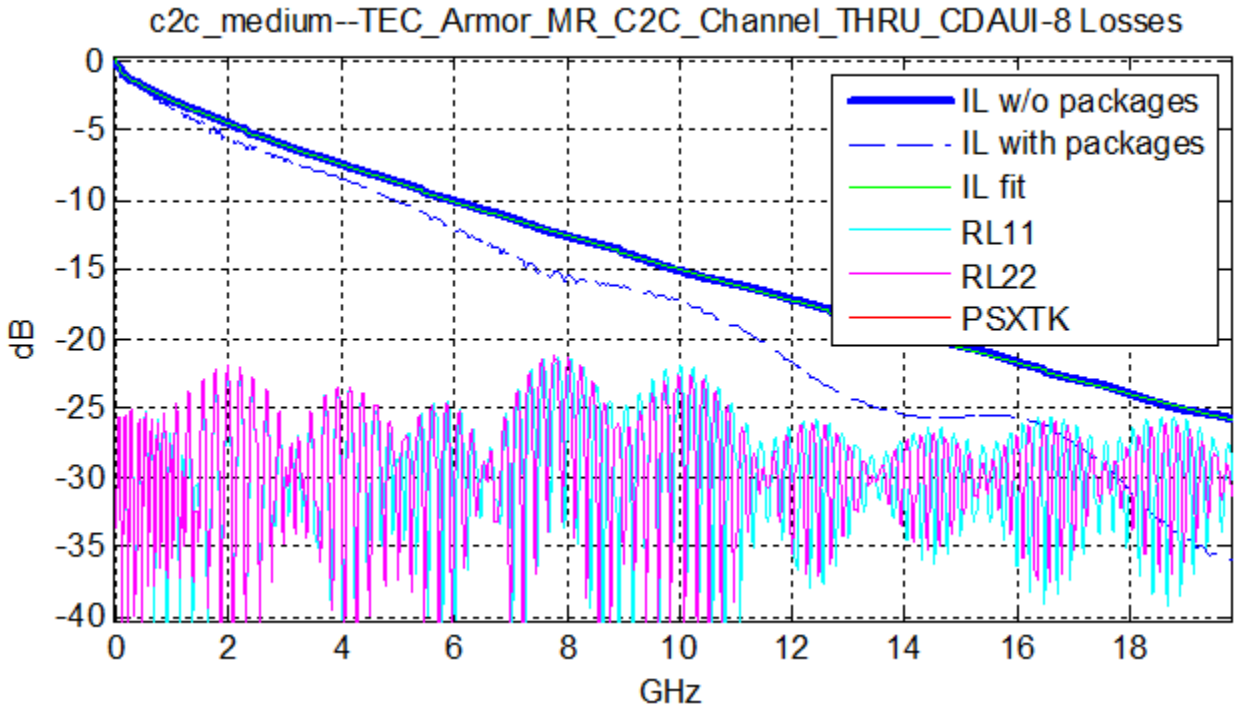
No-FEC C2M and C2C

- Channel 1: Next generation 28Gb/s press-fit stacked IO, 10 inch host
  - 9dB IL at 12.89 GHz.
  - Added one FEXT channel



No-FEC C2M and C2C

- Channel 2: shanbhag_02_0914.pdf
  - 18.2dB IL at 12.89 GHz.
  - Added one FEXT channel



No-FEC C2M and C2C

DER_0	COM Parameters	COM for Channel 1		COM for Channel 2	
		Z_p=12mm	Z_p=30mm	Z_p=12mm	Z_p=30mm
1e-12	Default	1.7dB	0.8dB	1.6dB	0.8dB
1e-12	SNR_TX=33dB	2.8dB	1.7dB	2.6dB	1.6dB
1e-7	Default	3.5dB	2.9dB	4.1dB	3.2dB

- COM threshold is set to 2dB. SNR_TX and other potential improvements on package, jitter, CTLE, and channel need to be studied and justified. healey_3bs_01_0315.pdf
- Lower-latency FEC can be used to relax PMD requirement. For example, DER_0 can be set to 1e-7.
- F_b is set to 25.78125 GHz for 1e-12 DER, and 26.5625GHz for 1e-7 DER.
- Simulation results seem encouraging.

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Lower-latency FEC

- A lower-latency FEC, RS(272,257,t=7,m=10), was presented in [4].
- This table shows DER requirement and latency of more FEC candidates. DER is set to achieve FLR equivalent to 1e-12 BER.

FEC	"a"=0.5	Precoding	"a"=0	Latency
RS(272,257), KS4?	2.4e-5	1.8e-5	2.0e-4	~99ns
RS(181,172)	1.0e-7	2.2e-6	4.8e-5	~65ns
RS(136,129)	4.4e-9	1.1e-7	1.6e-5	~49ns
RS(271,257)	2.4e-5	1.8e-5	2.0e-4	~99ns
RS(544,514), KP4	3.1e-4	2.0e-4	8.2e-4	~198ns
RS(528,514), KR4	1.1e-5	9.0e-6	1.0e-4	~169ns

- Decoding latency can be reduced to some extent by increasing complexity.
- RS(272,257), RS(181,172), or RS(136,129) can be added to KP4 implementation with negligible cost, and achieves 1/2, 1/3, or 1/4 of KP4 latency.
- RS(272,257) DER requirement for 1e-12 BER is similar to KR4 FEC, but runs at KP4 clock rate.
- RS(272,257) DER for electrical link here is 1e-5, same as 802.3bs C2C/C2M and 802.3bj PAM4.
- RS(136,129) works when there is not much error propagation.
  - It can carry FEC protected control bits for adaptive TX FIR to enable no-DFE solution.

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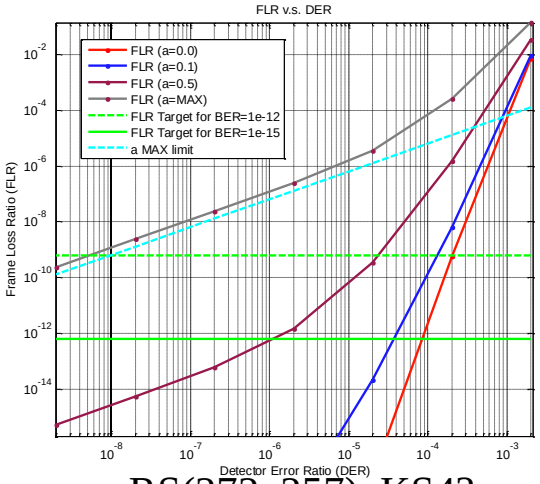
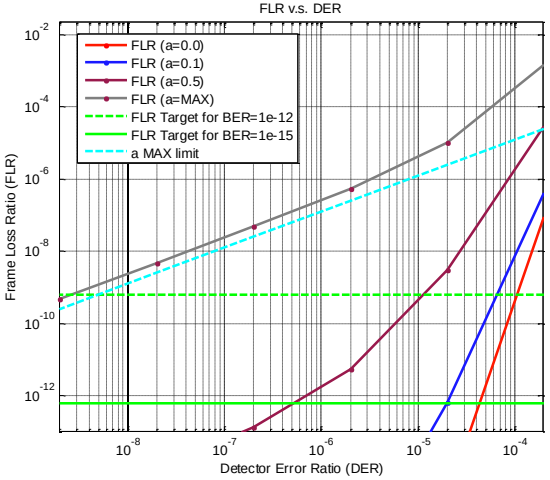
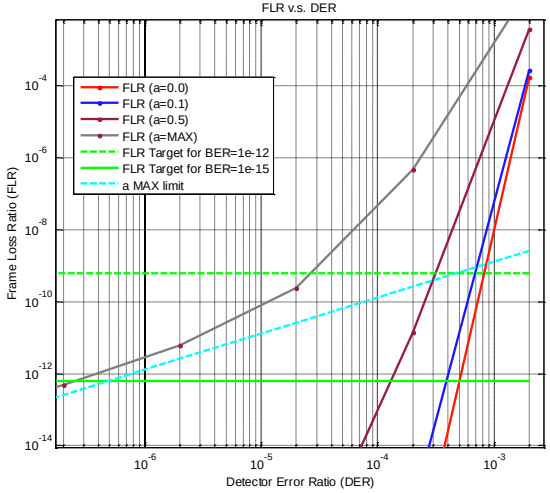
FEC Performance on Electrical Link



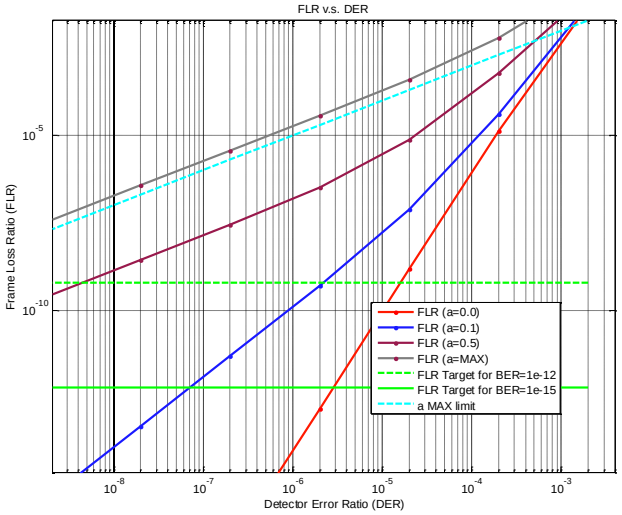
RS(272, 257), KS4?



RS(528, 514), KR4



RS(544, 514), KP4



RS(136, 129)

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An Example of Low-latency Schemes

Schemes	FEC	FEC Latency (ns)	DER Target	F_b (GHz)	COM for Channel 1 (dB)			
					Default Setting		TX_SNR=33dB	
1	No	0	1e-12	25.78125	1.7	0.8	2.8	1.7
2	RS(272,257)	99	1e-5	26.5625	**5.2**	**4.5**	-	-
3	RS(181,172)	65	1e-6	26.5625	**4.3**	**3.6**	-	-
4	RS(136,129)	49	1e-7	26.5625	**3.5**	**2.9**	-	-

- Use C2C COM simulation as an example.
- Lower-latency FEC can be used to get rid of repeaters, or relax PMD/channel requirements.
- The same method can be applied to C2M.

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Conclusions

- **Conclusions:**
  - Low-latency link on copper cable is feasible.
    - No-FEC C2M and C2C
      - No FEC latency.
    - Lower-latency FEC
      - Easy to be added.
- **Proposal:**
  - Adopt low-latency link (FEC latency less than 100ns) as an objective.

Thanks!