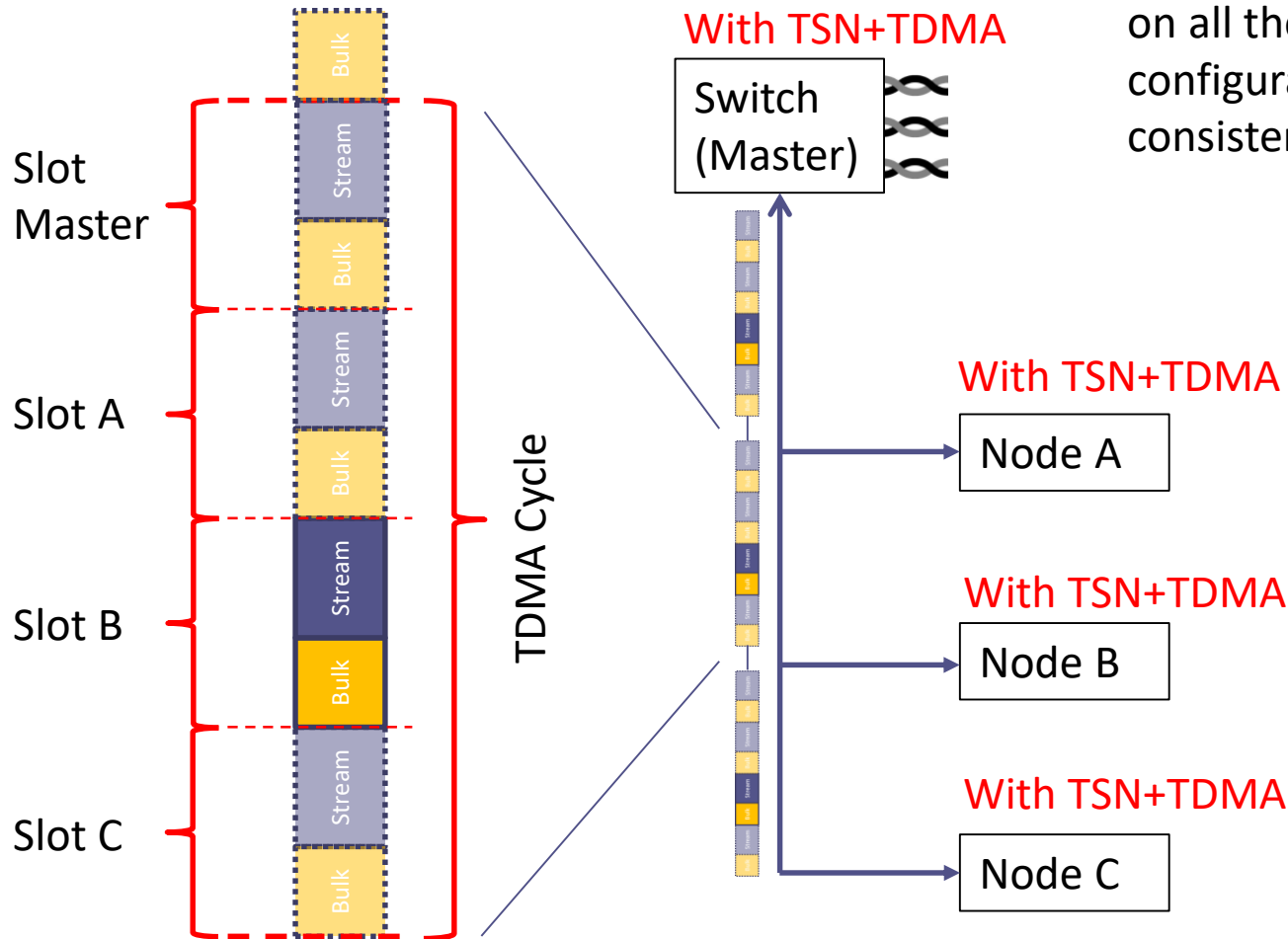# Canova Tech

The Art of Silicon Sculpting

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IEEE802.3cg TF

PHY-Level Collision Avoidance – Comparison with TDMA

September 8th, 2017
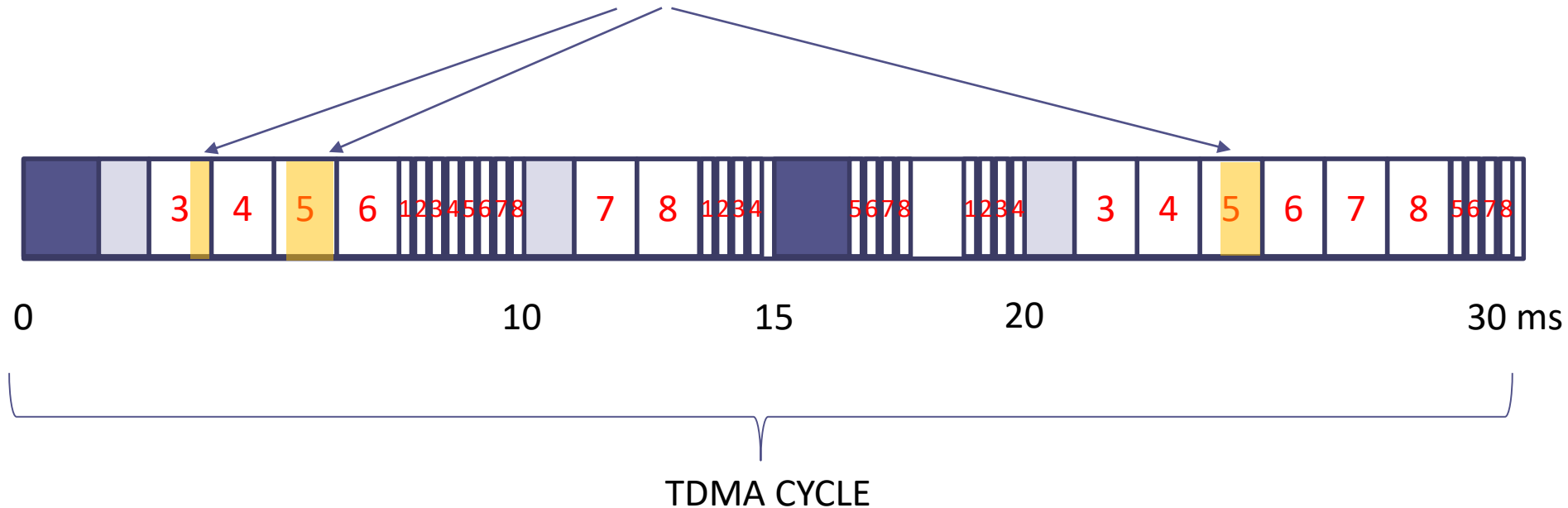
TSN + TDMA applied to 10M SPE multidrop

TSN+TDMA is required to run on all the nodes and configuration shall be consistent across the nodes

Slot Master

Slot A

Slot B

Slot C

TDMA Cycle

With TSN+TDMA

Switch (Master)

With TSN+TDMA

Node A

With TSN+TDMA

Node B

With TSN+TDMA

Node C

Example: design of TDMA cycle

Example slots usage (8 nodes network)

Partially used time slots (unused time is wasted)
e.g. random size packets

| 3 | 4 | 5 | 6 | 12345678 | 7 | 8 | 1234 | 5678 | 1234 | 3 | 4 | 5 | 6 | 7 | 8 | 5678 |

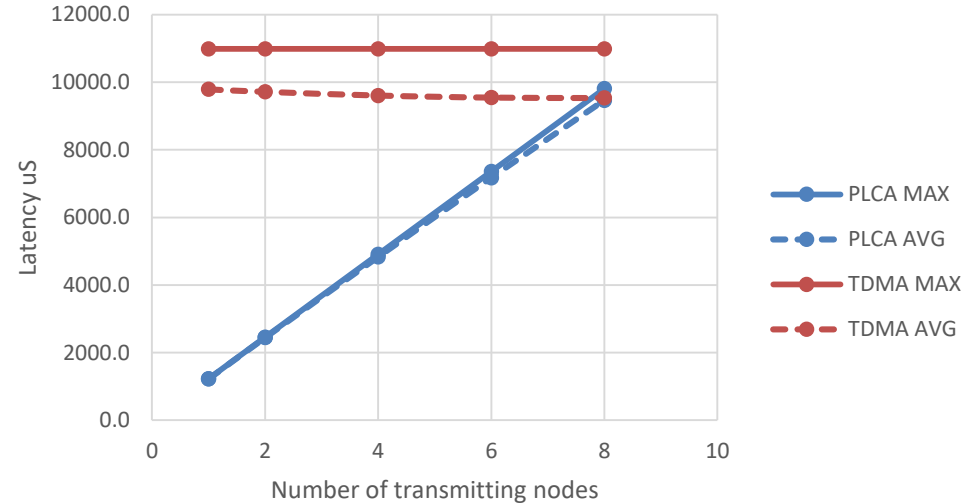0   10   15   20   30 ms

TDMA CYCLE

One or more available time slot must be statically assigned to each node
Unused time slots are wasted, they cannot be used by other nodes as in PLCA
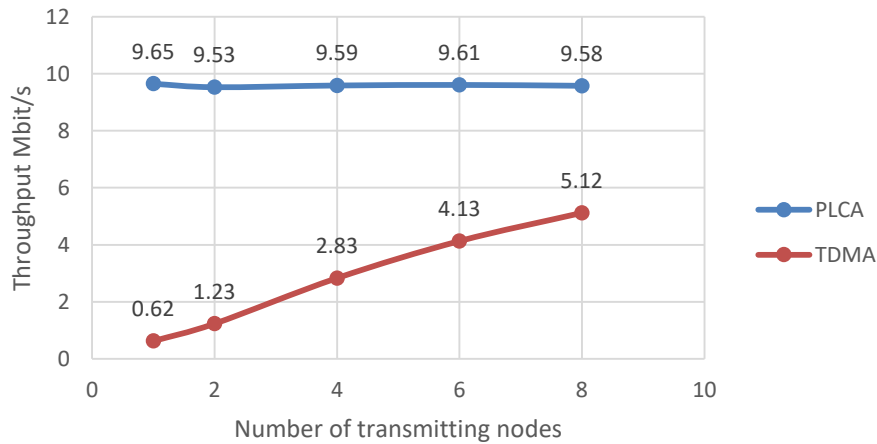
PLCA vs TDMA performance
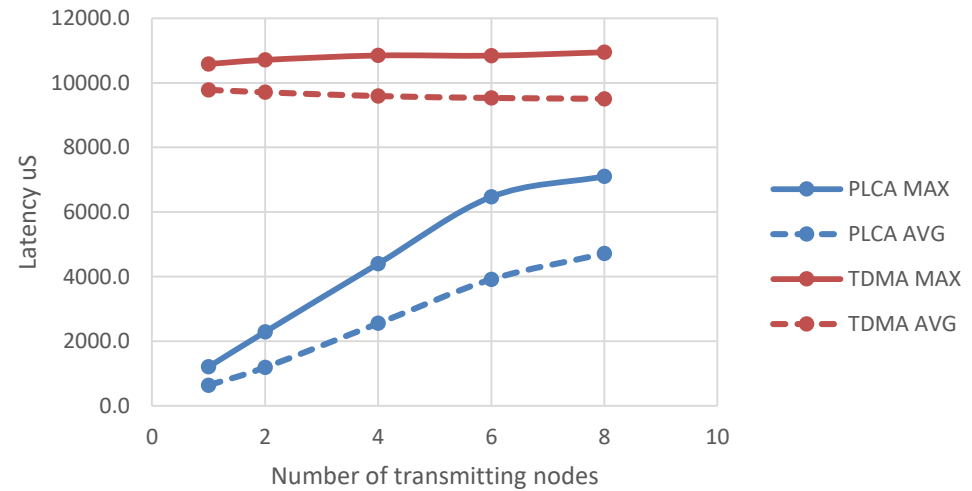

THROGHPUT - burst with PKT_SIZE = 1500
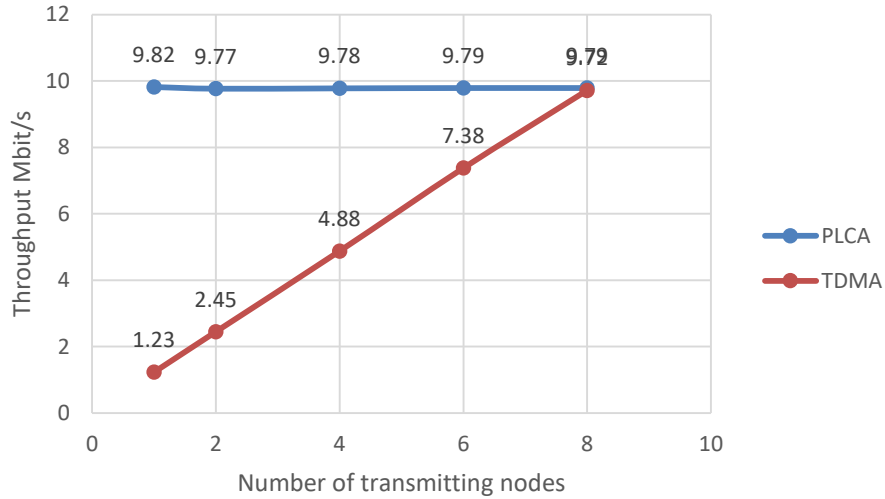
LATENCY - burst with PKT SIZE = 1500

THROUGHPUT - burst with PKT_SIZE = random(60, 1500)

LATENCY - burst with PKT SIZE = random(60, 1500)

PLCA

- Works with existing MAC
- Transparent to MAC client and upper level protocols
- Efficient use of available bandwidth (very little overhead)
- Adds packet jitter (variable latency)
  - worst case is determined, always guaranteed and less than TDMA
- Optional, can be reverted to standard CSMA/CD
- Impact on PHY complexity is very low

TSN + TDMA

- Requires HW support in the MAC
- Requires a full engineered network
- Pushes all the complexity at host (SW) / MAC level
  - Might not be suitable for low-end processors
- Very deterministic
- Significant throughput penalty due to unused / partially filled time slots

Thank You !