Short/Mid-Reach
10SPE PHY with Multipoint

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A 15/40m PHY Candidate

- A short-reach (15/40m, 4 conn) for point-point interface
  - Goal - a 50% reduction in power, area, pins relative to 100BT1

AWG	Length @ IL limit(m)	Length @ ohms loop R 6.5	12	25	4M IL @15m 4 conn	IL @ 100m 4 conn	IL @ 200m 4 conn	IL @ 1km 10 conn
14	1589	353	652	1359	0.4	1.5	3.4	16.5
16	1261	221	408	850	0.5	1.8	4.2	20.7
18	1000	139	258	536	0.5	2.3	5.3	25.9
20	793	88	162	337	0.6	2.8	6.6	32.6
22	629	55	102	212	0.8	3.5	8.3	41.0
24	499	35	64	133	0.9	4.4	10.4	51.6
26	395	22	40	84	1.1	5.5	13.1	65.0
28	314	14	25	53	1.4	6.9	16.5	81.9

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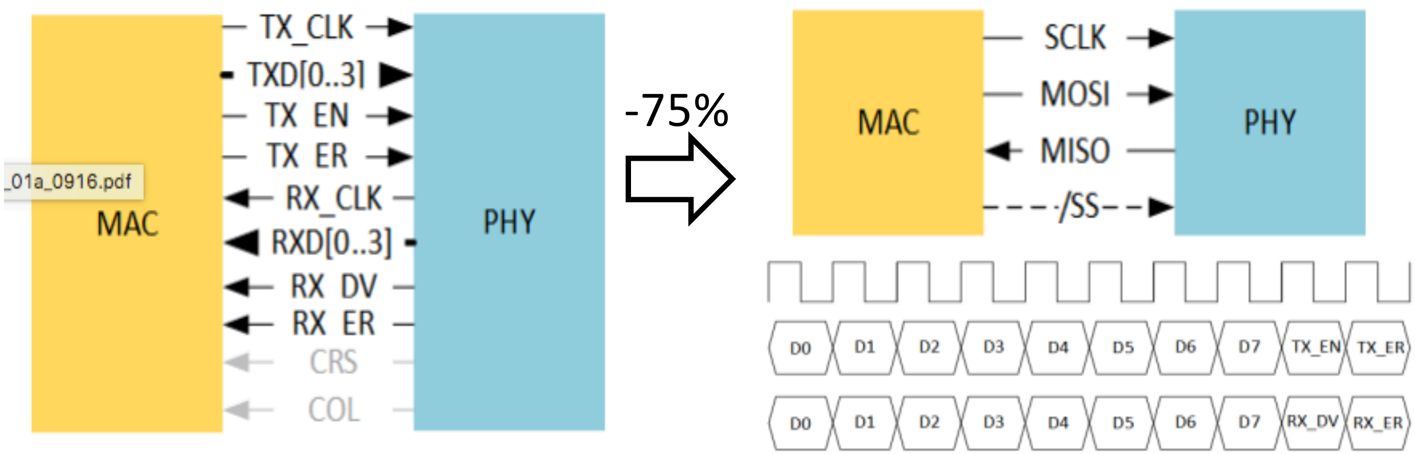
10Mb/s SPE PHY Strawman

- Simplify the signaling
  - DME (Differential Manchester Encoding)
  - TX - Class AB transmitter sending binary levels @ 20MHz
  - RX - Analog equalizer, comparators for receive,
  - RX - Largely eliminate DSP, except for floating EQ

10Mb/s SPE PHY Package Design

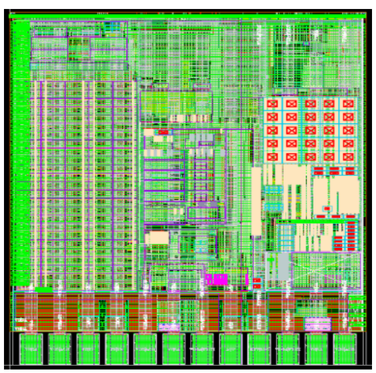
- Can the package follow the silicon area reduction?
  - A 100BT1 discrete PHY may have 36 pins
- Power supply pins will scale significantly
- MII is 16 pins, a significant percentage of the total
  - Can reduce this to 4 pins without changing the MAC interface: “xMII”
  - cordaro_thaler_10SPE_01a_0916.pdf



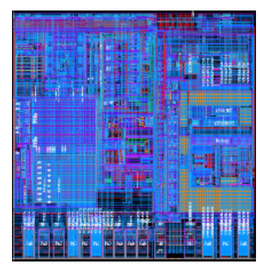
- A 14-pin package is reasonable for this protocol

10Mb/s SPE PHY Design

- Area < ~25-30% of 100BT1 area
  - This is approximately the area of 100Base-TX
- Power Dissipation < ~33% of 100BT1
  - Power reduction supports reduction of package pins
  - Important given the number of 10Mb/s nodes in the network
- Low-power drives low pin-count packages

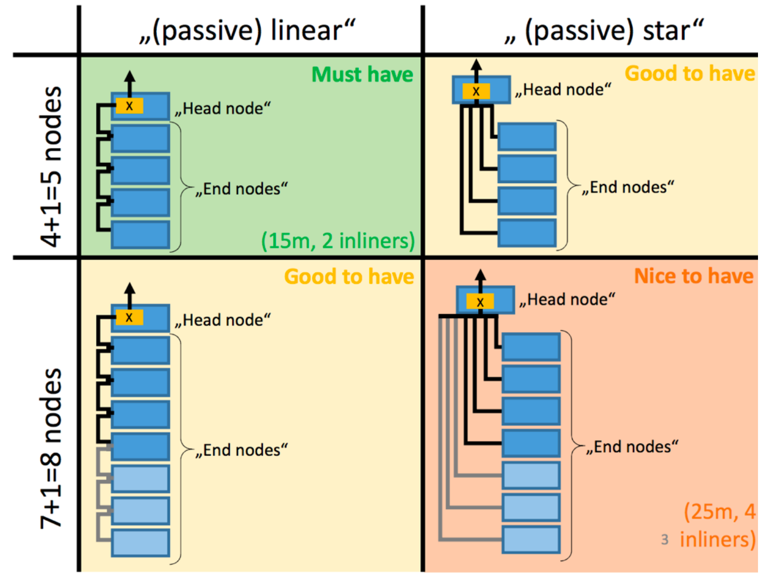


Conclusion: Yes, it’s possible to reduce silicon area/power by >50%



What About Multipoint?

- Increases signal-integrity challenge relative to the baseline, but it can be managed
- Need to fix insertion loss, delay, number of nodes
  - Some models exist for automotive, need to expand the list for other use cases (i.e. cabinets, building infrastructure)
- Bigger challenge is addressing the implications of “sharing” versus point-point



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What About Multipoint

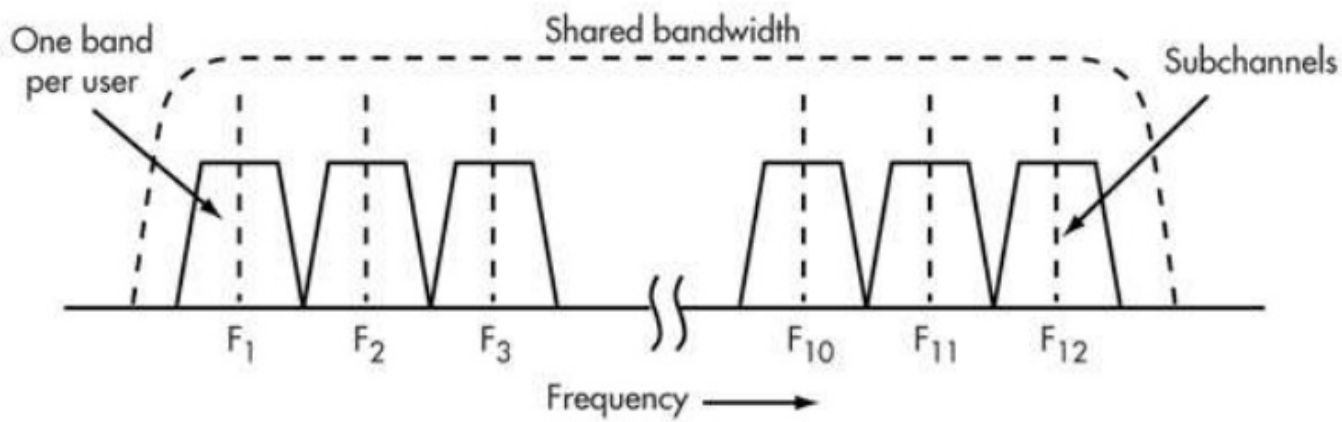
- For this simple, traditional PHY can we add circuitry to implement CMAS/CD?
  - Shows promise, leverages existing PHY topologies with some additional modifications
  - Costs network performance and places limitations on physical constraints
- Alternative - TDMA-based
  - Can also leverage traditional PHY architectures, but the overall solution is compromised:
    - Inefficient allocation of resources
    - Allocate time-slots for nodes AND allocate time-slots in between
    - Fixed number of nodes, time-sync challenges given variable spacing

How About FDMA?

- The frequency domain is a clean way to "share." Everyone can talk at the same time, nodes go through a set-up and are allocated a fixed-channel
- Better network performance, opens the door to lower power (analog implementation), but it's different/new

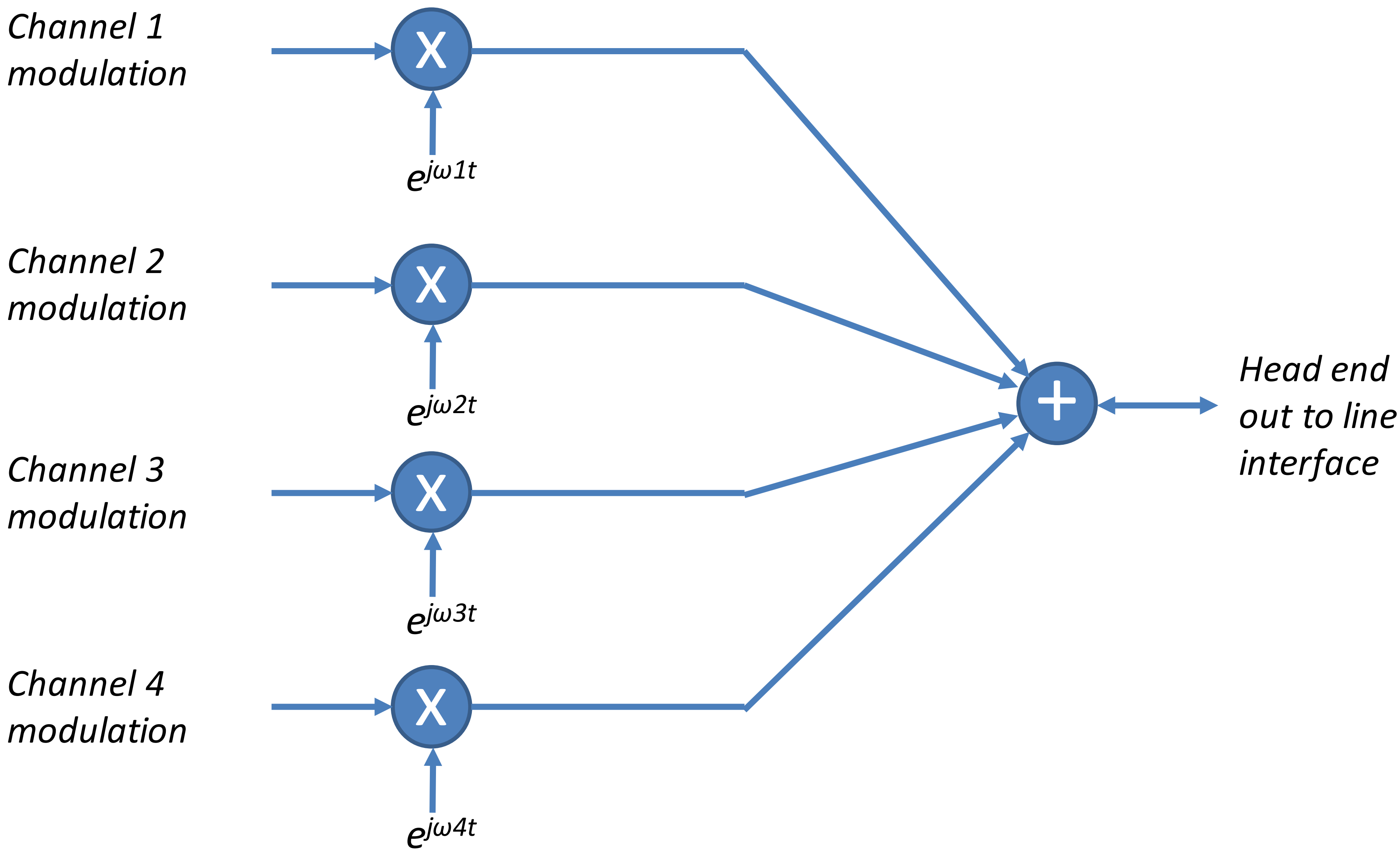
FDMA-Conceptual

- Leverages simple low-power/low-cost multichannel wireless topologies

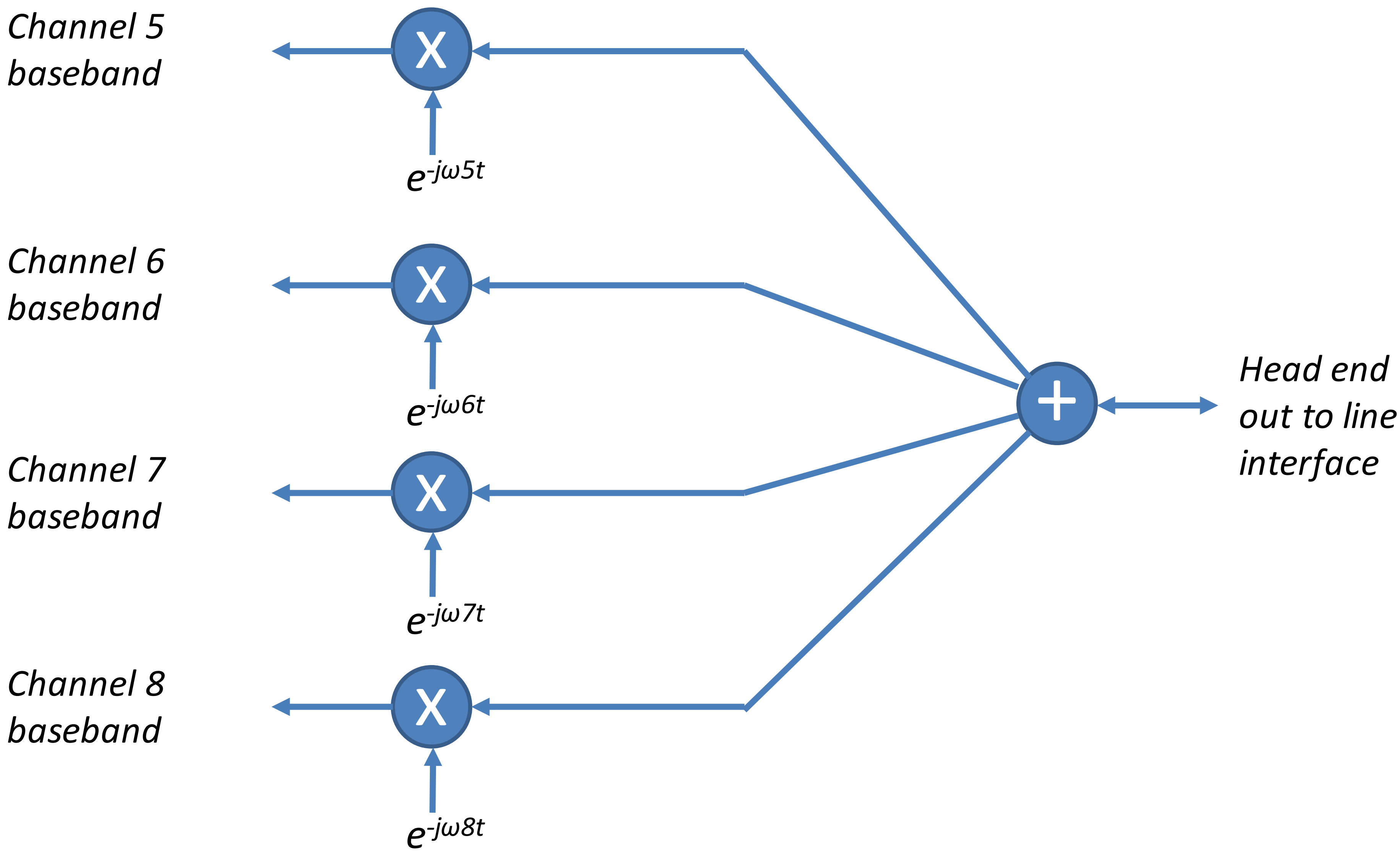


– Frequency Allocation
  - First consider 4 channels
  - Use all the available bandwidth (i.e. 100MHz?) and allocate individual 10MHz channels – OR use 36MHz ("sweetspot bandwidth") and rely on encoding to get 10Mb/s from 4MHz channels

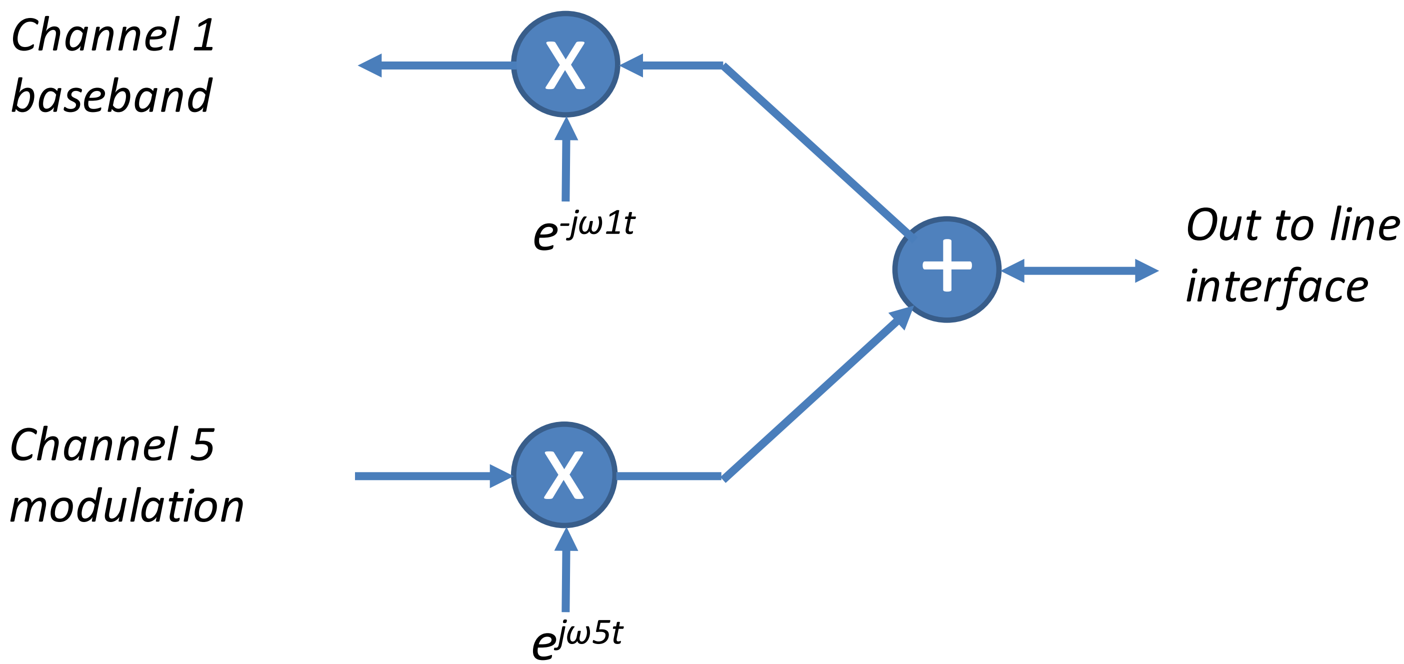
Parallel head-end transmitter conceptual



Parallel head end receiver conceptual



Single-node transmitter/receiver conceptual



More Needed

- Autonegotiation and channel assignment
- Channel conditions for non-automotive mid-reach multi-drop cases
  - Fix on max/min conditions
  - Connector characteristics
- Power estimation and complexity analysis for both topologies

Thank-You!