Optional Power Distribution
IEEE 802.3 10 Mb/s Single Twisted Pair Ethernet Task Force

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Purpose

- **Scope**
  - **Optional Power Distribution consistent with Link Segment DCR and use case power requirements.**

Contributors

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- Steffen Graber, Timo Graber – Pepperl+Fuchs
- David Brandt – Rockwell Automation

IEEE 802.3cg: Adopted Objectives

Objectives (2)

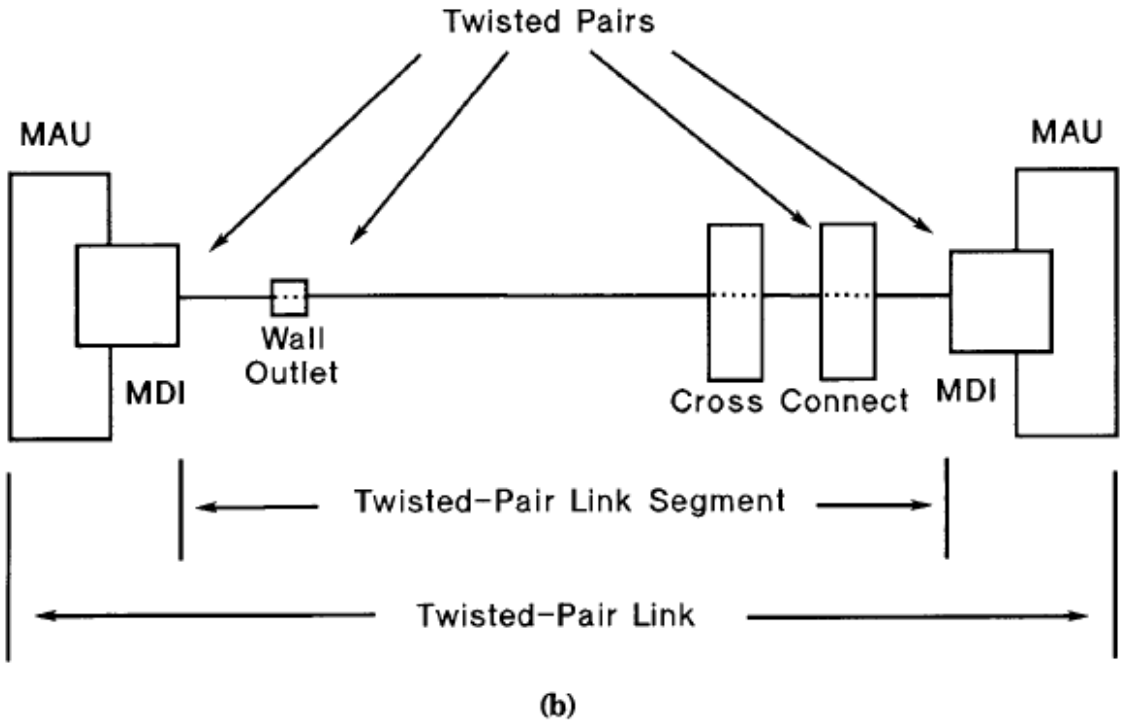
11. Define the performance characteristics of a link segment and a PHY to support operation over this link segment with single twisted pair supporting up to four inline connectors using balanced cabling for up to at least 15 m reach
12. Define the performance characteristics of a link segment and a PHY to support point-to-point operation over this link segment with single twisted pair supporting up to 10 inline connectors using balanced cabling for up to at least 1 km reach
13. Support fast-startup operation using predetermined configurations which enables the time from power_on**=FALSE to a state capable of transmitting and receiving valid data to be less than 100ms
14. Maintain a bit error ratio (BER) at the MAC/PLS service interface of less than or equal to 10^{-10} on link segments up to at least 15m, and 10^{-9} on link segments up to at least 1km
15. Specify one or more optional power distribution techniques for use over the 10 Mb/s single balanced twisted-pair link segments, in conjunction with 10 Mb/s single balanced twisted-pair PHYs, in the automotive and industrial environments

Source: http://www.ieee802.org/3/10SPE/objectives_10SPE_111016.pdf

Link Segment

1.4.242 link segment: The point-to-point full-duplex medium connection between two and only two Medium Dependent Interfaces (MDIs).

- **Example 10BASE-T**



(b)

Figure 14–2—Twisted-pair link

P802.3bu PoDL System

- **Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet**

Figure 104–3 illustrates the block diagram for a PoDL system.

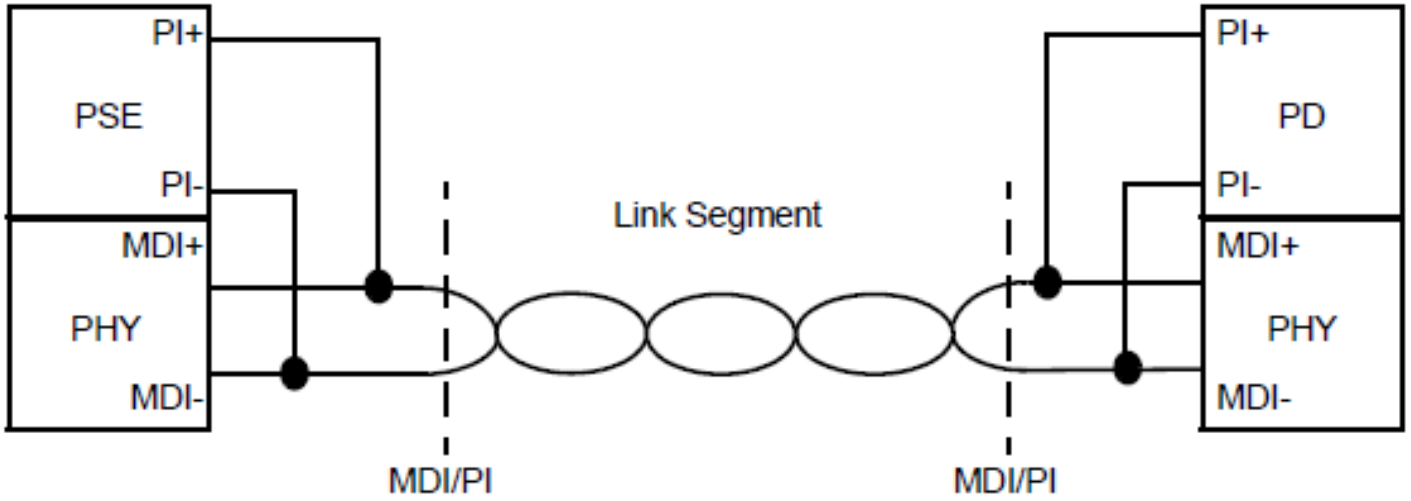


Figure 104–3—PoDL system block diagram

Note: PI interface elements that prevent loading of the data signal by the PSE and PD are not shown. PHY elements that block DC are not shown.

P802.3bu PoDL System

- **Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet**

104.3 Class power requirements

Table 104–1—Class power requirements matrix for PSE, PI, and PD

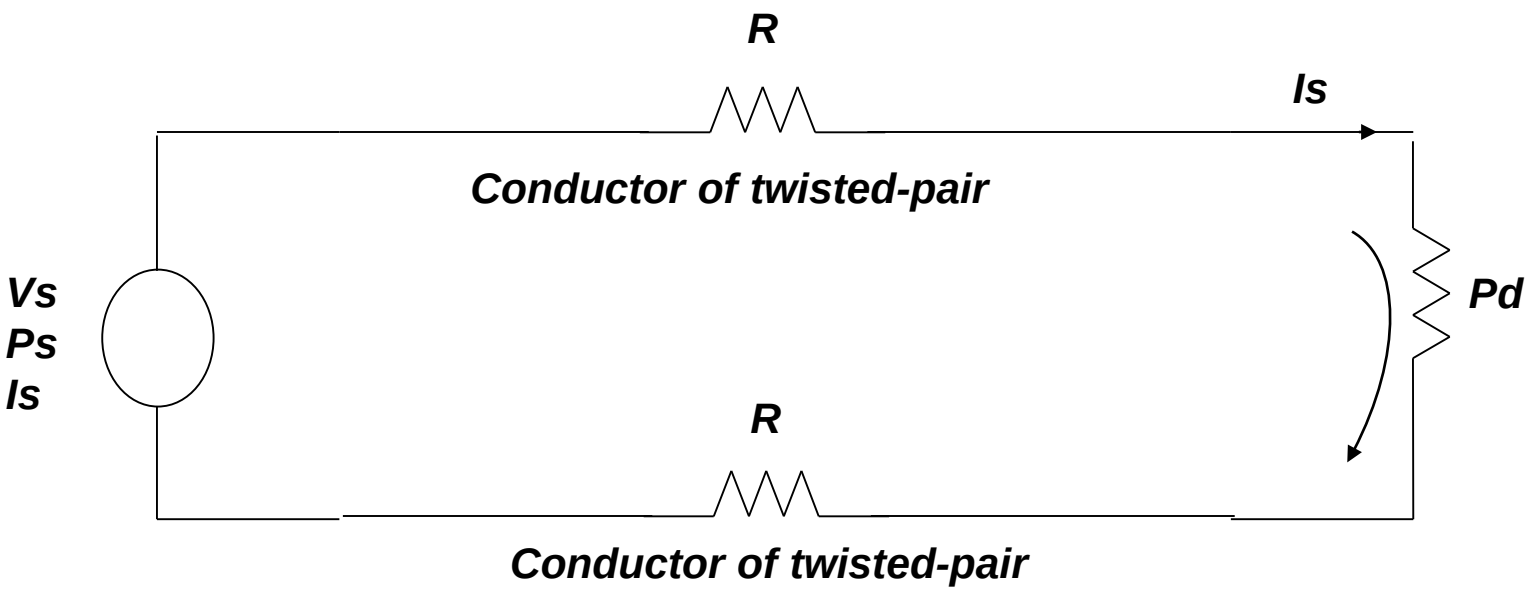
	12 V unregulated PSE		12 V regulated PSE		24 V unregulated PSE		24 V regulated PSE		48 V regulated PSE	
Class	0	1	2	3	4	5	6	7	8	9
$V_{PSE(max)}$ (V)[a]	18	18	18	18	36	36	36	36	60	60
$V_{PSE\_OC(min)}$ (V)[b]	6	6	14.4	14.4	12	12	26	26	48	48
$V_{PSE(min)}$ (V)	5.6	5.77	14.4	14.4	11.7	11.7	26	26	48	48
$I_{PI(max)}$ (mA)[c]	101	227	249	471	97	339	215	461	735	1 360
$P_{Class(min)}$ (W)[d]	0.566	1.31	3.59	6.79	1.14	3.97	5.59	12	35.3	65.3
$V_{PD(min)}$ (V)	4.94	4.41	12	10.6	10.3	8.86	23.3	21.7	40.8	36.7
$P_{PD(max)}$ (W)[e]	0.5	1	3	5	1	3	5	10	30	50

[a] $V_{PSE(max)}$ is the maximum allowed voltage at the PSE PI over the full range of operating conditions.
[b] $V_{PSE\_OC(min)}$ is the minimum allowed open circuit voltage measured at the PSE PI.
[c] $I_{PI(max)}$ is the maximum current flowing at the PSE and PD PIs except during inrush or an overload condition. $I_{PI(max)}$ may be exceeded during inrush or an overload (see 104.4.6.2). Users are cautioned to be aware of the ampacity of cabling, as installed, and local codes and regulations (see 104.8.1).
[d] $P_{Class(min)}$ is the minimum average available output power at the PSE PI.
[e] $P_{PD(max)}$ is the maximum average available power at the PD PI.

PSEs and PDs are further categorized by their Class. These Classes and the relevant electrical specifications are shown in Table 104–1.

DC loop resistance
Less than 6 Ω for 12 V unregulated Classes and less than 6.5 Ω for 12 V regulated, 24 V regulated and unregulated, and 48V regulated Classes.

Schematic representation



Power at the output of the power supply: Ps=Vs*Is
Max Power dissipated in the cable: Pc=(Is^2)*2R
Power at the powered device: = Pd = Ps-Pc
Loop resistance = 2R

802.3cg Link Segment - copper cable DCR

AWG	Diameter(in)	Diameter(mm)	Diameter(m)	area (m^2)	Resistance (m)
14	0.064085	1.627754	0.001627754	2.08098E-06	0.0092
15	0.057069	1.449551	0.001449551	1.65028E-06	0.0116
16	0.050821	1.290858	0.001290858	1.30872E-06	0.0147
17	0.045257	1.149538	0.001149538	1.03785E-06	0.0185
18	0.040303	1.023689	0.001023689	8.2305E-07	0.0233
19	0.035890	0.911618	0.000911618	6.52703E-07	0.0294
20	0.031961	0.811816	0.000811816	5.17614E-07	0.0371
21	0.028462	0.722941	0.000722941	4.10483E-07	0.0468
22	0.025346	0.643795	0.000643795	3.25526E-07	0.0590
23	0.022571	0.573314	0.000573314	2.58152E-07	0.0744
24	0.020100	0.510549	0.000510549	2.04722E-07	0.0938
25	0.017900	0.454655	0.000454655	1.62351E-07	0.1183
26	0.015940	0.404881	0.000404881	1.28749E-07	0.1492
27	0.014195	0.360555	0.000360555	1.02102E-07	0.1881
28	0.012641	0.321083	0.000321083	8.09698E-08	0.2372
29	0.011257	0.285931	0.000285931	6.42115E-08	0.30
30	0.010025	0.254628	0.000254628	5.09217E-08	0.38
31	0.008927	0.226752	0.000226752	4.03824E-08	0.48
32	0.007950	0.201928	0.000201928	3.20245E-08	0.60

Reference conductor resistivity = 1.92*10^-8 Ω m

802.3cg Link Segment - copper cable DCR

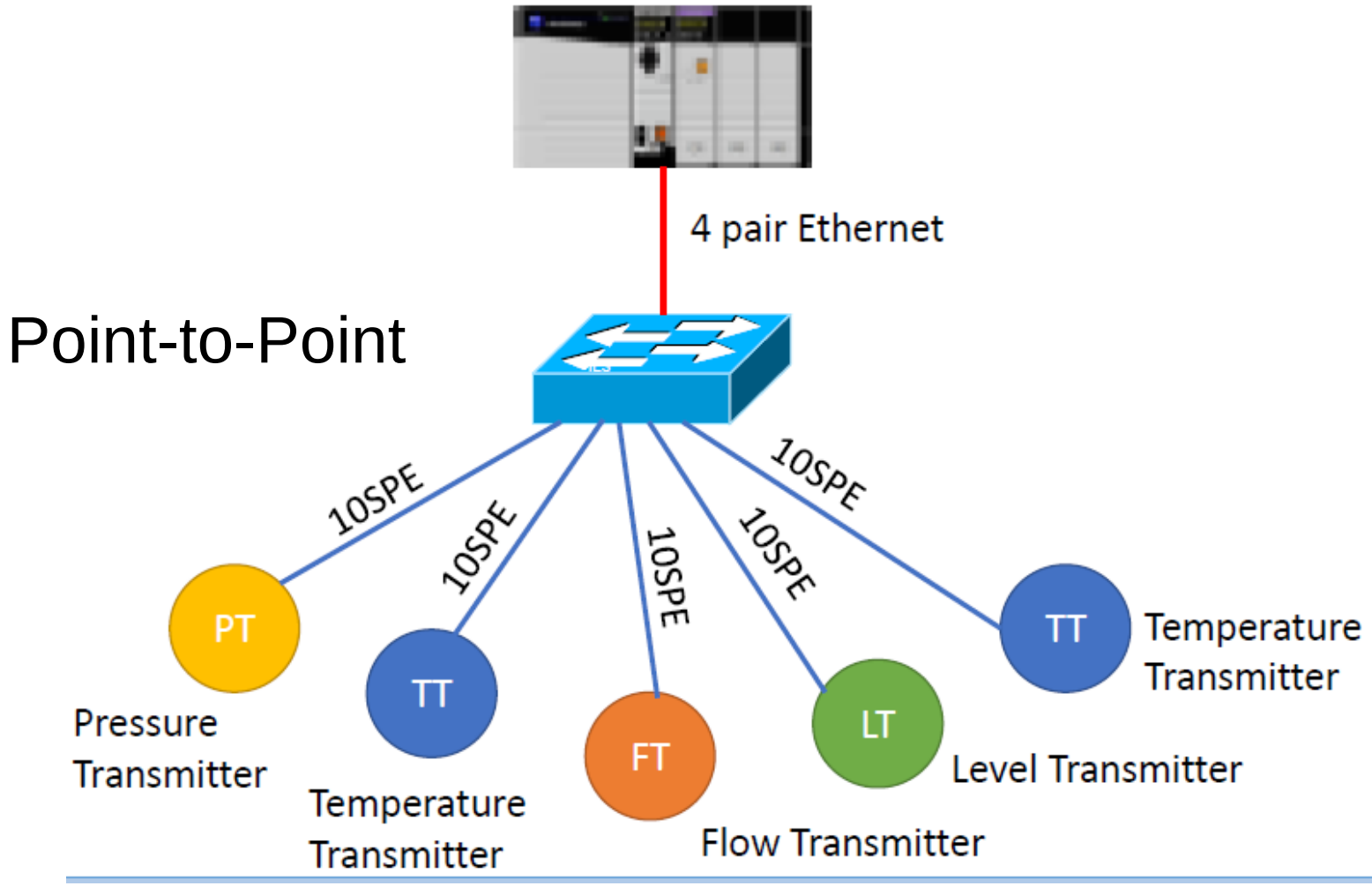
AWG	Diameter(in)	Diameter(mm)	dB/m at 4 MHz solid	dB/m at 4 MHz stranded	Cable @ 4 MHz stranded @ IL limit (dB)	Cable (m) @ IL limit	10*connectors (dB)	Channel Il (dB)
14	0.064085	1.627754	0.013389	0.016067	25.54	1589	0.4	25.94
15	0.057069	1.449551	0.015035	0.018042	25.54	1415	0.4	25.94
16	0.050821	1.290858	0.016883	0.020260	25.54	1261	0.4	25.94
17	0.045257	1.149538	0.018959	0.022751	25.54	1123	0.4	25.94
18	0.040303	1.023689	0.021290	0.025548	25.55	1000	0.4	25.95
19	0.035890	0.911618	0.023907	0.028688	25.55	891	0.4	25.95
20	0.031961	0.811816	0.026846	0.032215	25.55	793	0.4	25.95
21	0.028462	0.722941	0.030146	0.036175	25.55	706	0.4	25.95
22	0.025346	0.643795	0.033852	0.040623	25.54	629	0.4	25.94
23	0.022571	0.573314	0.038014	0.045617	25.54	560	0.4	25.94
24	0.020100	0.510549	0.042687	0.051225	25.54	499	0.4	25.94
25	0.017900	0.454655	0.047935	0.057522	25.54	444	0.4	25.94
26	0.015940	0.404881	0.053828	0.064594	25.54	395	0.4	25.94
27	0.014195	0.360555	0.060446	0.072535	25.54	352	0.4	25.94
28	0.012641	0.321083	0.067876	0.081452	25.54	314	0.4	25.94
29	0.011257	0.285931	0.076221	0.091465	25.54	279	0.4	25.94
30	0.010025	0.254628	0.085591	0.102710	25.54	249	0.4	25.94
31	0.008927	0.226752	0.096114	0.115336	25.54	221	0.4	25.94
32	0.007950	0.201928	0.107929	0.129515	25.54	197	0.4	25.94

Link segment IL - 25.95 dB @ 4 MHz

802.3cg Link Segment - DCR

AWG	Diameter(in)	Diameter(mm)	Diameter(m)	area (m^2)	Resistance per meter (ohm)	Length @ IL limit (m)	Conductor resistance @ IL limit (ohm)	Loop resistance @ IL limit (ohm)	10 connector DCR	Link segment resistance @ IL limit (ohm)
14	0.064085	1.627754	0.001627754	2.08098E-06	0.0092	1589	14.67	29.33	4.00	33.33
15	0.057069	1.449551	0.001449551	1.65028E-06	0.0116	1415	16.47	32.94	4.00	36.94
16	0.050821	1.290858	0.001290858	1.30872E-06	0.0147	1261	18.50	37.00	4.00	41.00
17	0.045257	1.149538	0.001149538	1.03785E-06	0.0185	1123	20.78	41.55	4.00	45.55
18	0.040303	1.023689	0.001023689	8.2305E-07	0.0233	1000	23.33	46.66	4.00	50.66
19	0.035890	0.911618	0.000911618	6.52703E-07	0.0294	891	26.20	52.40	4.00	56.40
20	0.031961	0.811816	0.000811816	5.17614E-07	0.0371	793	29.42	58.84	4.00	62.84
21	0.028462	0.722941	0.000722941	4.10483E-07	0.0468	706	33.04	66.07	4.00	70.07
22	0.025346	0.643795	0.000643795	3.25526E-07	0.0590	629	37.10	74.19	4.00	78.19
23	0.022571	0.573314	0.000573314	2.58152E-07	0.0744	560	41.66	83.31	4.00	87.31
24	0.020100	0.510549	0.000510549	2.04722E-07	0.0938	499	46.78	93.55	4.00	97.55
25	0.017900	0.454655	0.000454655	1.62351E-07	0.1183	444	52.53	105.05	4.00	109.05
26	0.015940	0.404881	0.000404881	1.28749E-07	0.1492	395	58.98	117.96	4.00	121.96
27	0.014195	0.360555	0.000360555	1.02102E-07	0.1881	352	66.23	132.46	4.00	136.46
28	0.012641	0.321083	0.000321083	8.09698E-08	0.2372	314	74.37	148.74	4.00	152.74
29	0.011257	0.285931	0.000285931	6.42115E-08	0.30	279	83.51	167.02	4.00	171.02
30	0.010025	0.254628	0.000254628	5.09217E-08	0.38	249	93.78	187.55	4.00	191.55
31	0.008927	0.226752	0.000226752	4.03824E-08	0.48	221	105.30	210.60	4.00	214.60
32	0.007950	0.201928	0.000201928	3.20245E-08	0.60	197	118.24	236.49	4.00	240.49

802.3cg DC Powering Use Cases



Source: http://www.ieee802.org/3/cg/public/Jan2017/10SPE_Powering_Use_Cases_BV.pdf

802.3cg DC Powering Use Cases (P-to-P)

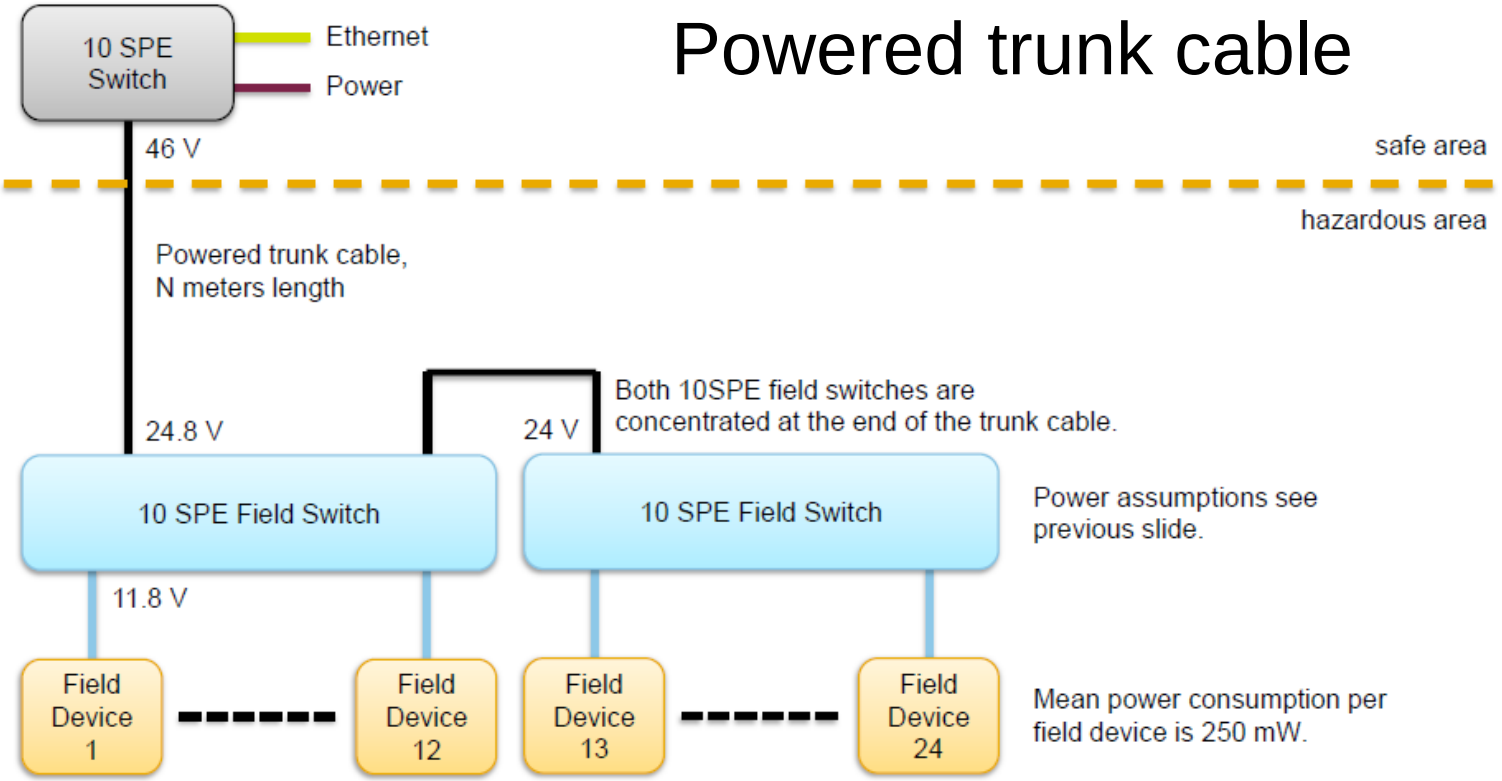
- The device class for the powered device (PD) based on process industry use cases

Device Class (PD)	Max. Voltage	Min. Voltage	Power
Low Power Device	17.5 V	9.0 V	0.5 W
Medium Power Device	17.5 V	9.0 V	2 W
High Power Device	17.5 V	9.0 V	5 W
Ultra High Power Device	48.0 V	24.0 V	up to 120 W (topology dependent)

Source: Steffen Graber Pepperl+Fuchs

802.3cg DC Powering Use Cases

10SPE Calculation Example



Powered trunk cable

http://www.ieee802.org/3/cg/public/Jan2017/Graber_10SPE_09a_0117.pdf

802.3cg DC Powering Use Cases

- Powered trunk cable

- Power supply equipment (PSE) based on process industry long trunk use cases.
- Power at the PD (field switch or trunk end-point PD) depends on the trunk length and AWG

Source Class (PSE) for Trunk	Output voltage	Output Power
High Power Source	48.0 V	60 W
Ultra High Power Source	48.0 V	120 W

Source: Steffen Graber Pepperl+Fuchs

Optional Power Distribution

- **Link Segment DCR and length @ IL limit different for each AWG.**
- **Variety of voltages, currents and power for “use cases” presented.**
- **Optional power distribution;**
  - **Specify power/voltage/current/DCR for a link segment topology* (plug-and-play).**
  - **Specify “engineered” power delivery for other topologies*.**

***Topology with DCR less than or equal to DCR and length @ IL limit.**

Recommendations

- Adopt normative annex “Optional Power Distribution”
- Adopt PD power requirements for powered devices in Table below. Specify Link Segment DCR for each PD (TBD)

Device Class (PD)	Max. Voltage	Min. Voltage	Power
Low Power Device	17.5 V	9.0 V	0.5 W
Medium Power Device	17.5 V	9.0 V	2 W
High Power Device	17.5 V	9.0 V	5 W
Ultra High Power Device	48.0 V	24.0 V	up to 120 W (topology dependent)

Recommendations

- **Adopt PD power requirements for powered devices in Table below.**
- **Specify methodology to "engineer" link segment DCR and topology (cable diameter, length, number of devices in the daisy chain, etc.)**

Source Class (PSE) for Trunk	Output voltage	Output Power
High Power Source	48.0 V	60 W
Ultra High Power Source	48.0 V	120 W

Recommendations

- Adopt Link Segment DCR characteristics Table below with introduction detailing table entry derivation for inclusion in annex.

AWG	Resistance per meter (ohm)	Length @ IL limit (m)	Conductor resistance @ IL limit (ohm)	Loop resistance @ IL limit (ohm)	10 connector DCR	Link segment resistance @ IL limit (ohm)
14	0.0092	1589	14.67	29.33	4.00	33.33
15	0.0116	1415	16.47	32.94	4.00	36.94
16	0.0147	1261	18.50	37.00	4.00	41.00
17	0.0185	1123	20.78	41.55	4.00	45.55
18	0.0233	1000	23.33	46.66	4.00	50.66
19	0.0294	891	26.20	52.40	4.00	56.40
20	0.0371	793	29.42	58.84	4.00	62.84
21	0.0468	706	33.04	66.07	4.00	70.07
22	0.0590	629	37.10	74.19	4.00	78.19
23	0.0744	560	41.66	83.31	4.00	87.31
24	0.0938	499	46.78	93.55	4.00	97.55