10 Mb/s Single Twisted Pair Ethernet
Evaluation Board Update
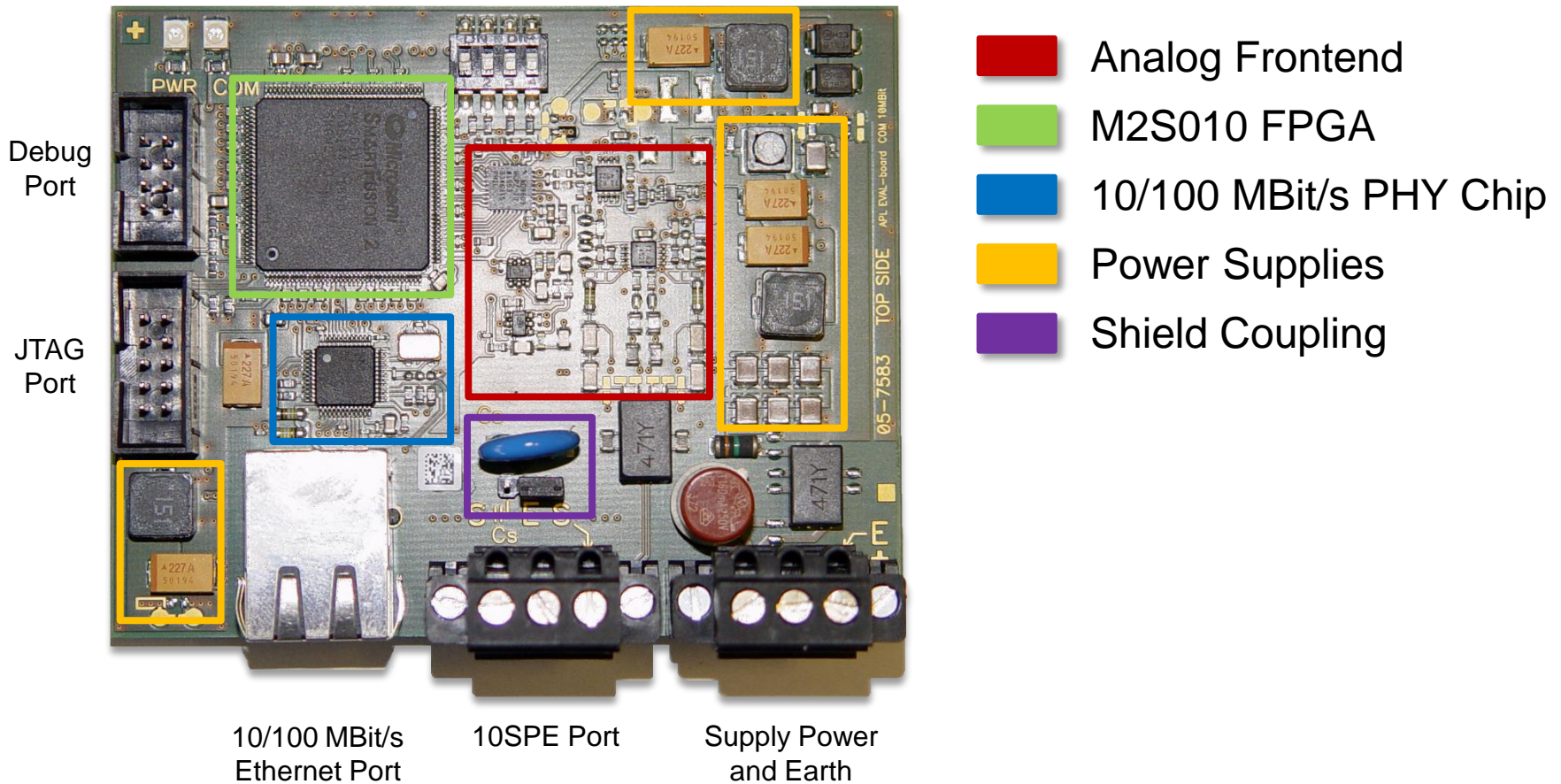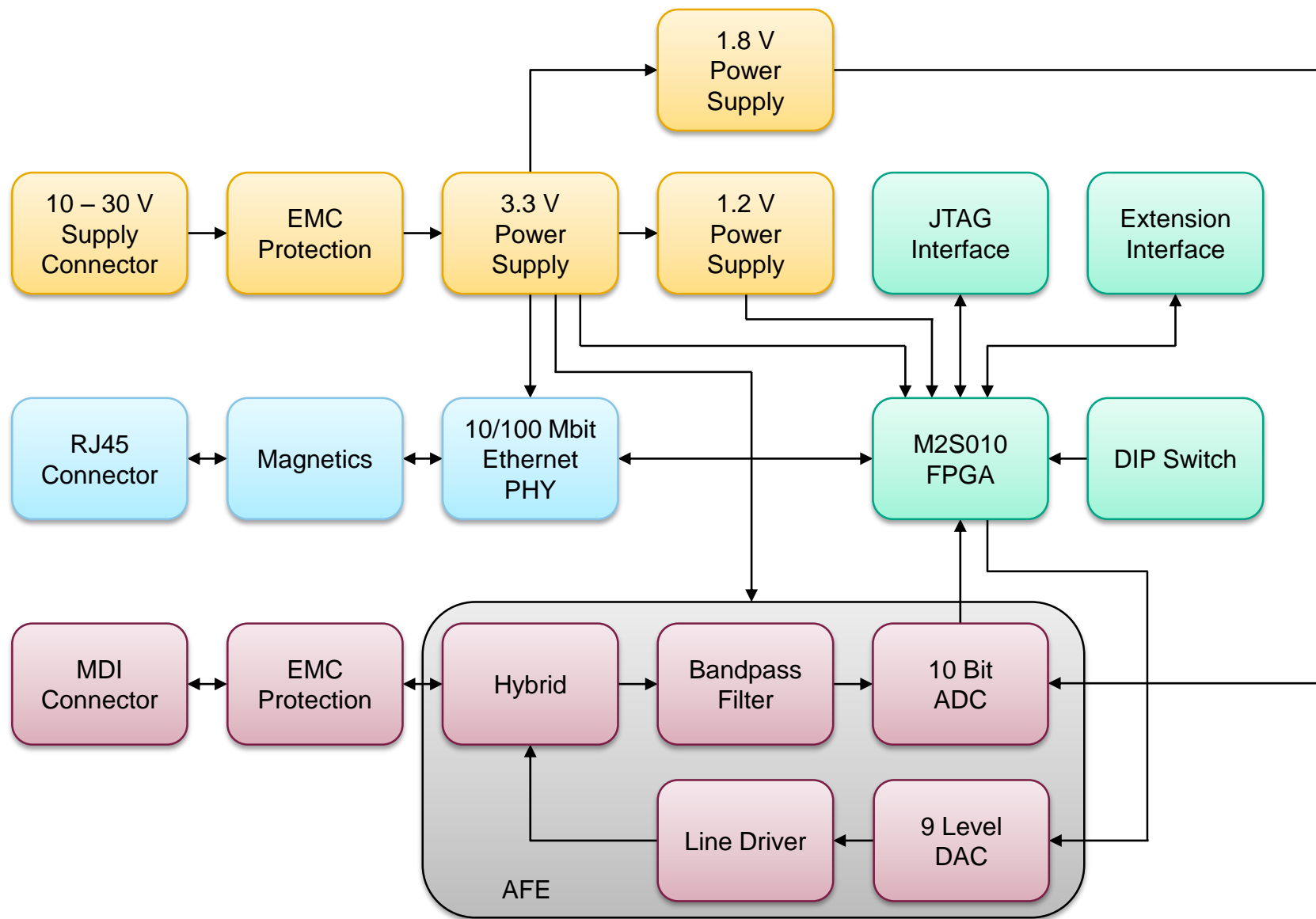
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Evaluation Board Overview

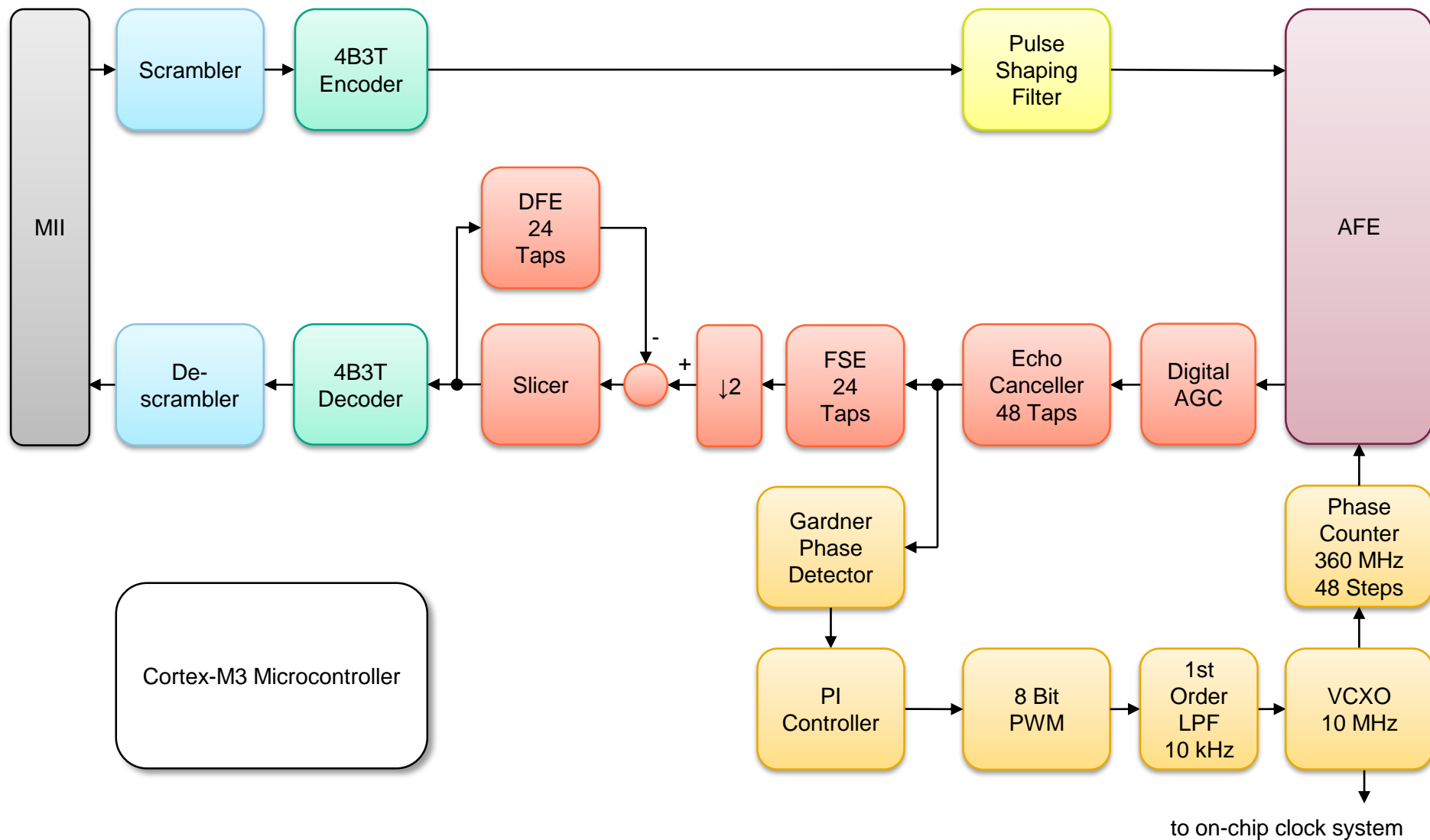- Below the PCB of the Evaluation Board can be seen.
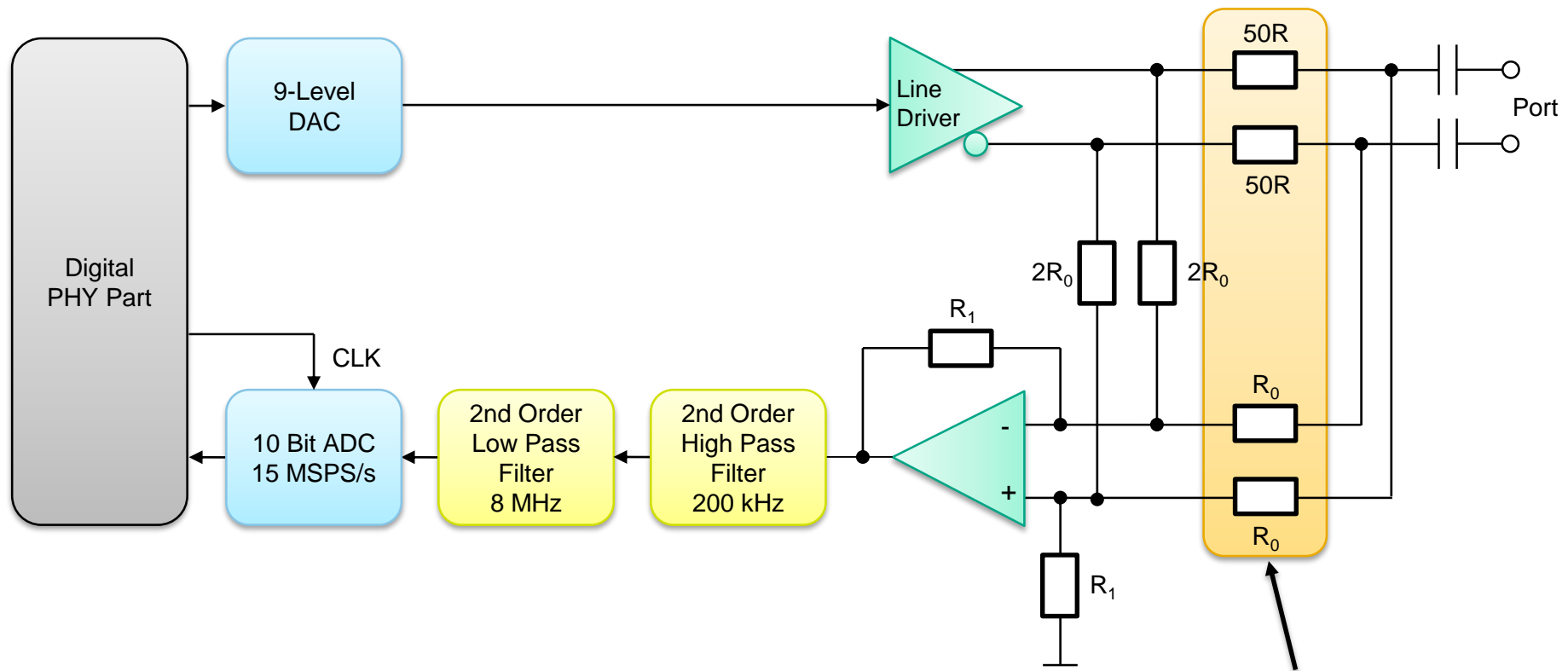

Debug Port

JTAG Port

10/100 MBit/s Ethernet Port

10SPE Port

Supply Power and Earth

Analog Frontend

M2S010 FPGA

10/100 MBit/s PHY Chip

Power Supplies

Shield Coupling

Evaluation Board Block Diagram

FPGA Implementation

Analog Frontend Implementation

- Due to simplicity of the discrete implementation a 10 bit ADC without analog AGC is being used.
- Filtering within the line driver for signal smoothing is not shown.
- Amplifier compensation within the receive circuit is not shown.

For intrinsically safe applications these resistors can also be used for current and power limiting purposes if they fulfill the demands of IEC/EN60079-11 (the resistor values will be different, depending on the application).

Implementation Update

- On the master side the following scrambler polynomial is being used: $f(x) = 1 + x^{-18} + x^{-23}$
- On the slave side the following scrambler polynomial is being used: $g(x) = 1 + x^{-5} + x^{-23}$
- The implemented descramblers are self synchronizing on the scrambled data stream.
- The 4B3T encoder takes 4 bit of data and produces a ternary triplet, depending on the running disparity.
- The 4B3T decoder takes a ternary triplet and returns the coded 4 bits.
- There is no need to synchronize to a running disparity (the ternary values have a distinct assignment to the 4 bit data value).
- The transmit filter is forming a trapezoidal transmit signal using 9 levels.
- The DAC output rate is 120 MHz.
- The ADC is now running at 15 MHz (2 times oversampling of the 7.5 MSPS/s symbol rate).
- The ADC resolution is 10 bit (with the possibility to get approx. 0.7 additional bits by an integrated PGA).
- Therefore the resulting ENOB of the ADC is approx. 10 bit.
- A digital AGC (with integrated digital offset compensation) is being implemented within the FPGA (this is the reason for the 10 bit ADC).
- Because the echo canceller is now running at two times the symbol rate the number of taps has been increased to 48 taps.
- The training speed of the echo canceller has been increased and now all echo canceller taps can be trained every fourth symbol during initial startup.
- The 24 tap FSE is running at two times the symbol rate and implements a fast training every four symbols.

Implementation Update

- The 24 tap DFE is running at baud rate speed also with a fast training every four symbols.
- After the initial fast training, the training speed is being reduced during normal operation.
- The FSE is initially being trained using blind adoption (CMA algorithm), during continuous operation LMS training is being used.
- The DFE is being trained with the LMS algorithm as soon as a good enough SNR at the slicer has been reached after the initial training of the FSE.
- A loop timed clock system is being used for the link.
- The master clock is running at a fixed rate.
- The slave clock is being adopted to the master clock, using the Gardner algorithm as phase detector.
- In the current design a VCXO is being used for frequency/phase adoption on the slave device side (in an integrated solution this will be handled by a PLL, the FPGA does not support the needed PLL).
- This VCXO is being guaranteed to allow an adjustment of ±100 ppm of its clock frequency (typical pull range is ±120 ppm) having an initial tolerance of ±50 ppm over the full operating temperature range.
- This allows for a maximum master clock tolerance of ±50 ppm.
- At the master side, the initial searching of the receive phase and the tracking of the receive phase over temperature is also done using the Gardner algorithm.
- A counter running at 360 MHz allows for an adjustment of the phase in 48 steps (7.5° steps)
- A Cortex-M3 microcontroller integrated within the FPGA is currently being used to handle the needed state machines for link training, master phase tracking, impulse noise detection, link loss etc.

Implementation Update

- A continuously transmitted data stream is necessary to keep the clocks between the master and the slave device synchronized, therefore with no active communication an IDLE data stream is being transmitted.
- The following line shows how the data transmission is currently being implemented:

IDLE	COMMA	EOC	SOC	IDLE	COMMA	EOC	SOF	DATA	COMMA	EOF	SOC	IDLE

- A control sequence is always consisting of 3 elements:
    - Comma Value (000 000)
    - End Delimiter
        - EOC – End of Control
        - EOF_OK – End of Frame (OK)
        - EOF_ERR – End of Frame with Error, e.g. cut-through RX error
    - Start Delimiter
        - SOC – Start of Control
        - SOF – Start of Frame
- The comma value is consisting of 6 consecutive zeros. Within the normal data stream only up to 4 consecutive zeros are allowed, so that the comma sequence can clearly be identified.
- An end delimiter is always having a disparity of zero.
- A start delimiter is being used to reset the disparity and to detect the signal polarity (therefore 2 groups of 4 start delimiters with different polarity and disparity exist).
- IDLE data consist of control information (e. g. 32 bit of control data) which are continuously repeated.
- Currently within the IDLE data only information about the actual training/link status are being transmitted.
- At least every 128 IDLE data bytes a new IDLE control sequence is being transmitted (Comma, EOC, SOC) to resynchronize in case of a receive error.
- If there is a continuous data transmission, the control sequences are transmitted within the interframe gap (96 bit times), so that no additional bandwidth is needed to transmit the control sequences.

Technical Data

- Link segment according to „Link Segment Baseline Proposal Industrial Applications“.

- Signal amplitude on the cable assuming 100 Ω characteristic impedance is 2.4 V_{pp} ± 120 mV.

- Voltage mode line driver to reduce the needed supply power of the output driver.

- Ternary 4B3T coded data stream.

Bit pattern	Disparity = 1	Disparity = 2	Disparity = 3	Disparity = 4
0000	+0+ (+2)	0-0 (-1)		
0001	0-+ (+0)			
0010	+-0 (+0)			
0011	00+ (+1)			--0 (-2)
0100	-+0 (+0)			
0101	0++ (+2)	-00 (-1)		
0110	-++ (+1)		--+ (-1)	
0111	-0+ (+0)			
1000	+00 (+1)			0-- (-2)
1001	+-+ (+1)			--- (-3)
1010	++- (+1)		+-- (-1)	
1011	+0- (+0)			
1100	+++ (+3)	-+- (-1)		
1101	0+0 (+1)			-0- (-2)
1110	0+- (+0)			
1111	++0 (+2)	00- (-1)		

- Signal level to symbol assignment:

  - +1.2 V → Logical +1

 - 0.0 V → Logical 0

  - -1.2 V → Logical -1

Technical Data

- Trapezoidal pulse shaping with a typical slew rate of 36 V/µs.
- Full Duplex data transmission over the link segment with echo cancelling.
- Scrambling of master and slave data stream to allow independent echo canceller and equalizer training.
- Master/Slave clock implementation:
  - The slave device adjusts its clock frequency and phase (including the propagation delay of the cable) to the master clock.
  - The master device has a fixed clock frequency and adjusts the receive phase depending on the cable propagation delay.
  - Tracking of cable's propagation delay change over temperature (typ. 50 ns for a 1000 m link segment from -40 to 70 °C).
- Maximum allowed clock tolerance including temperature: ± 50 ppm.
- Sequenced training (no need for special training symbols):
  - Clock Recovery
  - Clock Recovery + Echo Canceller (LMS Training)
  - Clock Recovery + Echo Canceller (LMS Training) + FSE (CMA Training)
  - Clock Recovery + Echo Canceller (LMS Training) + FSE (LMS Training) + DFE (LMS Training)
- Control information is being transmitted within the interframe gap between the Ethernet frames, not embedded within the normal data stream:
  - Easy synchronization due to unique comma sequences.
  - No additional bandwidth needed for control information coding.
  - Higher complexity, if forward error correction would be needed.
  - Breaking of the boundaries between PCS and PMA.
- No forward error correction being implemented.
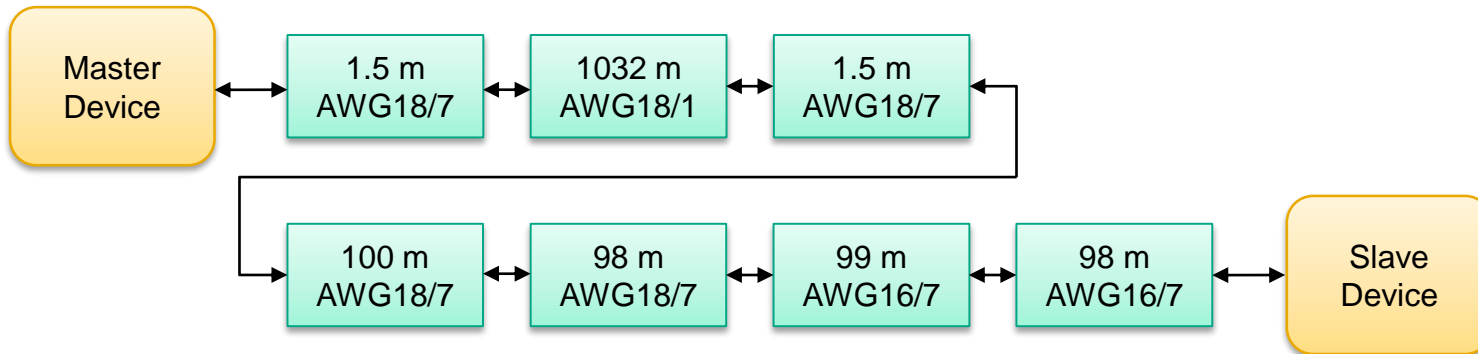- No auto negotiation being implemented.

Functional Testing
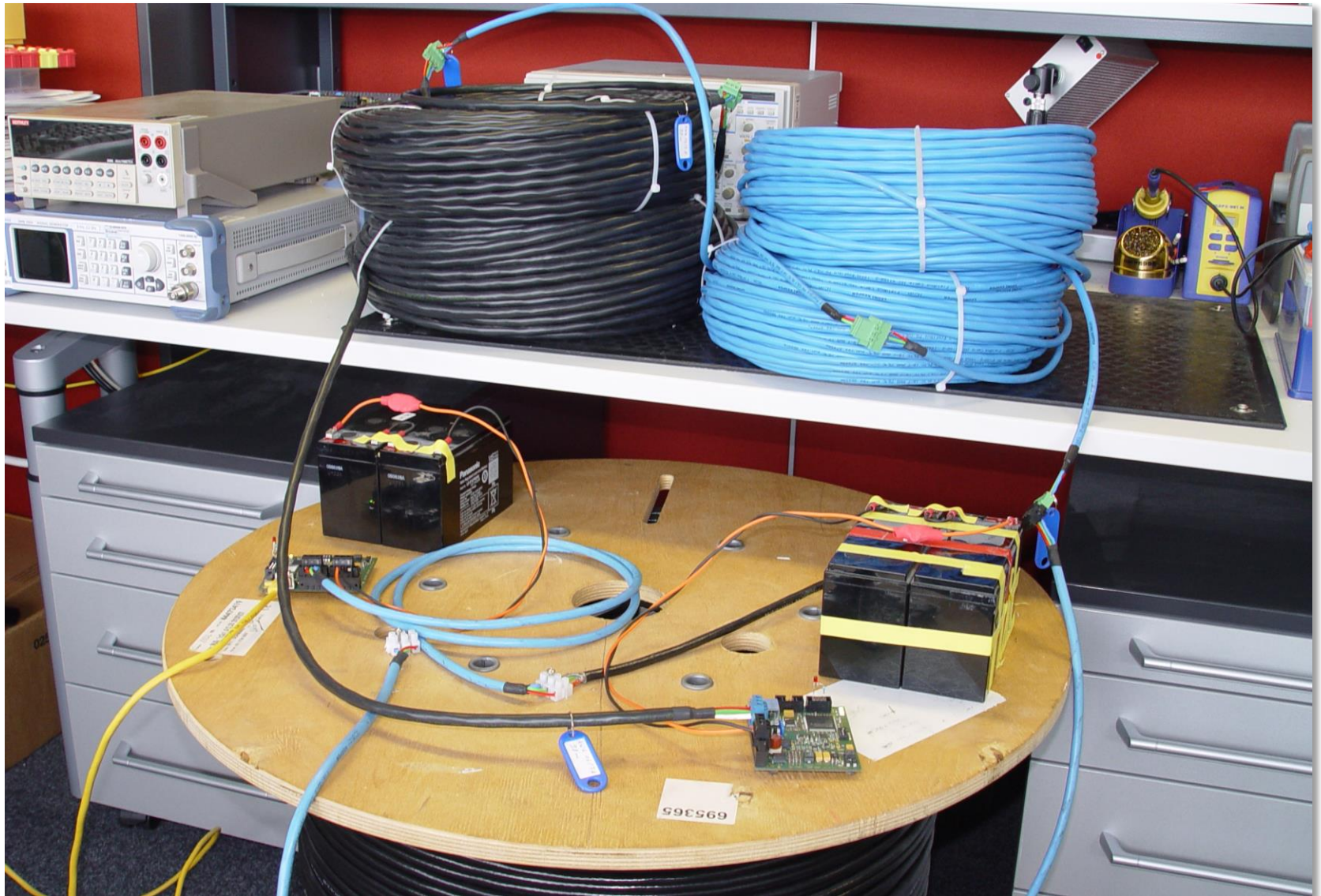
Functional Testing

- In a first step two evaluation boards have been connected to the 1032 m cable to see that an error free communication is possible.
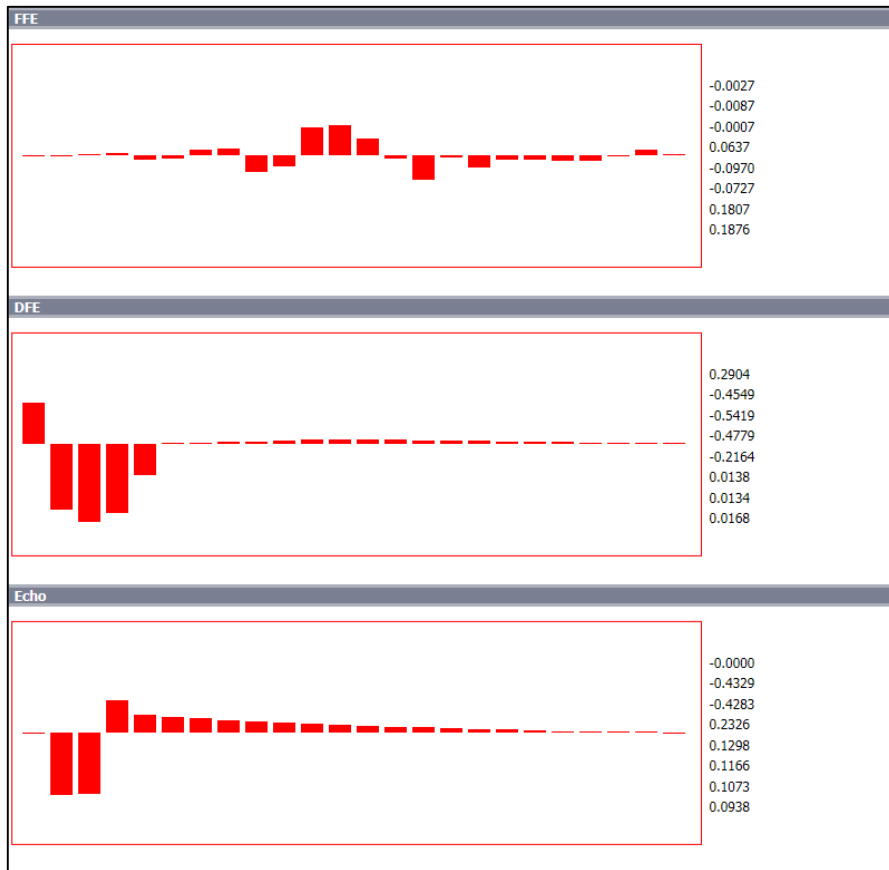
| Master Device | 1.5 m AWG18/7 | 1032 m AWG18/1 | 1.5 m AWG18/7 | Slave Device |
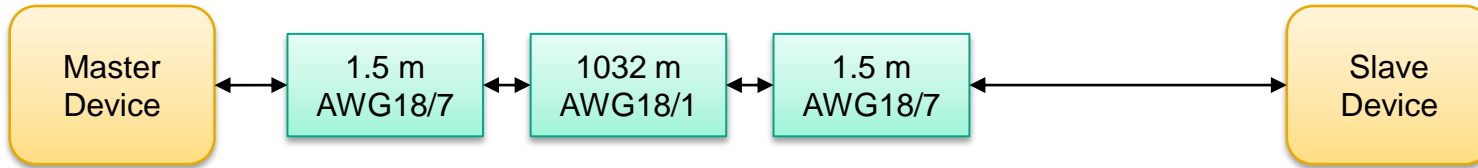
- Afterwards more cable rings of a length of approx. 100 m each have been added.
- The longest possible setup is being shown below.

| Master Device | 1.5 m AWG18/7 | 1032 m AWG18/1 | 1.5 m AWG18/7 |

| 100 m AWG18/7 | 98 m AWG18/7 | 99 m AWG16/7 | 98 m AWG16/7 | Slave Device |

- The total insertion loss of the link segment shown above is approximately 31 dB @ 3.75 MHz.
- Within some minutes no communication error could be observed.

Functional Testing

FFE

	-0.0027
	-0.0087
	-0.0007
	0.0637
	-0.0970
	-0.0727
	0.1807
	0.1876

DFE

	0.2904
	-0.4549
	-0.5419
	-0.4779
	-0.2164
	0.0138
	0.0134
	0.0168

Echo

	-0.0000
	-0.4329
	-0.4283
	0.2326
	0.1298
	0.1166
	0.1073
	0.0938

APL Link

APL Mode:	Master	μ FFE:	0.009999
PWM (Slave):	128	μ DFE:	-0.000999
Phase (Master):	112	μ Echo:	0.000010
Signal Quality:	0.000527	P1:	0.000000
AGC:	6.766357	I1:	0.000000
Idle Data:	3	P2:	0.000000
ADC Average:	522	I2:	0.000000
ADC Vref [mV]:	1000	Modulus:	1
Inv. Polarity:	1		

Errors

Link Loss (Uplink):	0	4B3T Errors:	0
Link Loss (Clock):	0	Buffer Overflows:	0
Link Loss (Edge Detector):	0	Protocol Violations:	0
Link Loss (Signal Quality):	0	ADC Spikes:	0
Link Loss (AGC):	0	Slicer Spikes:	0
Link Loss (Idle Data):	0	Clock Losses:	0

Statistics

Tx Requests:	682	Rx Packets:	636
Tx Queued Requests:	12	Rx Bytes:	59938
Tx Done:	682	Rx Mem Errors:	0
Tx Sent From Done:	12		
Tx Bytes:	46598		

- An integrated webserver provides a graphic representation of the filter coefficients, some information about the PHY status and several error counters.

EMC Testing

- EMC test levels according to EN 61326-1 (electrical equipment for measurement, control and laboratory use) and NE 21 (practical procedures for determining whether the devices used in laboratory and process control are immune to interference) are being used.

- Each device has an error output connected to a LED or an optical transmitter, which is set for about 1 s after a bit error has been detected.

- This failure output can be used to visually observe if there are bit errors or to regulate the measurement setup.

- Additionally ICMP packets have continuously been transmitted between a notebook, being connected to the RJ45 port of the master device, and the slave device.

- For communication with the slave device „fping" has been used with the following parameters: fping.exe x.x.x.x -s 1024 -t 0 -w 50 -c, where x.x.x.x is the IP address of the slave device.

- EFT
  - 1 kV, 5 kHz (15 ms/300 ms), 100 kHz (0.75 ms/300 ms)
- Conducted Immunity
  - 10 V/m, 10 kHz to 80 MHz

- Radiated Immunity, ESD and Surge testing have not yet been performed.

EFT Test Setup
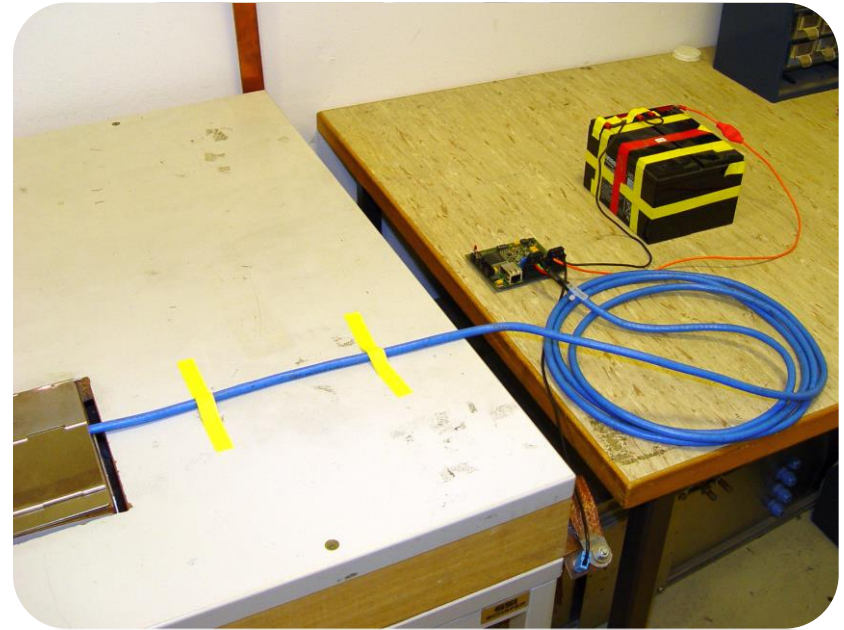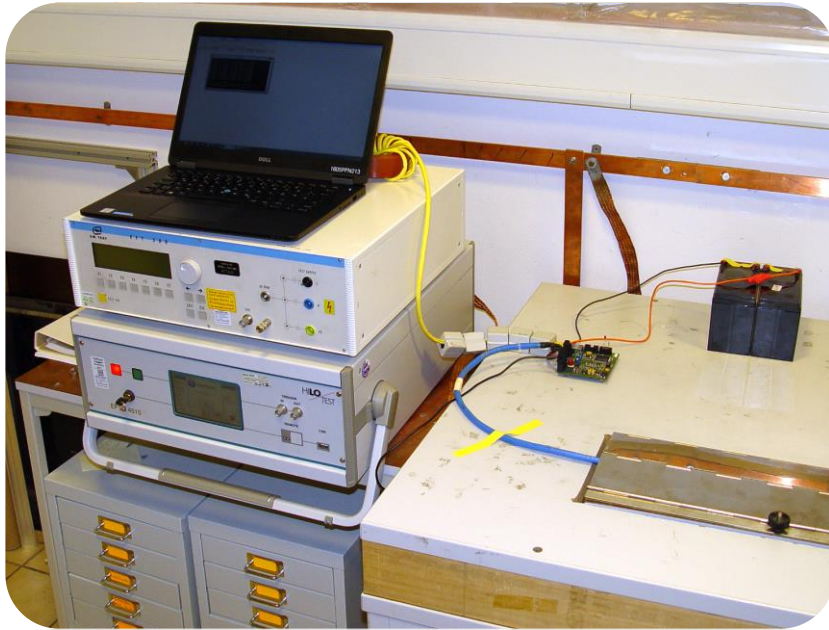
- Required level for EFT testing is 1 kV (1.1 kV including some safety margin for tolerances).
- EFT has been measured with 2.2 kV (two times the required test level) coupled to the EFT test clamp.
- EFT testing has been done for both polarities with the following parameters with 120 s measurement time:
  - 5 kHz/15 ms/300 ms (standard EFT)
  - 5 kHz/15 ms/20 ms (lowest period, which could be set at the burst generator)
  - 100 kHz/0.75 ms/300 ms (new higher frequency EFT, which will be demanded by NE21 in the future)
  - 100 kHz/0.75 ms/10 ms (lowest period, which could be set at the burst generator)
- The cable shield at the DUT side has been hard or capacitive grounded, while the cable shield at the auxiliary device side has been hard grounded.

EFT Test Results

- DUT is the master device, auxiliary device is the slave device:

2.2 kV - 5 kHz/15 ms/300 ms EFT		
Polarity	Shield hard grounded	Shield capacitive grounded
+	0 packets lost	0 packets lost
-	0 packets lost	0 packets lost

2.2 kV - 5 kHz/15 ms/20 ms EFT		
Polarity	Shield hard grounded	Shield capacitive grounded
+	0 packets lost	0 packets lost
-	0 packets lost	0 packets lost

2.2 kV - 100 kHz/0.75 ms/300 ms EFT		
Polarity	Shield hard grounded	Shield capacitive grounded
+	0 packets lost	0 packets lost
-	0 packets lost	0 packets lost

2.2 kV - 100 kHz/0.75 ms/10 ms EFT		
Polarity	Shield hard grounded	Shield capacitive grounded
+	0 packets lost	0 packets lost
-	0 packets lost	0 packets lost

EFT Test Results

- DUT is the slave device, auxiliary device is the master device:

2.2 kV - 5 kHz/15 ms/300 ms EFT		
Polarity	Shield hard grounded	Shield capacitive grounded
+	0 packets lost	0 packets lost
-	0 packets lost	0 packets lost

2.2 kV - 5 kHz/15 ms/20 ms EFT		
Polarity	Shield hard grounded	Shield capacitive grounded
+	0 packets lost	0 packets lost
-	0 packets lost	0 packets lost

2.2 kV - 100 kHz/0.75 ms/300 ms EFT		
Polarity	Shield hard grounded	Shield capacitive grounded
+	0 packets lost	0 packets lost
-	0 packets lost	0 packets lost

| 2.2 kV - 100 kHz/0.75 ms/10 ms EFT		
Polarity	Shield hard grounded	Shield capacitive grounded
+	0 packets lost	0 packets lost
-	0 packets lost	0 packets lost

EFT Test Results

- In all previous tests no bit errors, no link loss and no loss of the clock synchronization have been observed.

- To see the influence of the capacitive/hard grounded shield, in a next step the shield has been capacitive grounded on the auxiliary device and the shield connection has been completely removed on the DUT, even if this is not the intended shielding option for the link segment.

- The following table shows the results for the master and the slave device for a test voltage of 1.1 kV using a standard EFT test:

1.1 kV - 5 kHz/15 ms/300 ms EFT		
Polarity	Master device	Slave device
+	10 % packets lost	11 % packets lost
-	11 % packets lost	10 % packets lost

- The failure outputs on both devices have been activated, but no link loss and no loss of the clock synchronization have been observed.
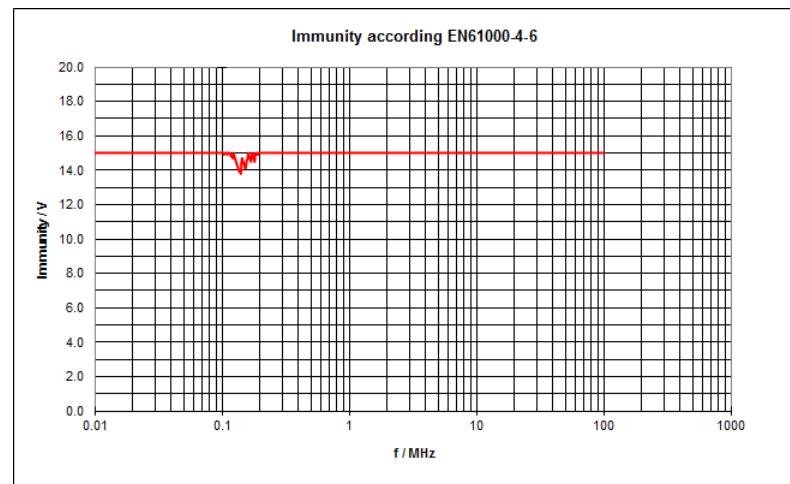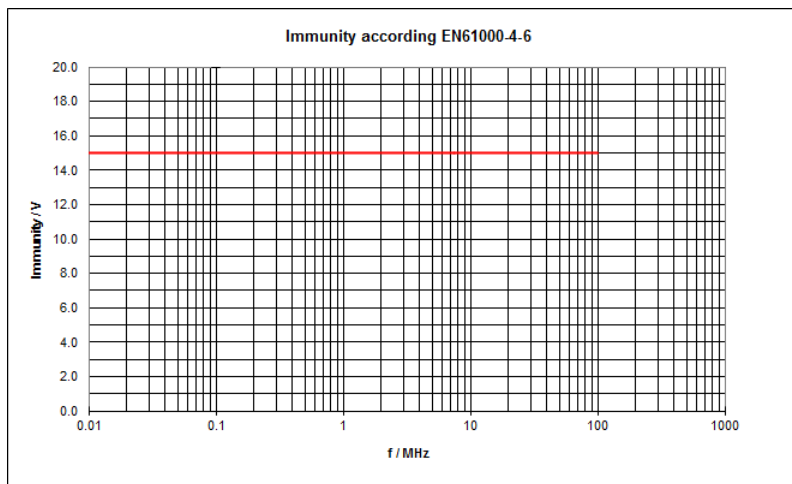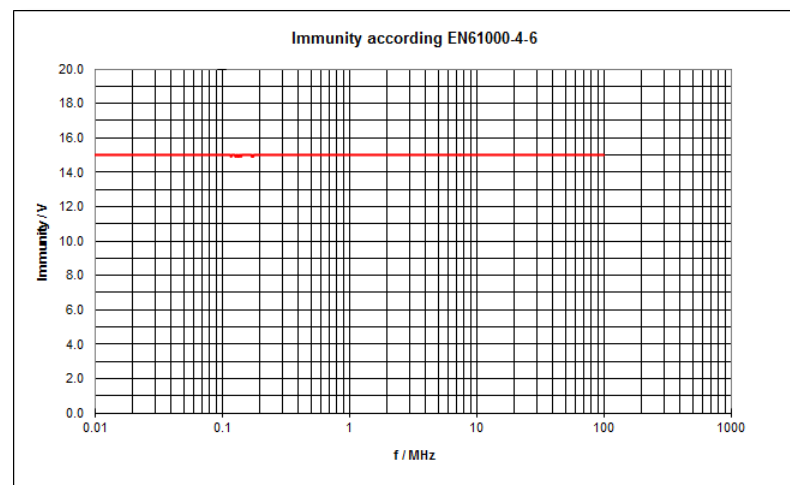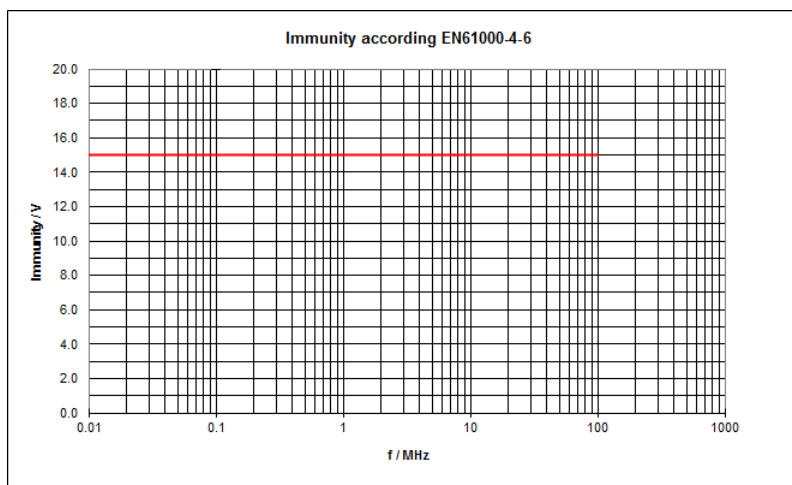
Conducted Immunity Test Setup
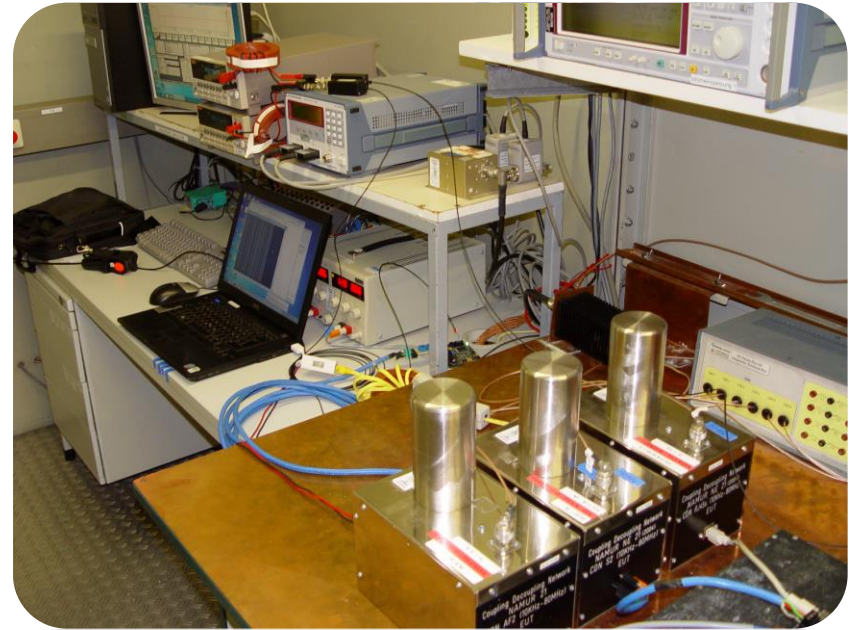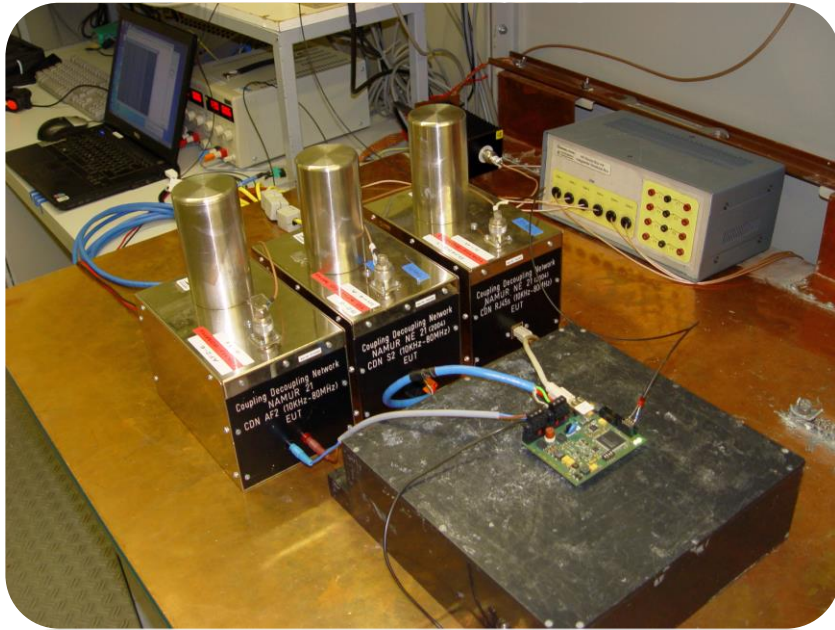
- Conducted immunity has to be tested with a logarithmic frequency sweep (1 % frequency increase per step) between 10 kHz and 80 MHz with an amplitude of 10 V (IEC/EN 61326 and NE21).
- The conducted immunity interferer signal amplitude is regulated by an optically isolated error output of the DUT.
- The following CDNs are used for the different connections to the evaluation board:
  - AF2 CDN for the power lines
  - S2 CDN for the 10SPE port
  - S8 CDN with RJ45 connection for the 10/100 MBit/s Ethernet port
- The S2 CDN is intended to be used with a hard grounded shield connection at the DUT only.
- In case a capacitive shield connection is being used at the DUT side, there is need for additional decoupling with a current compensated choke at the auxiliary device side to prevent resonance effects between the current compensated choke within the S2 CDN and the system on the decoupled side of the CDN in the lower frequency range.

Conducted Immunity Test Results

- Measurement results for master device (hard (left diagram) / capacitive (right diagram) grounded shield):


- Measurement results for slave device (hard (left diagram) / capacitive (right diagram) grounded shield):

Conducted Immunity Test Results

- Conducted immunity testing has been passed with 15 V as long as the cable shield is hard grounded on the DUT side.
- Conducted immunity testing has been passed with more than 13 V as long as the cable shield is capacitive grounded on the DUT side using a 4.7 nF Y2 capacitor.
- Using capacitive shield grounding the critical frequency range is between approx. 100 kHz and 200 kHz, which is mainly caused by the S2 CDN's integrated current compensated choke and which is below the 10SPE signal frequency range.
- Reason for this is that a S2 CDN is normally being used with a hard grounded shield connection at the DUT side, so that the interference current injected by the frequency generator of the test system is flowing over the cable shield to the DUT and from there to ground.
- If there is only a capacitive grounding at the DUT using a 4.7 nF ceramic capacitor, at lower frequencies a part of the interference current is flowing through the current compensated choke built into the S2 CDN and from there over the cable to the auxiliary device (on the decoupled side) causing some resonance effects in the lower frequency range.

Noise Test Setup
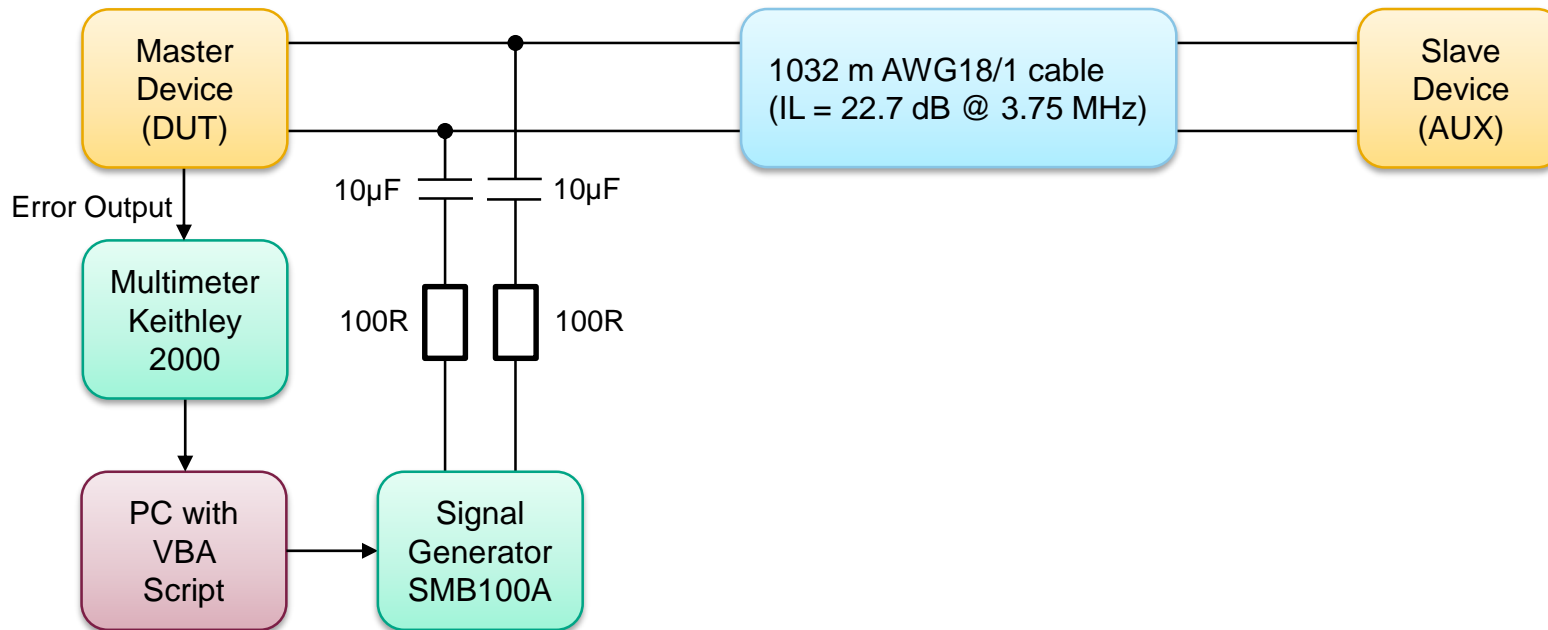
- A signal generator with an internal impedance of 50 ohms is simulating a sine wave interferer.
- Together with the external 2 x 100 ohms resistors, the internal termination resistor of the DUT of 100 ohms and the cable characteristic impedance of about 100 ohms, a voltage divider of approx. 1 : 6 is formed.
- The attenuator within the signal generator is set to a fixed level to prevent disturbances from the attenuator being switched when adjusting the signal amplitude.
- The bit error output of the DUT is sampled with a multimeter.
- Depending on the status of the error output the signal amplitude of the function generator is controlled by an Excel VBA script running on a PC.
- This script is also being used to subsequently measure the different predefined frequencies between 100 kHz and 20 MHz.

Noise Test Setup

- For each frequency the initial sine wave noise amplitude has been set to 30 mV$_{pp}$.
- After each second the noise amplitude has been increased by 20 % until the first bit error occurred or a maximum noise amplitude at the DUT of 1 V$_{pp}$ has been reached.
- After an error has occurred or the maximum noise amplitude has been reached, the next frequency value has been measured.
- For each frequency a correction factor for the signal generator output amplitude has been taken into account, to cover the DUT impedance tolerances, the cable characteristic impedance tolerances and the signal generator output tolerances.
- During the following tests the training of the echo canceller and the equalizer has been enabled.
- The measurement has to be done several times to get the minimum noise tolerance.
- Depending on some tolerances during the training, the phase difference between the interferer and the communication signal and the actual data sequence, there are differences between the individual measurement runs.

Noise Test Setup

Noise Test Results
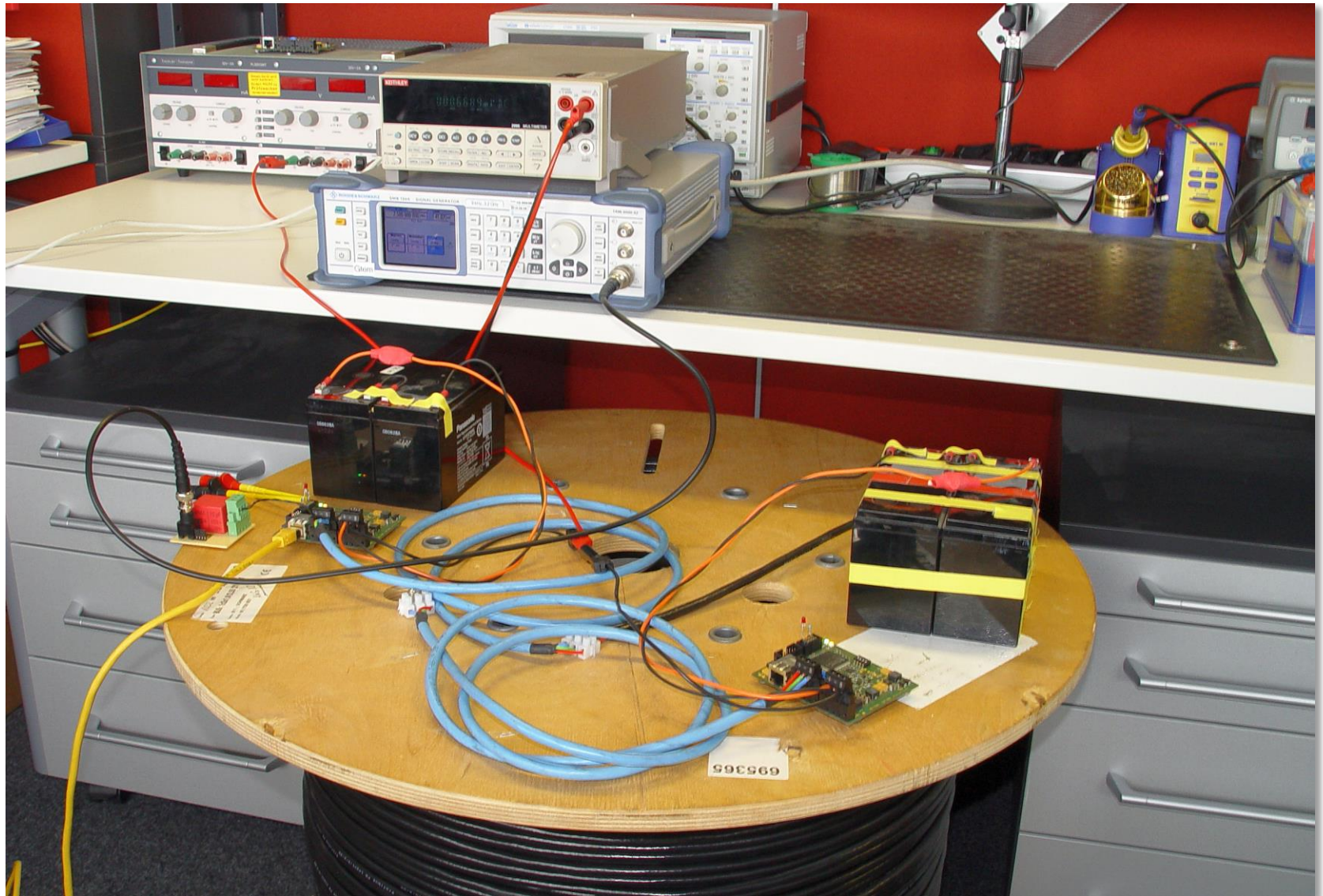
Sine Wave Noise Tolerance
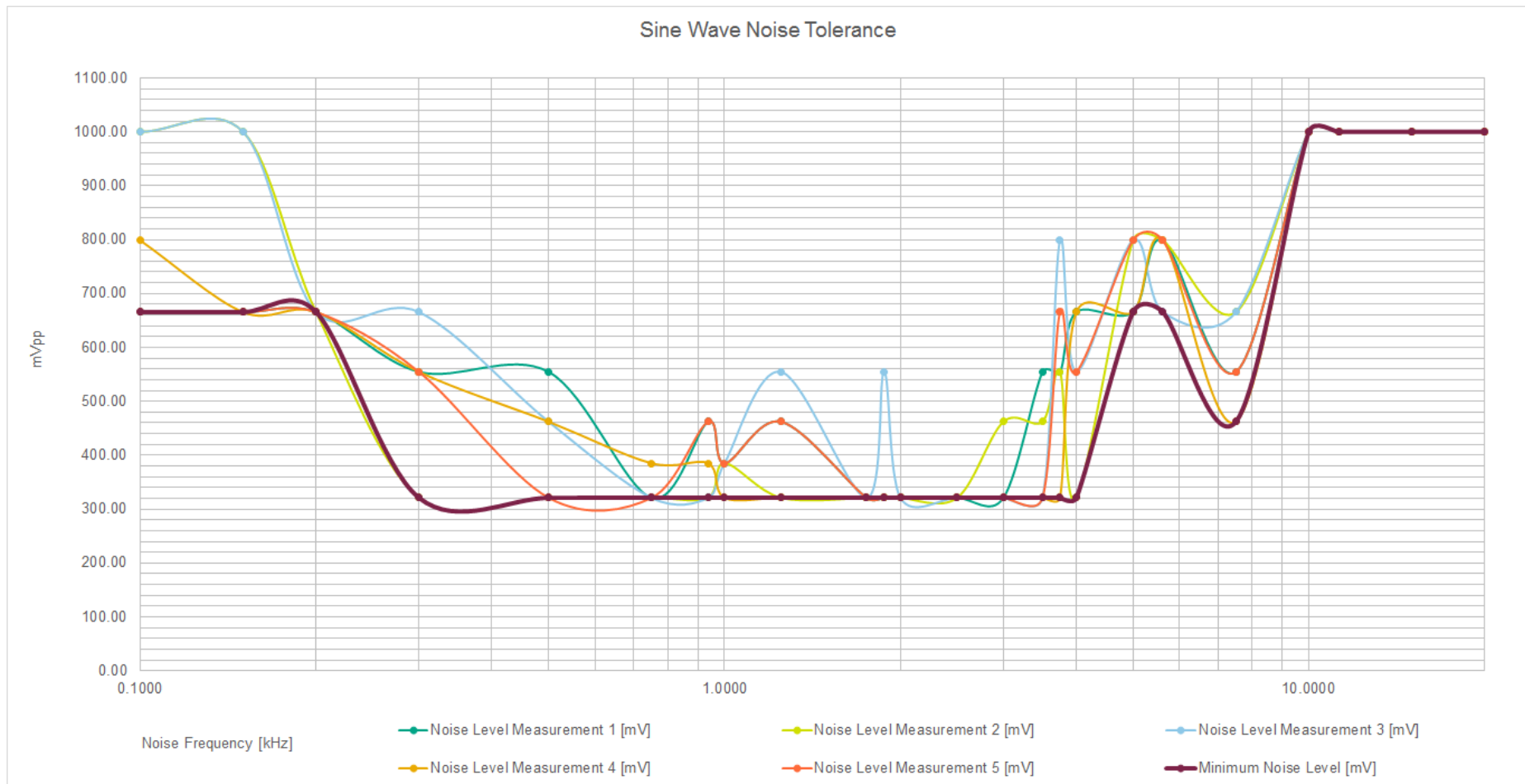
- The sine wave noise measurement has been done five times.
- The thicker red curve shows the minimum sine wave noise tolerance out of these five measurements.
- Minimum sine wave noise tolerance with active training is about 300 mV$_{pp}$.

Noise Test Results

- The previous measurement shows the tolerance against a slowly changing narrow band sine wave interferer.
- Therefore these results are valid, if the interferer changes in such a slowly manner that the filter coefficient training is fast enough to follow the external interferer.

- To see which noise level for a fast changing sine wave interferer is possible, the amplitude has been fixed and a continuous fast stepping of the frequencies has been done.
- Each frequency has been applied for 100 ms, then a noise pause of 900 ms has been applied and then the next frequency has been used.
- Most critical point is directly after switching on the noise at the new frequency, while the equalizer is not yet trained to the new noise situation.
- From that point on the equalizer training takes place and the SNR at the slicer gets better over time.
- After the highest frequency has been applied, the measurement continued again with the lowest frequency.
- As noise frequencies the same measurement frequencies as shown in the previous slide have been used.
- The LEDs at the bit error outputs of the master and the slave device have been observed and as soon as one of these LEDs has been activated a lower interferer level has been applied, until the LEDs were kept in off state.

- The noise tolerance of a narrow band sine wave interferer in this scenario has been **40 mV$_{pp}$** directly at the DUT port.

Thank You