10 Mb/s Single Twisted Pair Ethernet

PAM-3 PHY Baseline Proposal

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Isolation Requirements

- **It is proposed to have an optional galvanic isolation.**

- Depending on the application a galvanic isolation between the device circuits and the MDI leads, including frame ground can be required.

- Where such an isolation is required, the insulation shall meet the minimum application requirements or at least one of the following requirements (see e.g. clause 55.5.1):

  - 1500 V AC, 50 to 60 Hz for 1 minute
  - 2250 V DC for 1 minute
  - 10 times 2400 V, 1.2/50 µs surge pulses

- There can also be applications, where only an isolation between the trunk and a spur group, but not between different spurs is required, e.g. if all output voltages are electrically safe and there are no bigger potential differences.
- This practice is identical to current industrial installations.
- In this case the isolation requirements relate to the isolation between the trunk and the spur group, but there is no need for an additional galvanic isolation between the different spurs of this spur group, which would otherwise lead to a significant additional effort for isolating the data signals and power.

Modulation

- **It is proposed to use a PAM-3 with logical +1, 0 -1 as modulation.**

- A PAM-3 modulation is robust to implement and provides a coding of 1.58 bit/symbol, thus reducing the needed bandwidth.
- Transmitting of only three different levels within a symbol provides an acceptably high margin in the receive signal to distinguish the different symbol levels after applying the link segment's insertion loss.

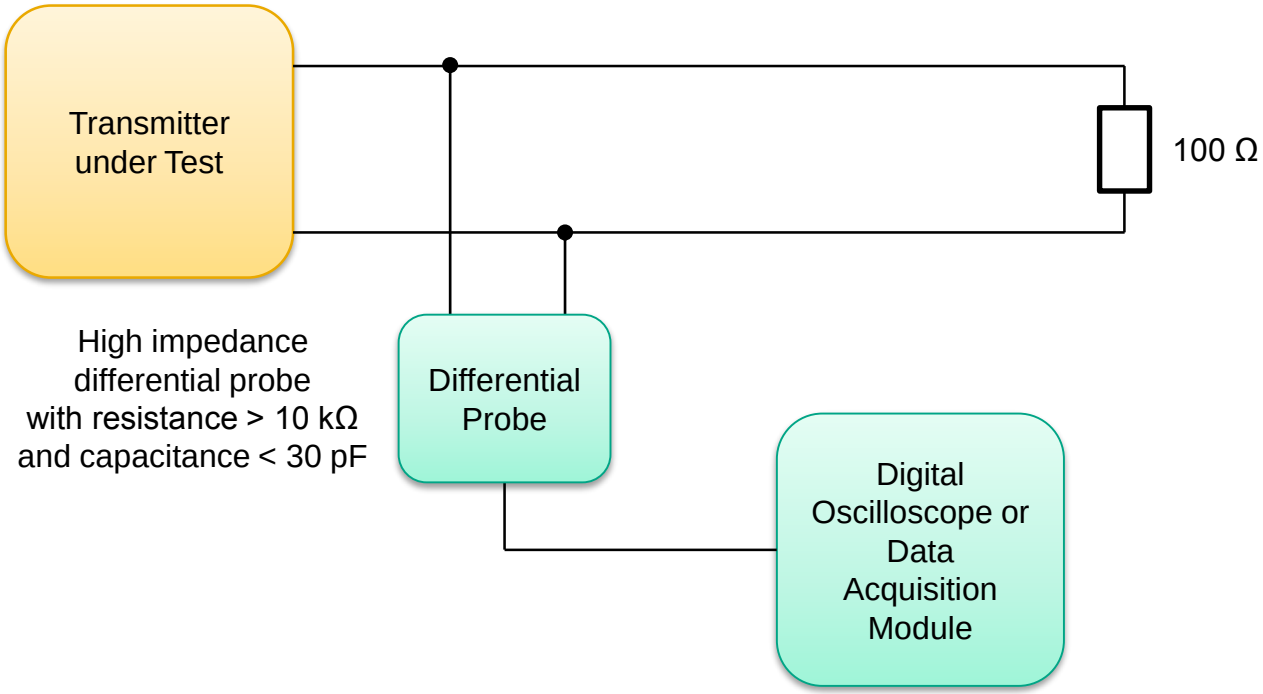
Symbol Rate

- **It is proposed to use a symbol rate of 7.5 MSymbols/s.**

- A symbol rate of 7.5 MSymbols/s leads to a Nyquist frequency of the communication signal of 3.75 MHz, which provides an acceptably low insertion loss applying the baseline model for the link segment.
- This symbol rate can be easily generated from standard oscillator values using PLLs with low nominator/denominator values, thus reducing the needed energy: 10 MHz (× 3 ÷ 4), 12 MHz (× 5 ÷ 8), 16 MHz (× 15 ÷ 32), 25 MHz (× 3 ÷ 10), 33 MHz (× 5 ÷ 22)
- As all denominator values are at least one time dividable by a factor of two, it is also easily possible to use a low speed PLL for a two times oversampled system.
- A symbol rate of 7.5 MSymbols/s compared to a minimum needed symbol rate for a PAM-3 of 6.31 MSymbols/s allows to use a 4B3T coding or alternatively a PCS block encoding with a maximum overhead of 18.87 %.

Transmitter Test Setup

- **It is proposed to use the following test setup for the subsequent transmitter tests.**



- The test setup is similar to the test setup described in clause 97.5.2.1.

Amplitude for Link Segments up to 1000 m

- **It is proposed to transmit with a peak-to-peak signal amplitude of 2.40 V ± 120 mV into 100 Ω for the 1000 m link segment.**

- To reduce the energy consumption of the line driver a voltage mode driver seems to be suitable in most cases, which due to the needed series termination internally has to drive two times the signal amplitude on the port side.
- Assuming a 3.3 V supply voltage for the PHY chip, theoretically a maximum peak-to-peak signal amplitude of 3.3 V at the port side would be possible.
- Nevertheless the output drivers need some headroom and also the supply voltage of the PHY chip has some tolerances, so that the maximum output amplitude is being limited to lower values using a low power standard driver output stage without integrated charge pumps.
- Therefore a maximum peak-to-peak signal amplitude of 2.40 V seems to be a good compromise.
- A reasonable tolerance of the peak-to-peak amplitude is assumed to be ± 5 % (± 120 mV), which is similar to other Ethernet PHYs.

Amplitude for Link Segments up to 200 m

- **It is proposed to transmit with a peak-to-peak signal amplitude of 1.00 V ± 50 mV into 100 Ω for the 200 m link segment.**

- The signal amplitude on a link segment up to 200 m may be reduced to a peak-to-peak amplitude of 1.00 V due to the much lower insertion loss of the 200 m link segment.
- This is necessary for intrinsically safe link segments including power to limit the maximum peak voltage, including DC power.
- A reasonable tolerance of the peak-to-peak amplitude is assumed to be ± 5 % (± 50 mV), which is similar to other Ethernet PHYs.

Signal Rise and Fall Times

- **It is proposed to have a nominal rise time of the signal of 53.333 ns ± 10 % for a -1 to +1 and a nominal fall time of the signal of 53.333 ns ± 10 % for a +1 to -1 transition.**

- As the rise and fall times are specified between 10 % and 90 % of the signal amplitude, assuming a linear transition between 0 % and 100 %, this equals to a time of 66.667 ns, which is half of the symbol time.
- The absolute value of the nominal slew rate for a peak-to-peak signal amplitude of 2.4 V is 36 V/µs ± 10 %.
- The absolute value of the nominal slew rate for a peak-to-peak signal amplitude of 1.0 V is 15 V/µs ± 10 %.
- For 0 → +1, +1 → 0, 0 → -1 and -1 → 0 transitions the same slew rates apply.
- Below 10 % and above 90 % of the signal amplitude a lower slew rate is acceptable, to consider the lower speed of the output driver when operating near to its supply rails.

Clock Tolerance

- **It is proposed to transmit at the master side with a symbol clock of 7.5 MHz ± 0.005 %.**

- Using the same oscillator tolerance as for other 10/100 Mbit/s Ethernet PHY ICs.
- An oscillator tolerance of ±50 ppm including initial tolerance, temperature variation, ageing, shock and vibration allows usage of PLL based as well as VCXO based clock recovery circuits.

Jitter Tolerance

- **It is proposed to allow a maximum jitter at the transmitter side of ±10 ns symbol-to-symbol jitter when driving into 100 Ω.**

- The nominal symbol time at 7.5 MSymbols/s is 133.333 ns.
- A symbol-to-symbol jitter of ±10 ns leads to a symbol duration between 123.333 ns and 143.333 ns.
- A symbol-to-symbol jitter of ±10 ns is a relative jitter of ±7.5 %.

Normalized Test Patterns for Transmitter

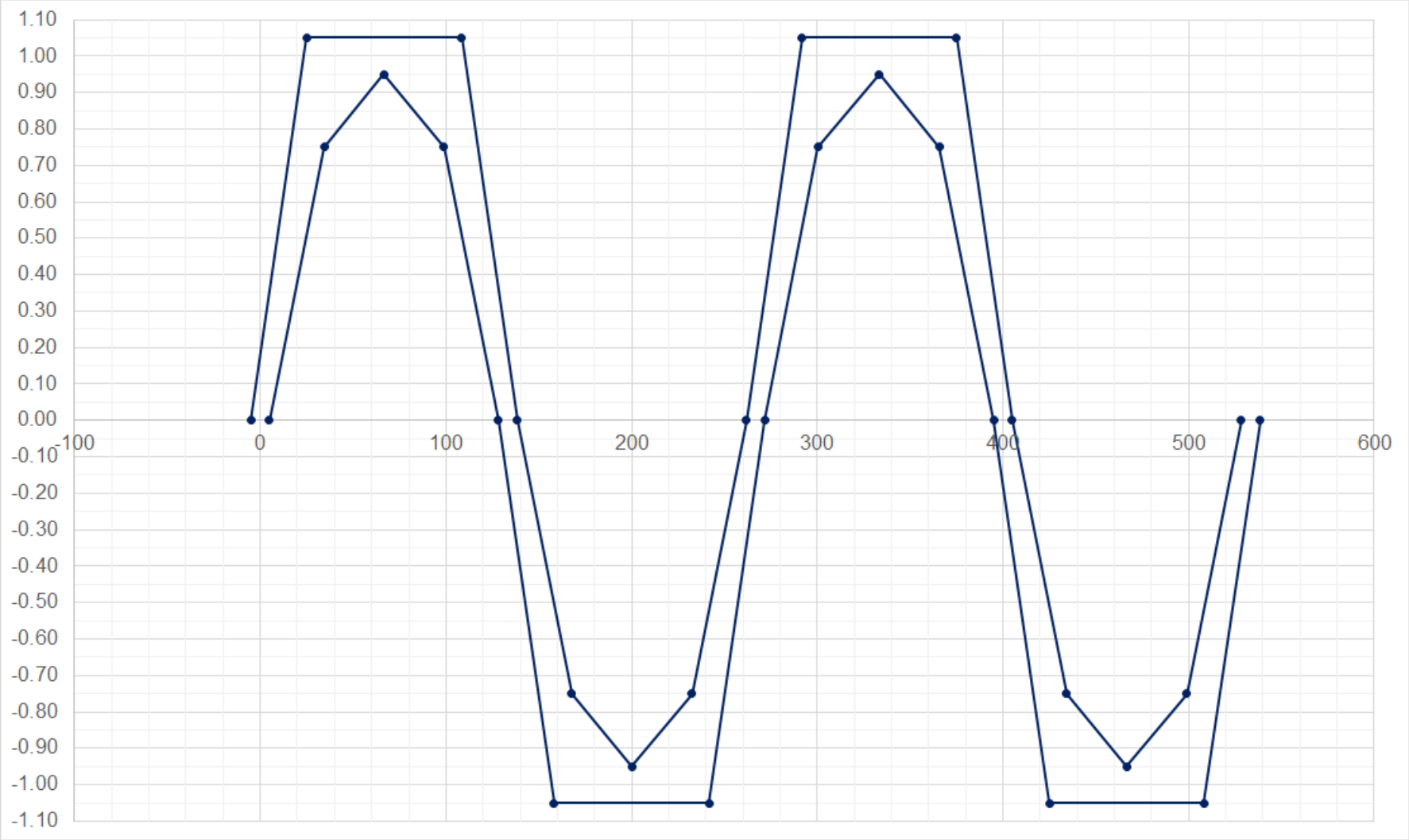
- **It is proposed to use two different test patterns for the transmitter driving into a 100 Ω load to check the transmitter's output specification.**

- The first test pattern is an alternating +1, -1 sequence.
- This test pattern can be used to see, if the nominal signal amplitude is within the specified range and if the specified rise and fall times are being met.

- The second test pattern is a sequence transmitting 10 symbols +1 and then 10 symbols -1 in an alternating way.
- This test pattern can be used to see, if the components of the coupling network between the PHY chip and the link segment as well as the components of the power injection network between the power supply and the link segment are within the desired range.
- Depending on the used PCS coding, an adoption of this test would be necessary.

Normalized Test Patterns for Transmitter

- **First Test Pattern (waveform, normalized amplitude, time scale in ns):**



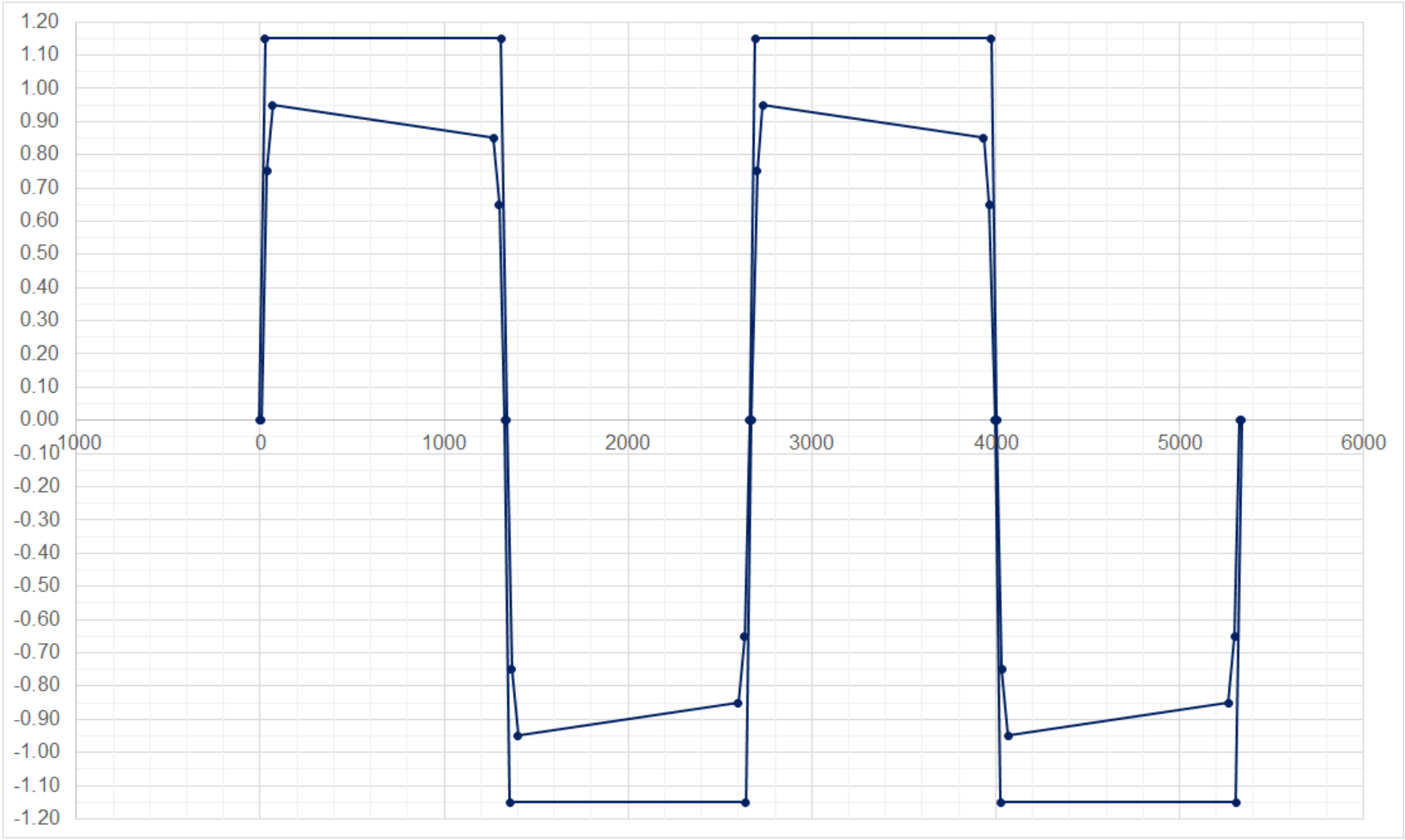
Normalized Test Patterns for Transmitter

- **First Test Pattern (table):**

Limit 1 Time [ns]	Limit 1 Normalized Amplitude	Limit 2 Time [ns]	Limit 2 Normalized Amplitude
-5.000	0.00	5.000	0.00
25.000	1.05	34.333	0.75
108.333	1.05	66.667	0.95
138.333	0.00	99.000	0.75
167.667	-0.75	128.333	0.00
200.000	-0.95	158.333	-1.05
232.333	-0.75	241.667	-1.05
261.667	0.00	271.667	0.00
291.667	1.05	300.333	0.75
375.000	1.05	333.333	0.95
405.000	0.00	365.666	0.75
434.333	-0.75	395.000	0.00
466.667	-0.95	425.000	-1.05
499.000	-0.75	508.333	-1.05
528.333	0.00	538.333	0.00

Normalized Test Patterns for Transmitter

- **Second Test Pattern (waveform , normalized amplitude, time scale in ns):**



Normalized Test Patterns for Transmitter

- **Second Test Pattern (table):**

Limit 1 Time [ns]	Limit 1 Normalized Amplitude	Limit 2 Time [ns]	Limit 2 Normalized Amplitude
-5.000	0.00	5.000	0.00
25.000	1.15	34.333	0.75
1308.333	1.15	66.667	0.95
1338.333	0.00	1266.667	0.85
1367.667	-0.75	1299.000	0.65
1400.000	-0.95	1328.333	0.00
2600.000	-0.85	1358.333	-1.15
2632.333	-0.65	2641.667	-1.15
2661.667	0.00	2671.667	0.00
2691.667	1.15	2701.000	0.75
3975.000	1.15	2733.333	0.95
4005.000	0.00	3933.333	0.85
4034.333	-0.75	3965.667	0.65
4066.667	-0.95	3995.000	0.00
5266.667	-0.85	4025.000	-1.15
5299.000	-0.65	5308.333	-1.15
5328.333	0.00	5338.333	0.00

Full Duplex Operation

- **It is proposed to support full duplex operation with echo cancelling on the link segment only for the 200 m and 1000 m link segments.**

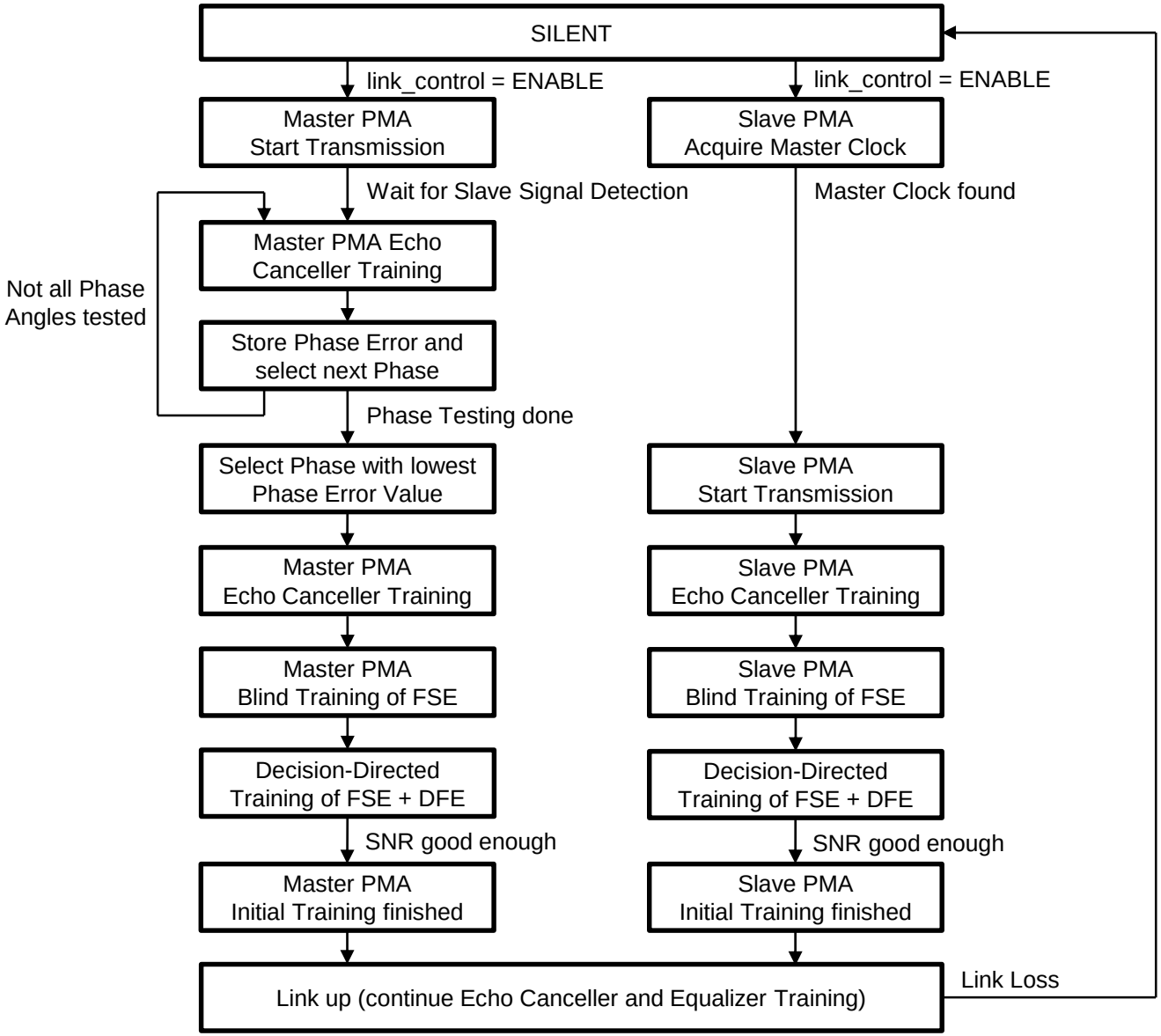
- On the link segment only full duplex operation with continuous echo cancelling is being supported using a continuous symbol stream.
- No block oriented communication or half duplex operation will be supported physically on the link segment for the 200 m or 1000 m.
- On the MII interface a „simulated“ half duplex mode will be possible.

Blind Link Training

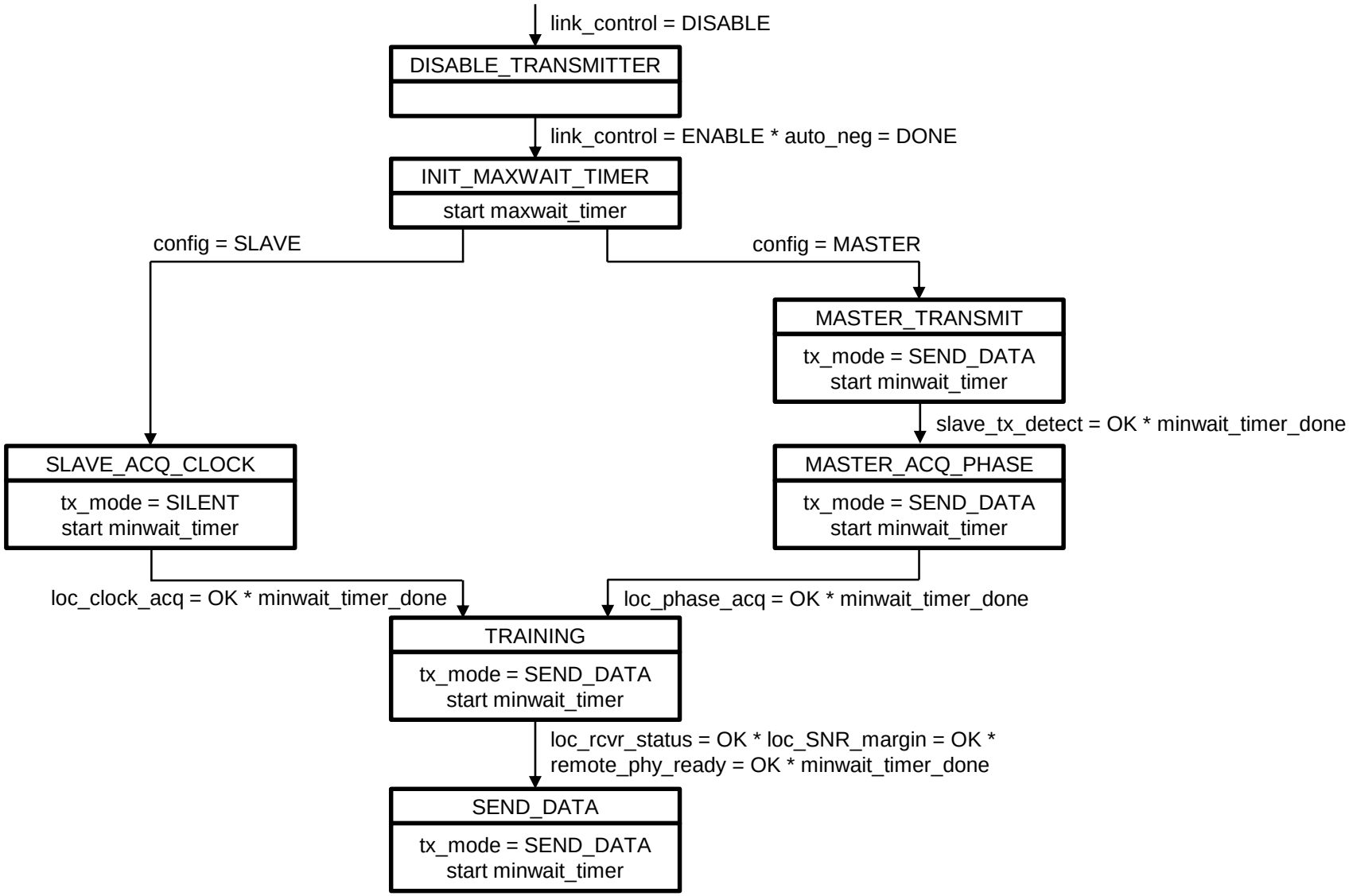
- **Suggested is to use a blind link training without the need for dedicated training sequences.**

- Implementing initial blind training of the equalizer simplifies the training sequence.
- After a good enough SNR is being reached, it is switched from blind training to decision-directed training.
- Master and slave independently decide when to switch from blind to decision-directed training.

Implemented Link Training State Machine



PHY Control State Diagram



PCS Block Encoding

- **It needs to be discussed how to implement a block based encoding within the PCS to be able to provide a continuous data stream to the PMA.**

- Currently a 4B3T coding in combination with a self-synchronizing scrambler is being used on the PCS layer, which is a simple encoding limiting the lower frequency content of the signal and therefore the baseline wander on the link segment.
- Due to the 4B3T coding special comma sequences are needed to synchronize the bit stream on the PMA layer.
- Therefore currently the boundary between the PCS and the PMA is not as clear as it is used to be for modern PHY implementations.

- One idea would be to use a 64B/66B or similar encoding in combination with a self-synchronizing scrambler to limit the low frequency content of the bit stream to similar values as for the 4B3T code and therefore keeping the BLW on the link segment adequately low.
- An efficient way to code the binary data stream into PAM-3 symbols needs to be found.
- Depending, if a FEC is needed or not, there should be enough headroom to also add a not too complex (optional) FEC.

Thank You