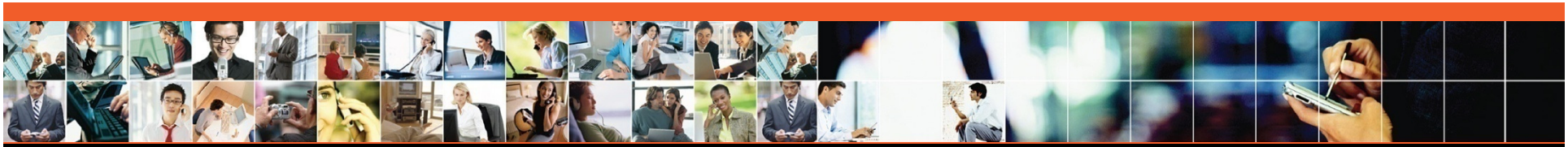

Line Codes and Block Codes Primer

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Modulation / Line Codes

- Modulation at the transmitter
  - Typically PAMx
  - Line code maps data bits to transmit symbols
- 802.3 examples
  - NRZ/PAM2 for SERDES
  - PAM3: 4B3B for 100BASE-T1, 3B2T for 1000BASE-T1, MLT3 for 100BASE-TX
  - PAM5 for 1000BASE-T
  - PAM16 for 2.5GBASE-T
- higher # of levels
  - lower baud rate
  - increased sensitivity to noise (line noise, crosstalk, RS, CS)
  - more bit errors per symbol error
- fewer # of levels
  - higher baud rate
  - decreased sensitivity to noise, better for decision feedback equalizers
  - fewer bit errors per symbol error

Block codes

- Block code purpose
  - map the MII symbols into bits for transmitting
  - compress # of bits needed to represent the MII signals,
    - Start of Packet, End of Packet, Idle, Low Power Idle, TX_ER (transmit error), TX_EN (transmit enable)
  - transport link status information
    - XGMII: Local Fault, Remote Fault, Link Not Available, Low Power Idle

Block codes – 8B10B

- 8B10B – 1000BASE-X SERDES
  - Per byte coding
  - DC balanced signaling
    - disparity rules for DC balance
  - maps GMII
    - Start of Packet, End of Packet, Transmit Error, Low power Idle, Idle, Confuration (auto-negotiation)
    - for half duplex: Carrier Extend, Carrier Extend Error,
  - block alignment indication during idle
  - minimal error detection ability
  - no data scrambler required

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D0.0	00	000 00000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100
D4.0	04	000 00100	110101 0100	001010 1011
D5.0	05	000 00101	101001 1011	101001 0100
D6.0	06	000 00110	011001 1011	011001 0100
D7.0	07	000 00111	111000 1011	000111 0100
D8.0	08	000 01000	111001 0100	000110 1011
D9.0	09	000 01001	100101 1011	100101 0100

Block codes – 64B66B

- 64B66B
  - 10GBASE-R SERDES
  - 8 byte block code
  - 2 bit header for block alignment indication
  - maps XGMII
    - Start of Packet, End of Packet, Transmit Error, Low power Idle, Idle, Local Fault, Remote Fault, Link Not Available,
  - requires data scrambler
  - minimal error detection ability

Input Data	Sync	Block Payload							
Bit Position: / Data Block Format:	0 1	2							65
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	01	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block Type Field							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x1e	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	10	0x2d	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	10	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	10	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	10	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	10	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	10	0x4b	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	10	0xaa	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	10	0xb4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	10	0xcc	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	10	0xd2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	10	0xe1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	10	0xff	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Block codes – nB(n+1)B

- nB(n+1)B
  - single header bit indicates if entire block is data only
  - remaining bits may be data only or control words only or mixed data/control
  - relies on FEC to prevent error propagation / undetected frame error
  - requires data scrambler
  - longer blocks more efficient
- 64B65B
  - 2.5/5/10GBASE-T
  - XGMII
- 80B81B - 1000BASE-T1
  - GMII

Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Transmit Data Scramblers

- Linear Feedback Shift Register
- DC balance
- Equal distribution of levels for multilevel PAM
- Reduce emissions, eliminate repetitive patterns
- Self-synchronizing scramblers cause error propagation at the receiver
- Good: $1 + x^{39} + x^{58}$ self sync for 2.5/5/10GBASE-T, 10GBASE-R
  - $1 + x^{13} + x^{33}$ side stream for 1000BASE-T
  - $1 + x^{4} + x^{15}$ side stream for 1000BASE-T1
- Bad: 100BASE-TX 11-bit LFSR -> killer packet issue

4B3B for PAM3

- 100BASE-T1 Line Code
  - Maps MII nibble to 3 bit symbols for ternary line modulation
    - TXD<3:0>, TX_EN, TX_ER at 25MHz
    - PAM3 at 66.666 Mbaud
  - SSD: Start of Stream Delimiter
    - 6 symbols replaces the first 9 bits of preamble
  - Stuff bits added for packets not a multiple of 3
  - ESD: End of Stream Delimiter
    - 6 symbols generated at end of packet
  - ERR_ESD: Error End of Stream Delimiter
    - Sent when transmit error is encountered
  - Errors propagate across 2 symbols / 3 bits
  - No FEC / error detection
- Side Stream Scrambler from 1000BASE-T
  - 33 bit LFSR synchronized during training
  - No error propagation

THANK YOU