147. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1S

147.1 Overview

This clause defines the type 10BASE-T1S Physical Coding Sublayer (PCS) and type 10BASE-T1S Physical Medium Attachment (PMA) sublayer. Together, the PCS, and PMA sublayers comprise a 10BASE-T1S Physical Layer (PHY). Provided in this clause are fully functional and electrical specifications for the type 10BASE-T1S PCS and PMA.

The 10BASE-T1S PHY is a full/half-duplex point-to-point and half-duplex multidrop PHY specification, capable of operating at 10 Mb/s. The 10BASET1S PHY is intended to be operated over a single twisted-pair copper cable, defined in 147.7. The cabling supporting the operation of the 10BASE-T1S PHY is defined in terms of performance requirements between the attachment points (Medium Dependent Interface (MDI)), allowing implementers to provide their own cabling to operate the 10BASE-T1S PHY as long as the normative requirements included in this Clause are met.

This clause also specifies an optional Energy-Efficient Ethernet (EEE) capability. A 10BASE-T1S that supports this capability may enter a Low Power Idle (LPI) mode of operation during periods of low link utilization as described in Clause 78.

An optional support for PHY Level Collision Avoidance (PLCA) functions, described in Clause 148, is also specified in this clause. PLCA provides improved performance in terms of effective throughput and maximum transmission latency when operating in half-duplex mode over a multi-drop mixing segment network.

147.1.1 Relationship of 10BASE-T1S to other standards

The relationship between the 10BASE-T1L PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model are shown in Figure 147–1. The PHY sublayers (shown shaded) in Figure 147–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 10BASE-T1S is defined in Clause 98. MII is defined in Clause 22

147.1.2 Operation of 10BASE-T1S

The 10BASE-T1S PHY can operate using full-duplex or half-duplex point-to-point communications over a single twisted-pair copper cable with an effective rate of 10 Mb/s in each direction simultaneously.

Additionally, the 10BASE-T1S PHY can operate using half-duplex multidrop communications over a single twisted-pair copper cable interconnecting up to at least eight in-line PHYs with up to 10cm stubs, achieving an overall effective rate of 10 Mb/s, shared among the nodes.

In any operating mode the 10BASE-T1S PHY supports operation on a link segment or mixing segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 15 meters to support low cost applications requiring short physical reach, such as industrial, automotive and automation controls.

The 10BASE-T1S PHY utilizes two level Differential Manchester Encoding (DME) modulation transmitted at a 12.5 MBd rate. 4B5B encoding is used to further improve EMC performance and to perform out-of-band signaling among the connected PHYs. DME is a self-clocked and intrinsically balanced line coding which guarantees very low DC baseline wander and allows for robust clock and data recovery in noisy environments. The 4B5B mapping is contained in the PCS (see 147.3) while the DME encoder/decoder is contained in the PMA (see 147.2).

TODO: Figure 147-1 → same as 146-1

Auto-Negotiation (***Clause 98***) may optionally be used by 10BASE-T1S devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment or mixing segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup ***through the use of half-duplex differential Manchester encoding.*** The implementation of the Auto-Negotiation function is optional. ***If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98***.

The 10BASE-T1S PMA couples messages from the PCS to the MDI and provides clock and data recovery. The PMA provides full duplex or half-duplex communications at 12.5 MBd over the single twisted-pair copper cable. PMA functionality is described in 147.4. The MDI is specified in 147.8.

147.3 Physical Coding Sublayer (PCS) functions

147.3.1 PCS Reset Function

The Physical Coding Sublayer (PCS) consists of PCS Reset, PCS Transmit, and PCS Receive functions as shown in Figure 147–2. The PCS Reset function is explained in 147.3.1, the PCS Transmit function is explained in 147.3.2, the PCS Receive function is explained in 147.3.3, and the PCS Loopback function is explained in 146.3.4.

PCS reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PCS Reset shall set pcs_reset = ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

TODO: figure 147-2 – PCS reference diagram

147.3.2 PCS Transmit

147.3.2.1 PCS Transmit Overview

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 147–4, and the associated state variables, functions, timers and messages.

In each symbol period, PCS Transmit generates a symbol tx_sym conveyed to the PMA, where tx_sym is a five-bit vector. The PMA encode tx_sym, LSB first, into a DME stream over the wire pair BI_DA at a nominal symbol clock frequency specified in 147.5.4.5.

Upon the assertion of TX_EN, the PCS Transmit function passes three SYNC symbols to the PMA, followed by one SSD symbol, which replaces the first 16 bits of the preamble. Following SSD, TXD[3:0] is encoded into 5B symbols using encoding rules specified in 147.3.3.x.x, until TX_EN is de-asserted.

Following the de-assertion of TX_EN, the PCS Transmit generates a special code ESD, followed by either ESDOK or ESDERR when a transmit error is encountered.

The 10BASE-T1S has one special 5B symbol ‘I’ (1,1,1,1,1) which represents SILENCE. When the PHY is operating in half-duplex multidrop mode, the PMA Transmit functions shall put the PMD into a high impedance state on reception of this symbol from the PCS Transmit. When operating in point-to-point mode, the PMA shall drive a zero voltage level on the line on receipt of the ‘I’ symbol.

147.3.3.1.1 Variables

pcs_reset The pcs_reset parameter set by the PCS Reset function.

	Value: ON or OFF
pcs_txen	The TX_EN signal of the MII as specified in ... When optional PLCA functions are enabled, this signal is generated as specified in ... When set to FALSE transmission is disabled. When set to TRUE transmission is enabled. Value TRUE or FALSE
pcs_txer	The TX_ER signal of the MII as specified in ... When optional PLCA functions are enabled, this signal is generated as specified in ... When set to FALSE it indicates a non-errored transmission. When set to TRUE it indicates an errored transmission Value: TRUE or FALSE
pcs_txd	The TXD signal of the MII as specified in ... When optional PLCA is enabled, this signal is generated as specified in ... This signal represents a 4B data nibble to be transmitted.
tx_cmd	5B symbol to be transmitted when the PCS Transmit function is in SILENT state. The tx_cmd variable is set by the optional PLCA reconciliation sublayer to signal a BEACON condition or to commit a time slot as described in 148.x.x.x. When PLCA functions are not implemented, tx_cmd shall be set to the special 5B symbol 'I' (1,1,1,1,1) representing SILENCE.
tx_sym	5B symbol to transmit, generated from the MII data or directly passed from tx_cmd in SILENT state when optional PLCA reconciliation sublayer is implemented.
transmitting	the transmitting variable is set in the PCS data transmission as defined in figure… When this variable is set to TRUE it indicates a transmission is ongoing. Value: TRUE or FALSE
err	the err variable is set in the PCS data transmission as defined in figure… This variable is used to detect and latch a pcs_txer = TRUE condition during data transmission; if such error is detected, a ESDERR symbol is sent at the end of transmission. Value: TRUE or FALSE
link_control	This variable is generated by management or set by default. When set to FALSE all PCS functions are switched off and no data can be sent or received. Values: TRUE or FALSE.
SYNC	5B symbol defined as 'J' in 4B5B encoding (see also table ...)
SSD	5B symbol defined as 'K' in 4B5B encoding (see also table ...)
ESD	5B symbol defined as 'T' in 4B5B encoding (see also table ...)
ESDERR	5B symbol defined as 'H' in 4B5B encoding (see also table ...)
ESDOK	5B symbol defined as 'R' in 4B5B encoding (see also table ...)

147.3.3.1.2 Functions

ENCODE In the PCS transmit process, this function takes as its arguments the pcs_txd input data and returns the corresponding 5B symbol as defined in table ...

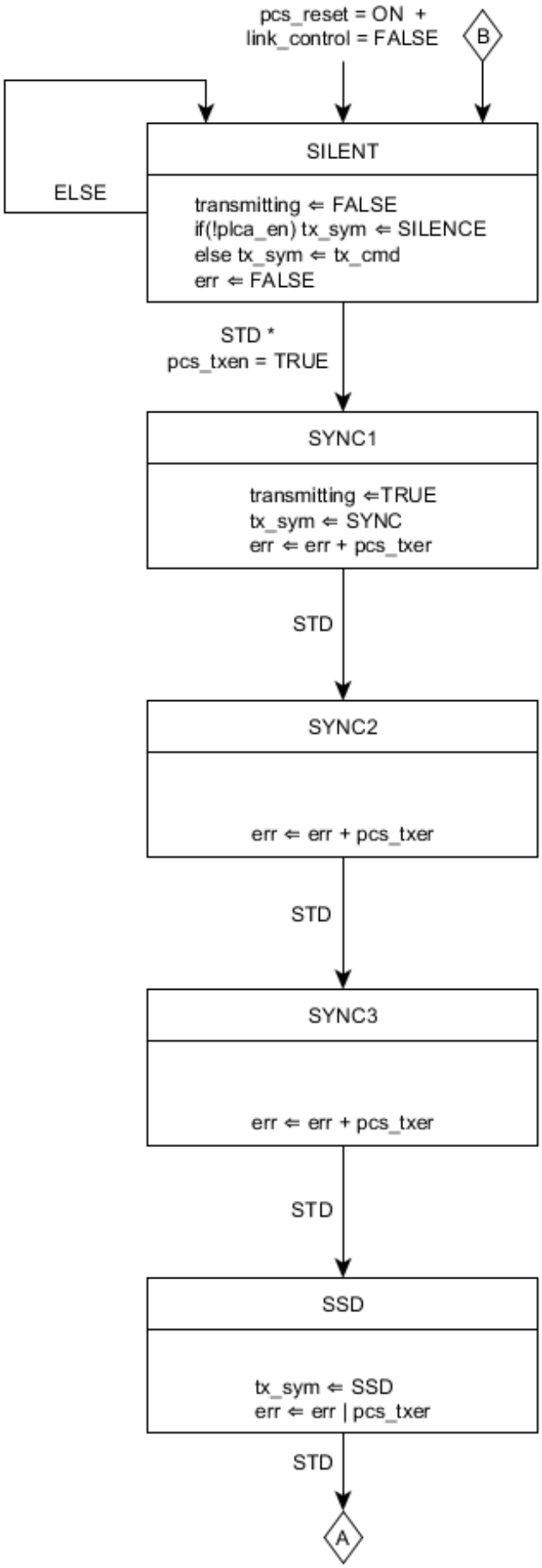
Name	4B	5B	Name	4B	5B	Special Function
0	0000	11110	I	-	11111	SILENCE
1	0001	01001	J	-	11000	SYNC
2	0010	10100	K	-	10001	SSD
3	0011	10101	T	-	01101	ESD
4	0100	01010	R	-	00111	ESDOK
5	0101	01011	H	-	00100	ESD
6	0110	01110	N	-	01000	BEACON
7	0111	01111				
8	1000	10010				
9	1001	10011				
A	1010	10110				
B	1011	10111				
C	1100	11010				
D	1101	11011				
E	1110	11100				
F	1111	11101				

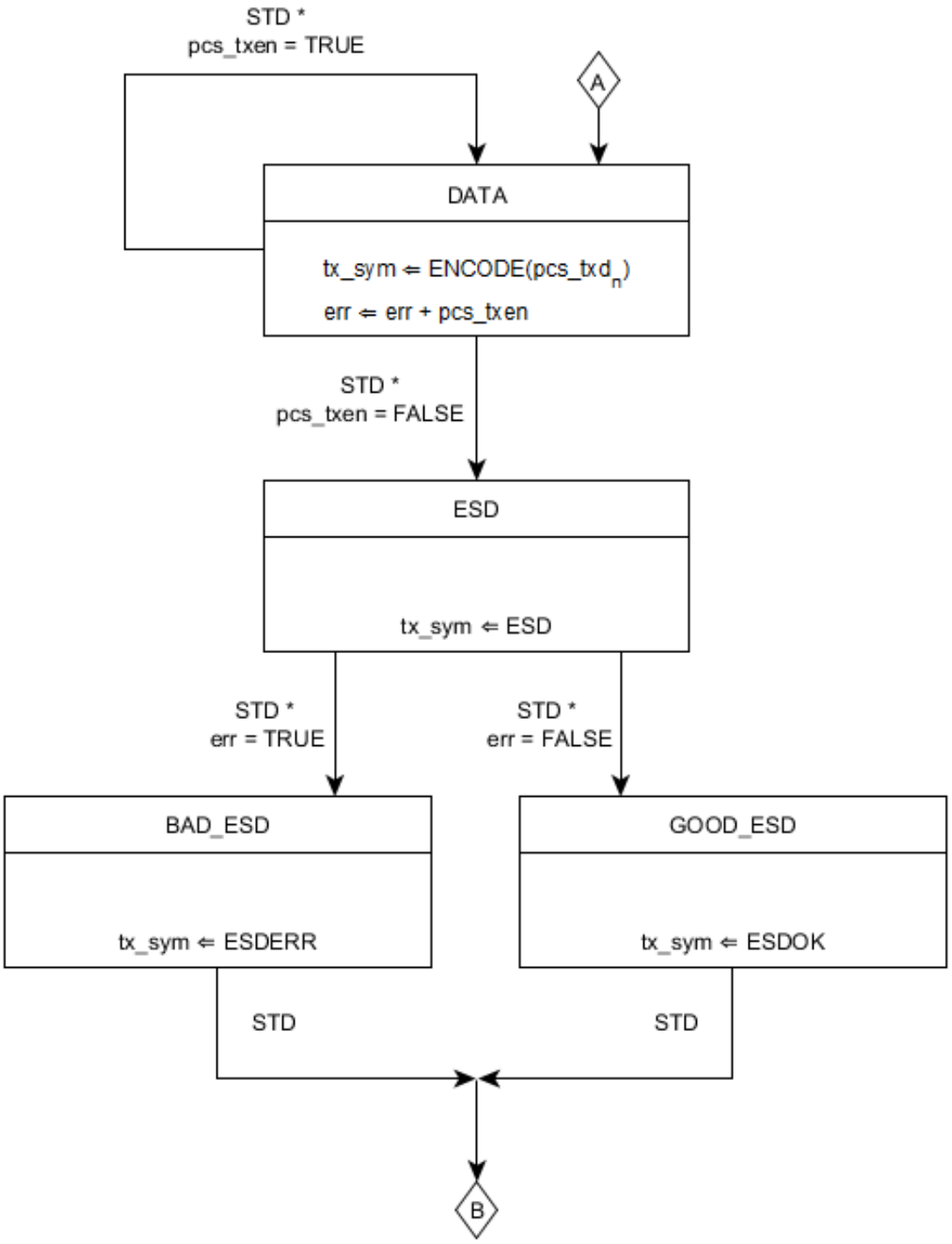
147.3.3.1.3 Timers

No timers are defined for the PCS Transmit functions.

147.3.3.1.4 Abbreviations

STD alias for 5B symbol timer done, synchronous to PCS TX clock


pcs_reset = ON +
link_control = FALSE
B
SILENT
ELSE
transmitting ⇐ FALSE
if(!plca_en) tx_sym ⇐ SILENCE
else tx_sym ⇐ tx_cmd
err ⇐ FALSE
STD *
pcs_txen = TRUE
SYNC1
transmitting ⇐TRUE
tx_sym ⇐ SYNC
err ⇐ err + pcs_txer
STD
SYNC2
err ⇐ err + pcs_txer
STD
SYNC3
err ⇐ err + pcs_txer
STD
SSD
tx_sym ⇐ SSD
err ⇐ err | pcs_txer
STD
A


STD *
pcs_txen = TRUE
A
DATA
tx_sym ⇐ ENCODE(pcs_txd$_n$)
err ⇐ err + pcs_txen
STD *
pcs_txen = FALSE
ESD
tx_sym ⇐ ESD
STD *
err = TRUE
STD *
err = FALSE
BAD_ESD
tx_sym ⇐ ESDERR
GOOD_ESD
tx_sym ⇐ ESDOK
STD
STD
B

147.3.4.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 147–7, and associated state variables.

NOTE: A JAB state machine as the one defined for the 10BASE-T1L PHY in clause 147 is not required for the 10BASE-T1S PHY because even in case of misdetection of the ESD special symbol, the actual end of a transmission can still be detected by the PMA exploiting the absence of DME activity on the line. In fact, during idle period (i.e. when no data is being transmitted), the PMD is either driving a constant zero voltage level or put into high impedance state, depending on the operating mode (see ...).

The finite state machine defined in figure ... is triggered by the reception of a SYNC symbol 'J' from the PMA Receive function and waits for the SSD symbol 'K' to start regenerating the packet preamble whose start has been replaced with the SYNC, SYNC, SYNC, SDD sequence by the PCS Transmit functions as described in figure ... Following the SSD marker there are four states before the DATA state to accomplish this task.

The DATA state, in which 5B symbols are decoded into MII data, is left when ESD followed by either ESDOK or ESDERR symbol is encountered or when the PMA detects SILENCE on the media (e.g. the transmitter prematurely stops data transmission).

The variables, functions, and timers used in Figure ..., are defined as below. For the definition of pcs_reset, SYNC, SSD, ESD, ESDOK and ESDERR see 147.3.3.1 and following.

147.3.4.1.1 Variables

receiving	the receiving variable is set in the PCS data receive as defined in figure… When it is set to TRUE it indicates a receive is ongoing. Value: TRUE or FALSE
pcs_rxdv	The RX_DV signal of the MII as specified in 22.2.2.7.
pcs_rxer	The RX_ER signal of the MII as specified in 22.2.2.10.
pcs_rxd	PCS decoded data synchronous to RX_CLK.
RXn	Received 5b symbol generated by PMA receive at time n
SILENCE	A 5B symbol defined as 'I' in 4B5B encoding

147.3.4.1.2 Functions

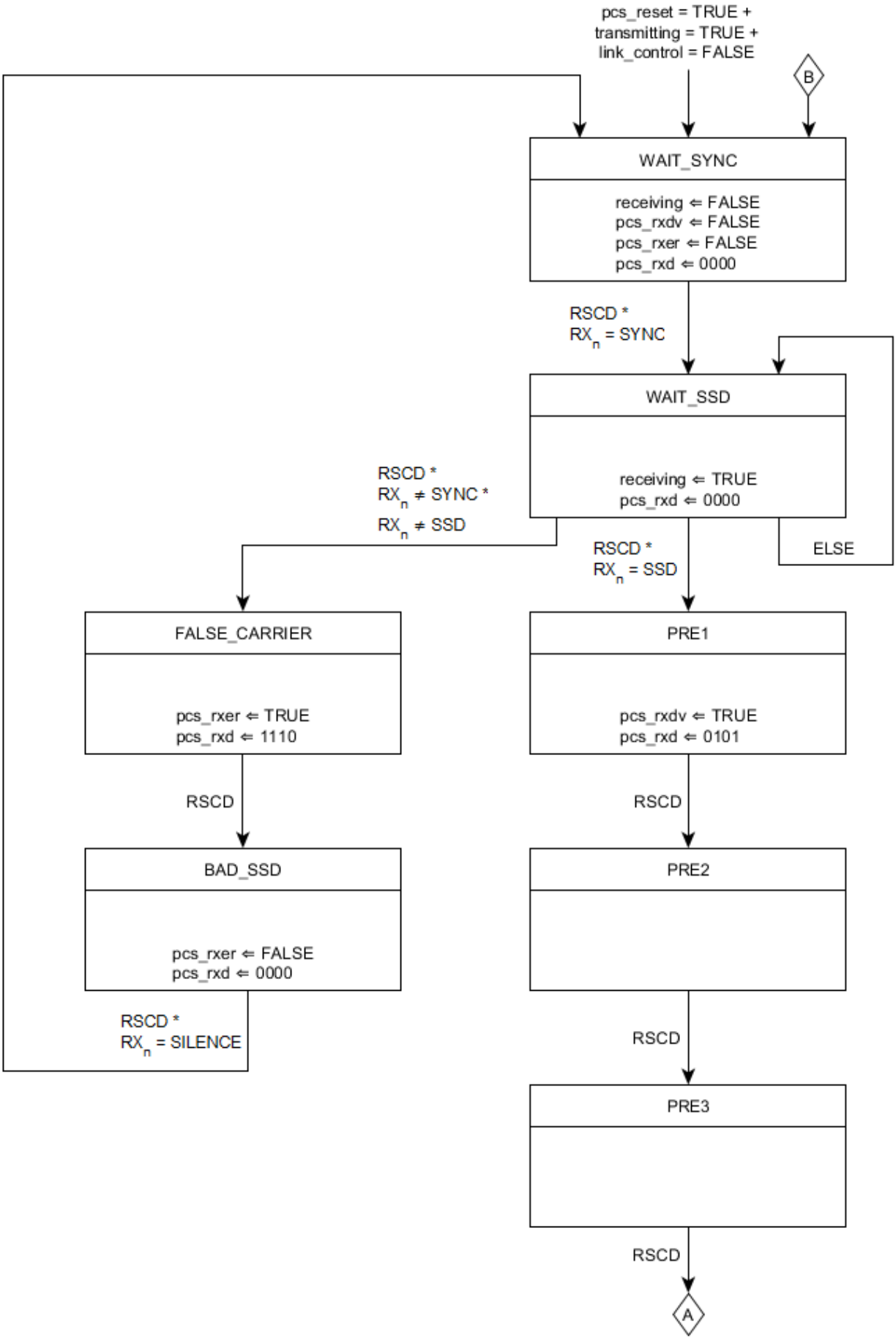
DECODE	in the PCS Receive process, this function takes as its arguments the sym_rx input data from PMA and returns the corresponding 4B MII data as defined in table ...

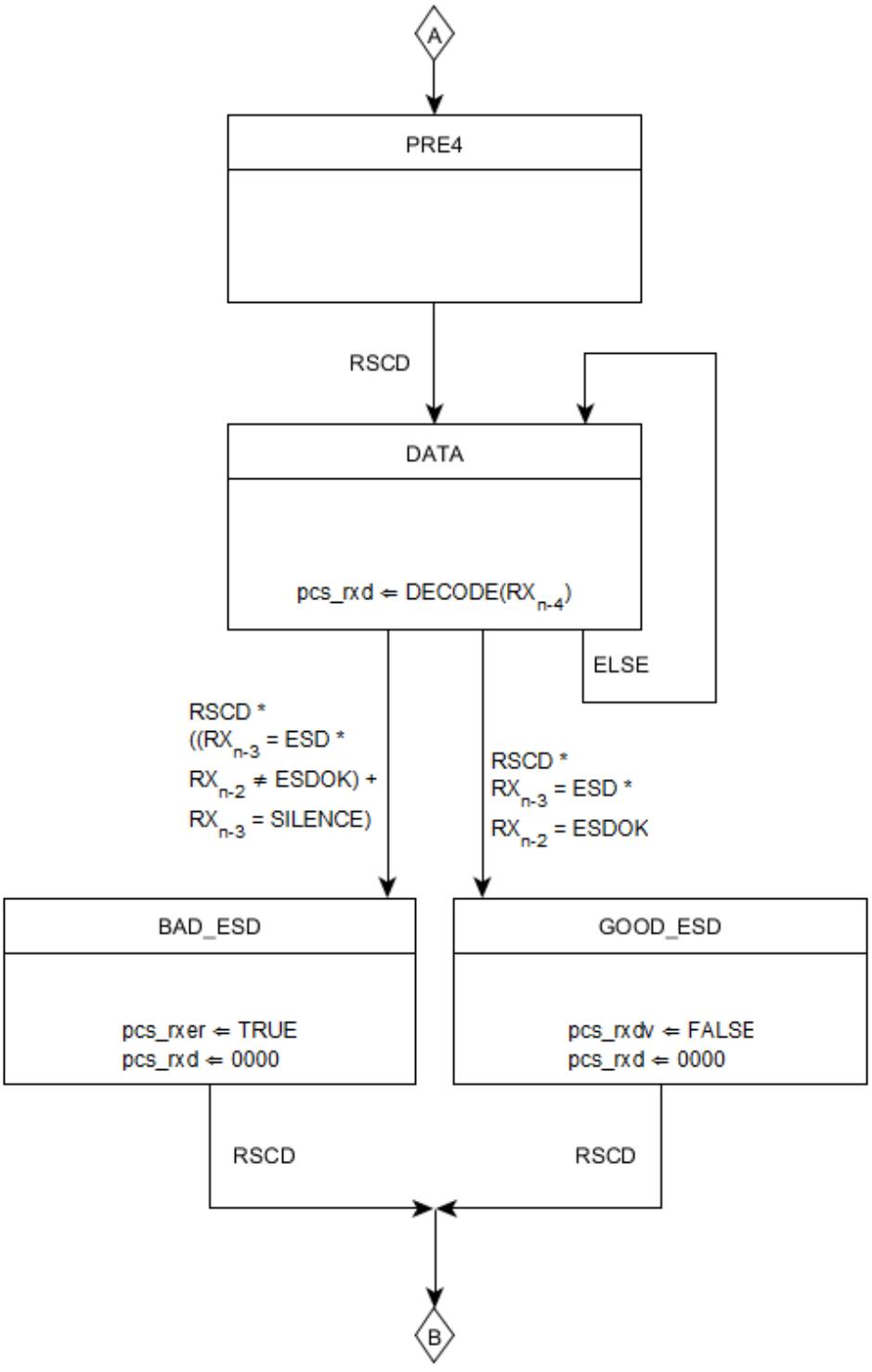
147.3.4.1.3 Timers

No timers are defined for the PCS Receive functions.

147.3.4.1.4 Abbreviations

RSCD	alias for Receive Symbol Conversion Done, synchronous to PCS RX clock


pcs_reset = TRUE +
transmitting = TRUE +
link_control = FALSE
B
WAIT_SYNC
receiving ⇐ FALSE
pcs_rxdv ⇐ FALSE
pcs_rxer ⇐ FALSE
pcs_rxd ⇐ 0000
RSCD *
RX_n = SYNC
WAIT_SSD
receiving ⇐ TRUE
pcs_rxd ⇐ 0000
RSCD *
RX_n ≠ SYNC *
RX_n ≠ SSD
RSCD *
RX_n = SSD
ELSE
FALSE_CARRIER
pcs_rxer ⇐ TRUE
pcs_rxd ⇐ 1110
PRE1
pcs_rxdv ⇐ TRUE
pcs_rxd ⇐ 0101
RSCD
RSCD
BAD_SSD
pcs_rxer ⇐ FALSE
pcs_rxd ⇐ 0000
PRE2
RSCD *
RX_n = SILENCE
RSCD
PRE3
RSCD
A


A
PRE4
RSCD
DATA
pcs_rxd ⇐ DECODE(RX n-4)
ELSE
RSCD *
((RX n-3 = ESD *
RX n-2 ≠ ESDOK) +
RX n-3 = SILENCE)
RSCD *
RX n-3 = ESD *
RX n-2 = ESDOK
BAD_ESD
pcs_rxer ⇐ TRUE
pcs_rxd ⇐ 0000
GOOD_ESD
pcs_rxdv ⇐ FALSE
pcs_rxd ⇐ 0000
RSCD
RSCD
B

147.3.5 PCS Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to a one (or PCS loopback mode is enabled by a similar functionality if MDIO is not implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium. The PCS loopback data flow is illustrated in Figure 146–11.

// TODO: copy Figure 146-11 ?

147.3.6 Collision detection

When operating in half-duplex mode, the 10BASE-T1S PHY shall detect physical collisions on the media during data transmission. When collisions are detected, the PHY shall assert the signal COL on the MII for the duration of the collision or until TX_EN signal is FALSE.

A collision may be detected by monitoring the rx_sym parameter conveyed through the PMA_UNITDATA.indication primitive for a SYNC, SSD symbol sequence (that is a 'JK' 5B sequence) and verify matching against the transmitted symbol sequence after the SSD. A collision results in a mismatch in the symbol sequence.

147.3.6 Carrier Sense

When operating in half-duplex mode, the 10BASE-T1S PHY shall sense when the media is busy and convey this information to the MAC asserting the signal CRS on the MII as specified in clause 22.x.

CRS is generated by PCS Receive as the logical OR of the "transmitting" and "receiving" variables.

147.4 Physical Medium Attachment (PMA) Sublayer

The PMA couples messages from the PMA service interface specified in 147.2.1 onto the 10BASE-T1S physical medium. The PMA provides both full duplex and half duplex communications to and from medium employing 2-level Differential Manchester Encoding modulation. The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 147.8.

// TODO: PMA figure

147.4.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:
a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

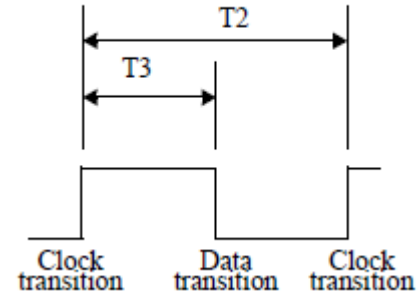
147.4.2 PMA Transmit function

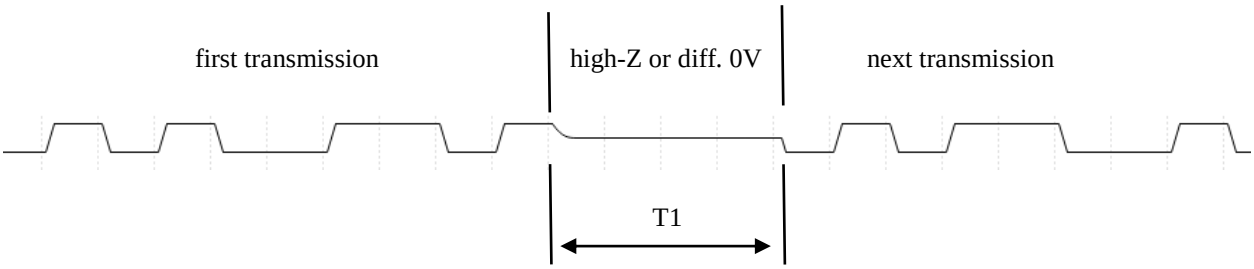
Figure xxx illustrates the signal flow of the 10BASE-T1S PMA Transmit function. During transmission, PMA_UNITDATA.request conveys to the PMA using rx_sym the value of the symbols to be sent over the single transmit pair.

// TODO: PMA transmit figure

DME uses the presence or absence of transitions between these two voltage levels to encode data, thus the polarity is irrelevant.

The tx_sym variable is a vector of 5 bits to be encoded, LSB first, using Differential Manchester Encoding (DME) rules defined below:





	Parameters	Min	Typ	Max	Units
T1	Delay between transmissions	200			ns
T2	Clock transition to clock transition		80		ns
T3	Clock transition to data transition (data = 1)		40		ns

If the tx_sym parameter value is the special 5B symbol ‘I’ (1, 1, 1, 1, 1) and the PHY is operating in multidrop mode, the PMD shall be put into high impedance state. When the PHY is operating in point-to-point mode a differential voltage of 0V (BI_DA+ = BI_DA-) shall be driven instead.

If tx_sym value is anything other than ‘I’ the following rules apply.

- A “clock transition” shall always be generated at the start of each bit.
- A “data transition” in the middle of a nominal bit period shall be generated if the bit to be transmitted is a logical ‘1’. Otherwise no transition shall be generated until next bit.

The timings for clock and data transitions are specified in table XXX.
Tolerance for the T2 and T3 parameter is +/- 100ppm to meet the MII TX_CLK specification in clause xxx.

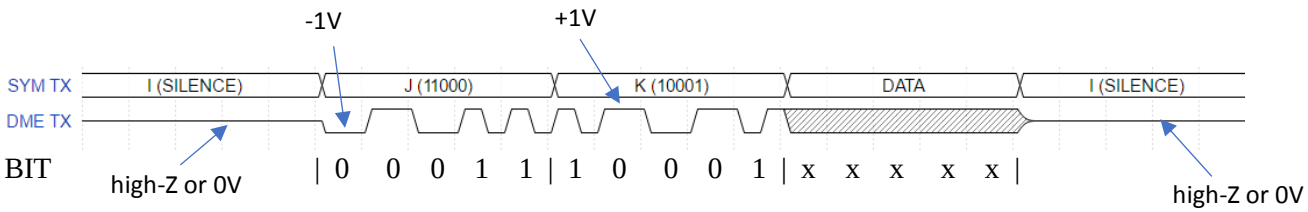


Figure 1: example DME encoding of 5B symbols

147.4.3 PMA Receive function

Figure xxx illustrates the signal flow of the 10BASE-T1S PMA Receive function. The 10BASE-T1S PMA Receive function comprises a single receiver (PMA Receive) for DME modulated signals on a single balanced pair, BI_DA. PMA Receive has the ability to translate the received signals on the single pair into the PMA_UNITDATA.indication parameter rx_sym. It detects 5B symbol groups from the signals received at the MDI and presents these sequences to the PCS Receive function.

The PMA receive function shall recover encoded clock and data information from the DME encoded stream received at the MDI. In order to accomplish this task, the PMA Receive shall achieve proper synchronization on both the DME stream and the 5B boundary.
At the start of each transmission, the symbol sequence J, J, J, K which replaces the first 16 bit of packet preamble is meant to allow the receiver to achieve such synchronization.

If the optional PLCA Functions are implemented, the PMA_CARRIER.indication primitive shall be supported as well. This one must indicate whether the PMA Receive has achieved synchronization at least on the incoming DME encoded stream.

147.4.6 PMA clock recovery

This PMA function recovers the clock from the received stream. PMA clock recovery outputs are used as input variables for other PMA functions.

147.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 10BASE-T1S Ethernet PHY.

// TODO: copy or reference clauses 146.5.1.1, 146.5.1.2. They apply as well for the T1S.

147.5.2 PMA electrical specifications

The test modes described in this sub clause shall be provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop. The test modes can be enabled by setting bits 1.xxxx.xx:xx (10BASE-T1S PMA/PMD Test Control Register) of the PHY Management register set as described in 45.2.1.xxx. If MDIO is not implemented a similar functionality shall be provided by another interface. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

c) Test mode 1 - Transmitter output voltage, timing jitter
d) Test mode 2 - Transmitter output droop test mode
e) Test mode 3 – Transmitter distortion test and PSD mask

When test mode 1 is enabled, the PHY shall repeatedly transmit the data symbol sequence (+1, -1). See 147.4.2 for transmit clock requirements.

When test mode 2 is enabled, the PHY shall transmit ten "+1" symbols followed by ten "-1" symbols. This sequence is repeated continually.

When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of “+1” and “-1” symbols. TBD: how to generate the sequence.

// TODO: copy or reference clauses 146.5.3, 146.5.4. They apply as well for the T1S.

147.5.4.1 Transmitter output voltage

Transmitter output voltage shall be tested using test mode 1 in combination with the test fixture shown in Figure 146–17. The transmitter output voltage shall be 1.0 V ± 30 % peak-to-peak. Transmitter output voltage can be set using the management interface or by hardware default set-up. Additionally, auto-negotiation can be used to find a common transmitter output voltage for the two PHYs.

Fixed transmitter driving levels can be selected by setting bits 1.xxxx.xx:xx (10BASE-T1L PMA/PMD Control Register) of the PHY Management register set as described in 45.2.1.xxx. If MDIO is not implemented a similar functionality shall be provided by another interface. Default setting is to use auto-negotiation.

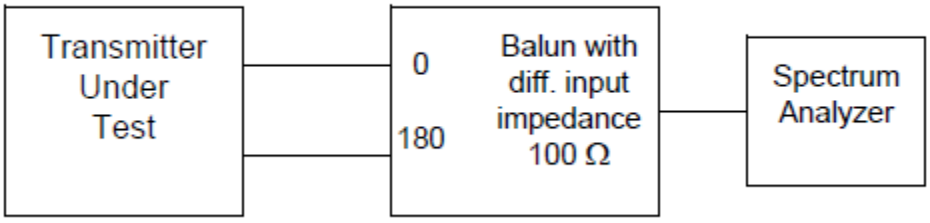
// TODO: copy or reference clause 146.5.4.2. It applies as well for the T1S.

147.5.4.3 Transmitter timing jitter

The transmitter symbol-to-symbol jitter shall be tested using test mode 1 in combination with the test fixture shown in Figure 146–17. The maximum jitter at the transmitter side shall be less than ± 7.5 ns symbol-to symbol jitter.

147.5.4.4 Transmitter power spectral density (PSD)

The transmitter Power Spectral Density (PSD) shall be measured using test mode 3 in combination with the test fixture shown in Figure xxx.



The measured PSD shall be between the upper and lower bounds specified in the table below. The upper and lower limits are given in Equation XXX and Equation XXX, and shown in Figure XXX.

$$Upper\ PSD(f) = \begin{cases} -59.3 - 1.5 * \dfrac{f\ -1}{19} & 300KHz < f < 20\ MHz \\ -60.8 - 3.7 * \dfrac{f\ -20}{20} & 20\ MHz < f < 40\ MHz \\ -64.5 - 8.0 * \dfrac{f-40}{17} & f > 40\ MHz \end{cases}$$

$$Lower\ PSD(f) = \begin{cases} -70.9 - 4.9 * \dfrac{f\ -1}{19} & 300KHz < f < 20\ MHz \\ -75.8 - 13.4 * \dfrac{f-20}{20} & f > 20\ MHz \end{cases}$$

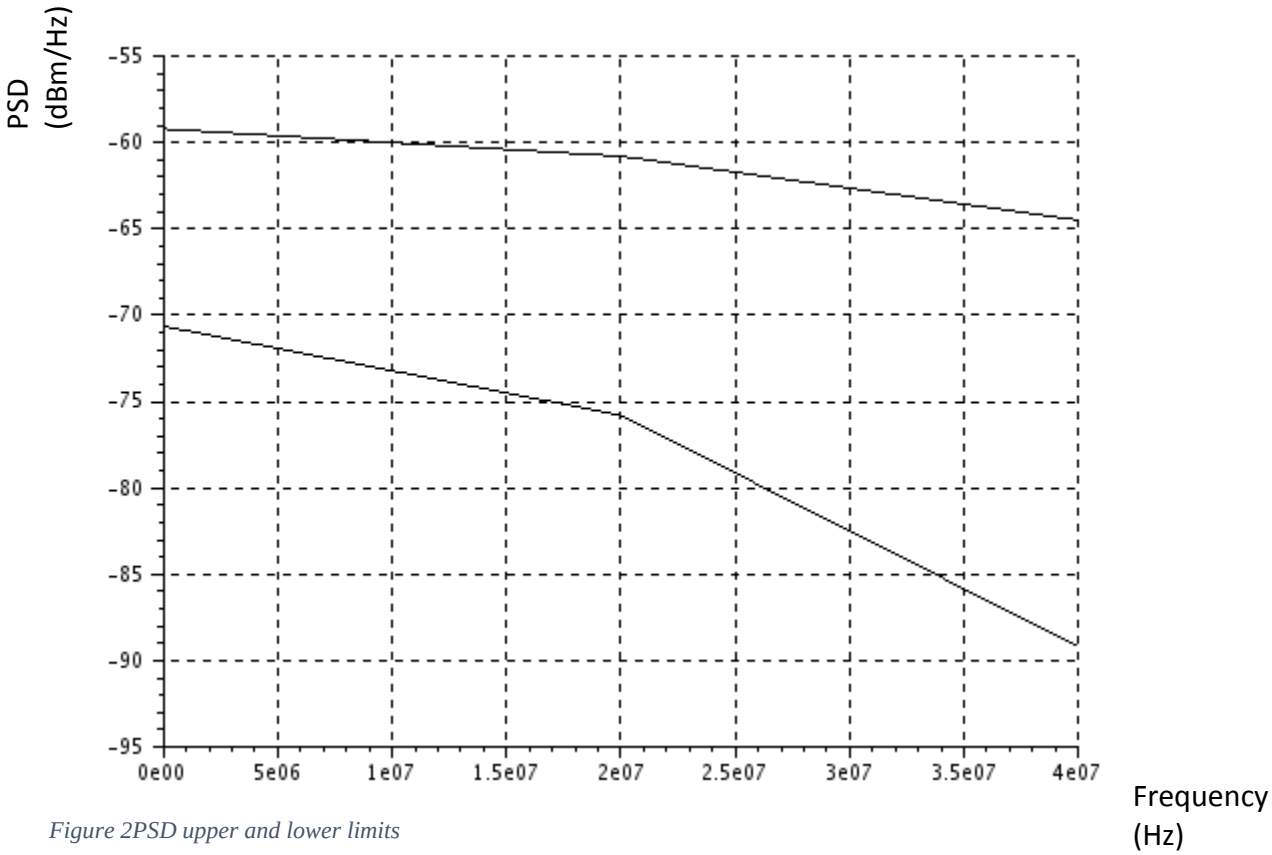


Figure 2PSD upper and lower limits

147.5.4.5 Transmit clock frequency

The symbol transmission rate shall be within the range 12.5 MBd ±100 ppm.

// TODO: copy or reference clause 146.5.x.x Alien Crosstalk Noise Injection. It applies as well for the T1S.
// TODO: this shall be discussed with the group

// TODO: copy or reference clause 146.5.7 PMA local loopback. It applies as well for the T1S.
// TODO: this shall be discussed with the group

// TODO: copy or reference clause 146.5.5 Receiver electrical specifications. It applies as well for the T1S.

147.6 PMD specification

147.6.2 PMD electrical specifications

This clause defines the minimum requirements of the PMD for both point-to-point and multidrop PHY operating modes.

The PMD shall be able to drive a line consisting of the MDI and a twisted pair copper cable with nominal characteristic impedance of 100 Ohms.

In order to support point-to-point operating mode, the PMD shall provide fixed 100 Ohm termination +/- 10% and shall be able to drive positive, negative and zero differential voltage levels as specified in … corresponding respectively to DME positive, negative and silence line states.

In order to support multidrop operating mode, the PMD shall provide fixed 50 Ohm termination +/- 10% and shall be able to drive positive or negative voltage levels and go to high impedance state as specified in … corresponding respectively to DME positive, negative and silence line states.

In Multidrop configuration the MDI shall be terminated by two 100 Ohm nominal resistances at the edges as in figure 3. When not driving the MDI, the PMD shall insert a fixed termination of 10 KOhms.

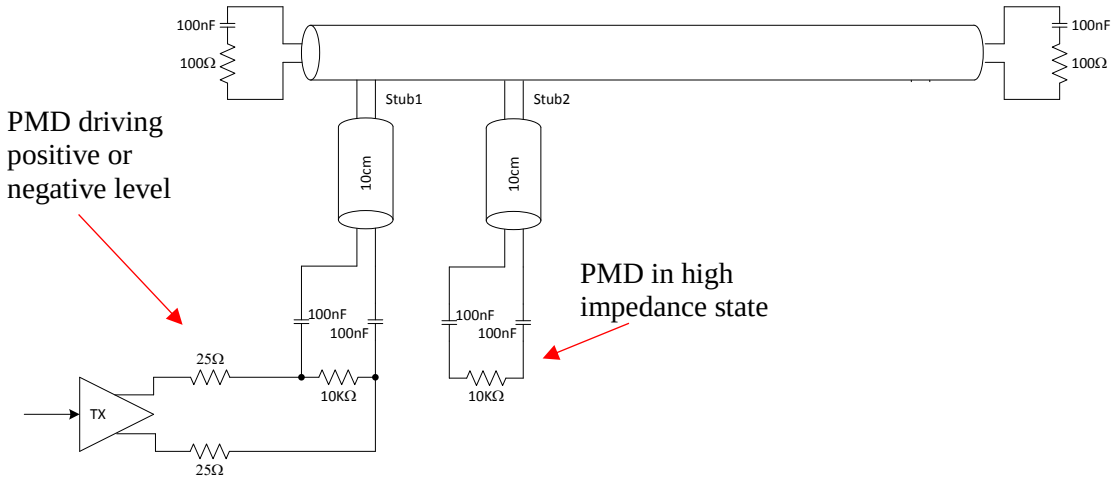


Figure 3: multidrop line termination and PMD

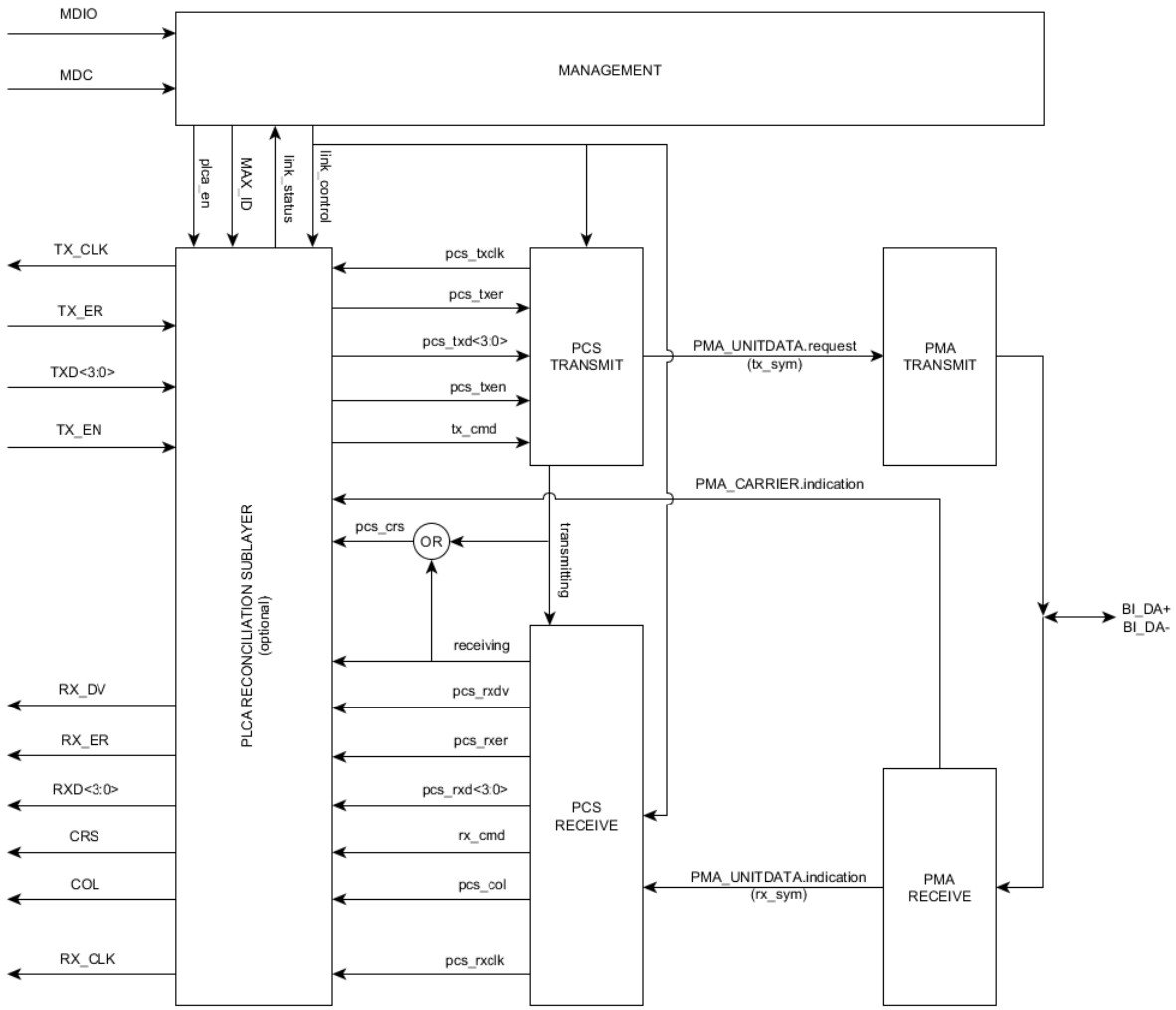
148. PLCA Reconciliation Sublayer

148.1 Overview

This clause defines an optional reconciliation sublayer for half-duplex, multidrop PHYs compliant with MII clause 22, such as the 10BASE-T1S, meant to improve performance (throughput, latency) over standard CSMA/CD method for small networks featuring a limited number of nodes and low propagation delays.

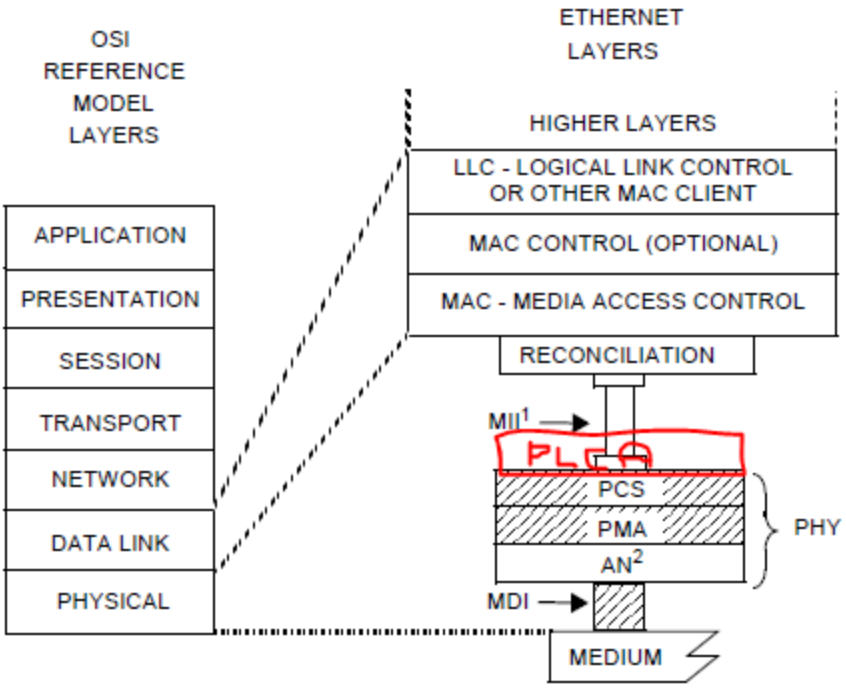
Exceeding CSMA/CD performance enables the use of ethernet based systems in specific environments such as automotive, industrial and automation controls, which often have strict requirements in terms of determinism and reliability on the transport network. PLCA, which stands for “PHY Level Collision Avoidance”, represents a competitive alternative to commonly used TDMA based protocols which typically yields a very high (and sometime unnecessary) degree of determinism while paying severe penalties in terms of efficient bandwidth allocation, flexibility and ease of use (network is typically required to be fully engineered).

PLCA is designed to work on top of standard CSMA/CD and can be dynamically enabled/disabled via management interface. When disabled, the system seamlessly reverts to normal CSMA/CD behavior.



148.1.1 Relationship of PLCA reconciliation sublayer to other standards

The relationship between the PLCA reconciliation sublayer, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model are shown in Figure xxx.



148.1.2 Operation of PLCA reconciliation sublayer

The working principle of PHY Level Collision Avoidance (PLCA) is that each PHY is assigned an ID that is unique across the multidrop mixing segment network, and may only transmit data during a specific time slot corresponding to its own ID number.

The main difference from a TDMA based system is that time slots are very short (typically 20 bit times) and may grow up dynamically to accommodate the actual size of the packet being transmitted. If a PHY doesn't have any data ready to transmit, it shall yield the time slot by remaining silent for the minimum time slot duration, giving another PHY the opportunity to transmit in turn.

One single PHY, the one with ID = 0, is given the role of master. The master PHY, which is the only one that needs to know the maximum allowed number of active PHYs on the network, is responsible for periodically signaling a "BEACON" condition which allows the slave PHYs to re-synchronize on a common time base to properly detect the start and the end of a time slot with minimum relative skew. After reception of a BEACON, the time slot counter is reset and a new "bus cycle" begins.

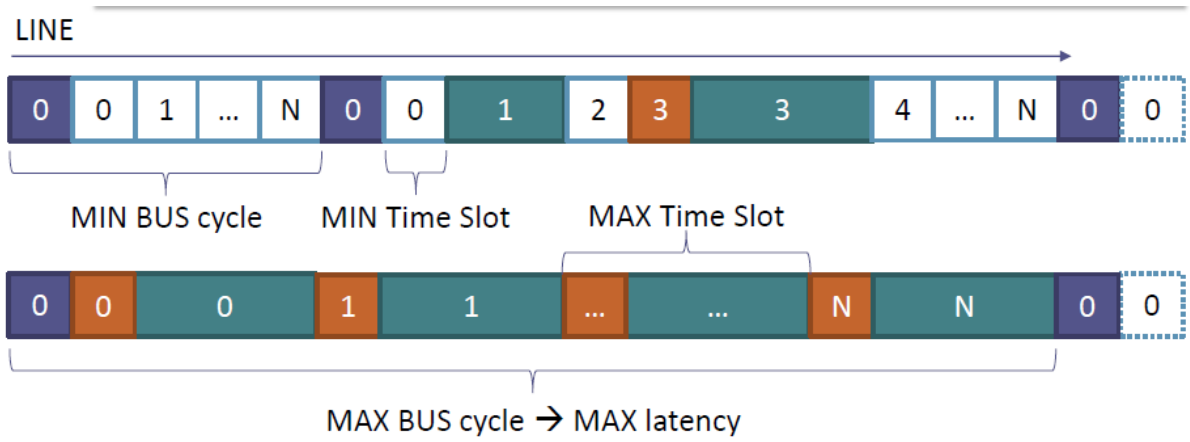


Figure 4: dynamic time slots (number inside boxes are PHY IDs)

This approach provides three main benefits:

1. physical collisions on the line are avoided, thus reducing the maximum transmit latency down to (N * MAX_PACKET_SIZE + BEACON_TIMER) bits, where N is the configured maximum number of PHYs and BEACON_TIMER is the duration of the BEACON signal, i.e. 20 bit times. This is the same number achievable using a fixed time slot TDMA approach with the exception that average latency is typically much shorter in PLCA approach because of non-transmitting PHYs yielding their time slots when they have no data to transmit. This maximum latency is usually hundreds of times larger using plain CSMA/CD due to collisions and random MAC back-offs.
2. Dynamic time slots allow for efficient allocation of available bandwidth, thus maximizing the throughput, especially when the network is loaded. When all PHYs have data to transmit, no time is actually wasted (best case). When only one PHY has data to transmit, the worst case wasted time is (N * TS_TIMER) where N is the configured maximum number of PHYs and TS_TIMER is the configured minimum time slot duration. See ... (efficiency calculation)
3. Since at each bus cycle all the PHYs always have one chance to transmit, the mechanism is intrinsically fair, avoiding starvation due to PHYs that keep gaining access to the media. This is something that might actually happen using plain CSMA/CD where after a collision the first PHY gaining access to the media have higher chances than others to re-gain such access because of reduced max backoff time.

One possible side effect of PLCA is that the actual latency of a single transmission is constrained but not predictable, resulting in a small amount of added packet-level jitter.

For TSN applications this jitter can be avoided by adding TSSI functions in between PLCA reconciliation sublayer and the PCS: in such a way timestamps are inserted right after the PLCA variable delay line, where remaining latency (PCS to MDI) is constant.

One important thing about PLCA is that for this mechanism to work, a PHY needs to know whether its connected MAC has data ready to be transmitted or not. Since no dedicated MII signal exists for this purpose, PLCA relies on CRS and COL MII interface to detect this condition.

When the MAC asserts the TX_EN signal, PLCA keeps the transmitted MII data in a variable delay line until one of the following condition occurs:

a) PHY is allowed to transmit because its dedicated time slot is met. In this case the delayed the data is conveyed to the PCS to eventually reach the media. When other PHYs are silent during their

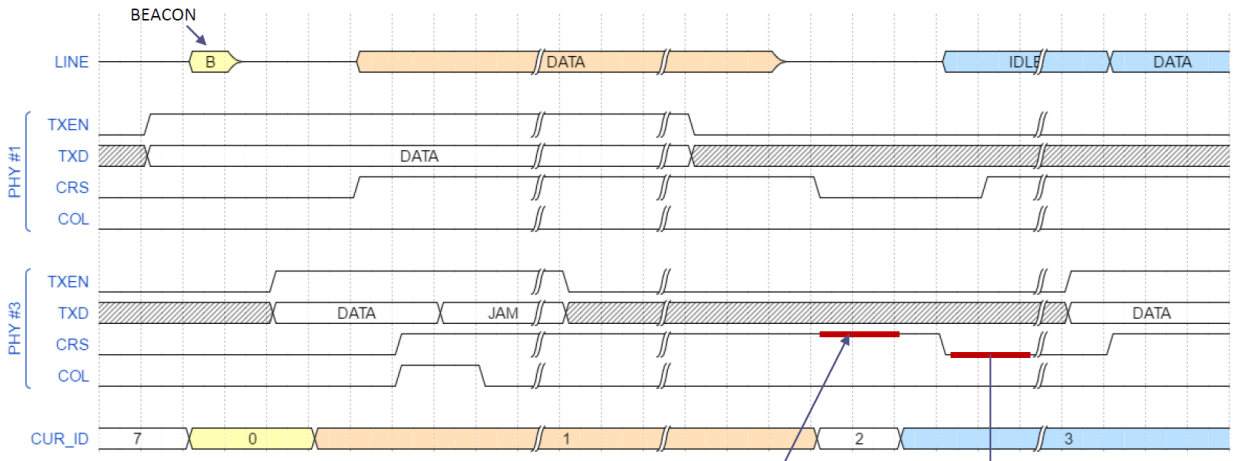
own time slot, this condition occurs at max in (N * TS_TIMER + BEACON_TIMER) bit times, which limits the required length of the delay line.

b) Another PHY puts a data on the line during its own time slot. In this case a transmission much longer than available delay line capacity is expected, thus a "logical" collision is signaled to the local MAC (COL = TRUE) to trigger a backoff and reset the delay line.

   As a consequence the local MAC will be ready to retransmit the same packet before the ongoing transmission ends (see clause 4.x.x.x). During this time, and until next chance to transmit, the CRS signal is forced in asserted state to prevent the MAC to deliver the packet before time (which would trigger more unwanted backoff).

   At this point CRS is de-asserted and SYNC symbols are put on the line to "commit" the time slot (have other PHYs stop their own TS_TIMER and prepare for receiving) until the local MAC delivers the packet, that is after one IPG period.

c) A false carrier is detected. In such case since the local TS_TIMER and time slot counter might not be in sync with other PHYs, a logical collision is triggered as in b) with the difference that a new BEACON must be received before retrying the transmission. If this happened to the master PHY, it will wait for all the slaves being silent for a safe amount of time before sending a new BEACON.



- BUS with 8 nodes
- Node #1 and #3 want to transmit data, others are silent
  - PHY #1 just defers TX until its own time slot is available
  - PHY #3 signals a collision because PHY #1 is transmitting, however:
    - No physical collisions on the line
    - Actual TX occurs immediately after PHY #1 transmission with no additional delay (MAX backoff + latency < MIN packet size)

148.2.1 PLCA Control

148.2.1.1 PLCA Control State Diagram

PLCA Control state machine is responsible for synchronizing time slots across the multidrop network and signaling other PLCA functions at which time data is allowed to be transmitted.

The PLCA Control function shall conform to the PLCA Control state diagram in figure ... and associated state variables, functions, timers and messages.

When PLCA functions are disabled, the PLCA control variables are reset to their default values and SILENCE is conveyed to the PCS through the tx_cmd variable, having the PHY work in normal CSMA/CD mode.

When PLCA functions are enabled the master PHY immediately switch to SEND_BEACON state to have slave PHYs synchronize their time slot counter and related timer. Slave PYHs wait in RESYNC state until a BEACON is signaled by PCS Receive via the rx_cmd variable.

The BEACON consists of at least four 'N' 5B symbols. Both the slave PHYs and the master PHY are required to detect the end of the BEACON before resetting the time slot timer. This is necessary since up to two 'N' symbols may be lost by the PMA Receive during DME and 5B boundary synchronization.

After syncing is done all PHYs have their time slot counters (curID) reset and their TS_TIMER started with a maximum skew of $\Delta RX_{lat} + T_{PD}$ where ΔRX_{lat} is the worst case receive latency difference among all the PHYs, while T_{PD} is the worst case propagation delay time between the master and all slave PHYs.

In WAIT_TS state the PHY waits for one of these possible conditions:

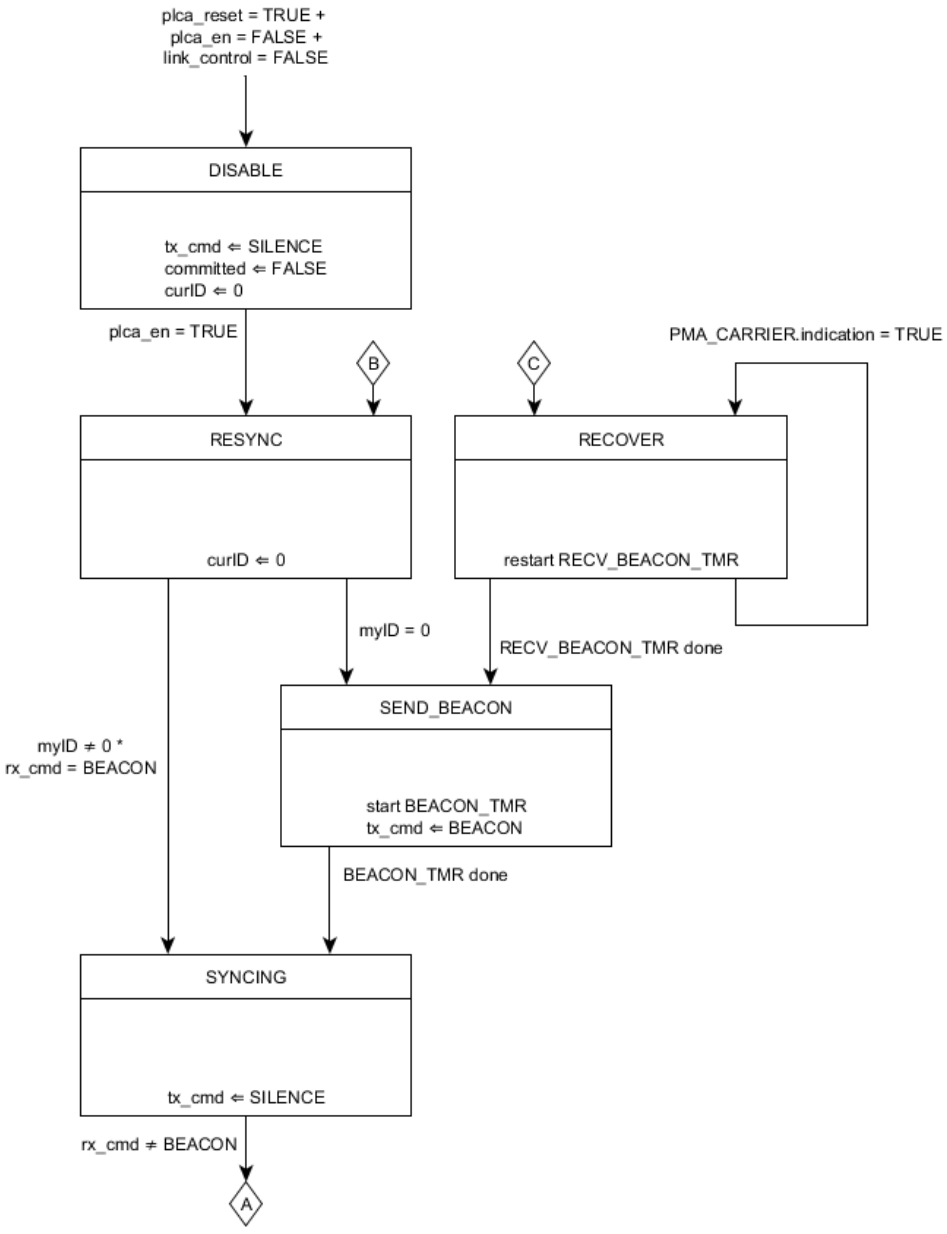
1. PMA achieves lock on a valid DME stream.
2. Time slot counter "curID" reaches "myID", signaling it's this PHY's turn to transmit
3. TS_TIMER elapses indicating the current time slot is yielded

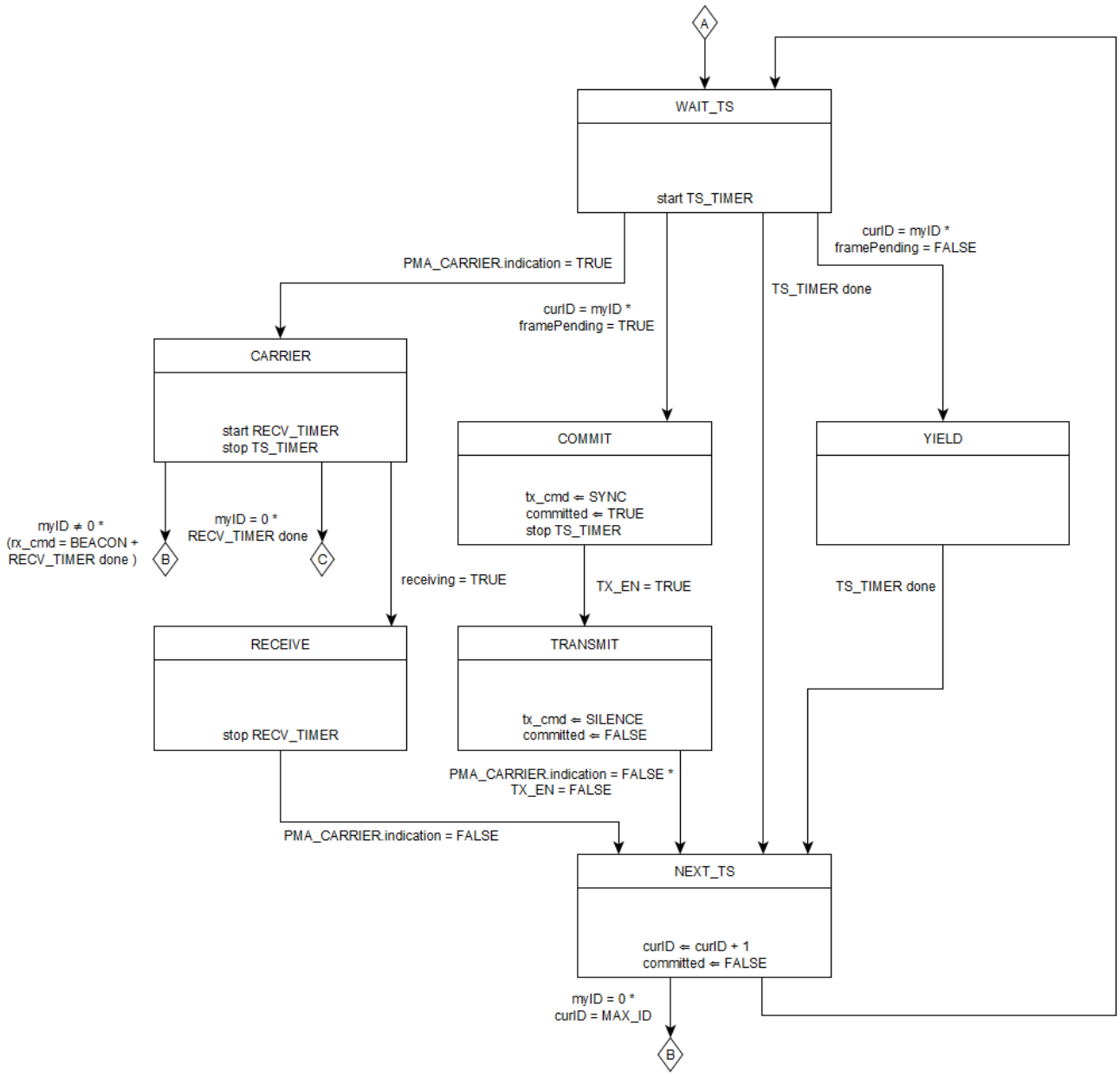
When first condition (1) occurs, it normally means that either a BEACON or a valid packet is about to be decoded and signaled by PCS Receive. However, depending on noise conditions, there's a low chance to have a false carrier indication instead.
PLCA relies on the less robust PMA_CARRIER.indication primitive (instead of the "receiving" variable) to detect a packet reception. This minimizes the time required to detect a "committed" time slot, allowing shorter time slots and improved efficiency.
To handle the unlikely event of a false carrier, an optimistic scheme is then used: PLCA control state machine assumes the indication of the PMA to be reliable and switch to CARRIER state arming the RECV_TIMER and stopping the TS_TIMER (i.e. assumes the time slot to be committed). At this point, if the "receiving" variable is set (good case) the state machine goes to RECEIVE state to actually receive the packet. If a BEACON is detected instead (still good case) it switches to RESYNC state. In case the RECV_TIMER expires, a recovery procedure is initiated to resynchronize the (possibly) misaligned TS_TIMER and/or time slot counter. The recovery procedure forces a slave PHY to wait for the next BEACON and a master PHY to wait for all slave PHYs to be silent for at least RECV_BEACON_TIMER before sending a new BEACON.

When condition (2) occurs PLCA Control samples the framePending variable to detect, at the very beginning of a time slot, if the MAC is ready to send out a packet. If not, the current time slot is yielded by wating for TS_TIMER to expire. Otherwise the time slot is committed by putting SYNC symbols on the line to have other PHYs PLCA Control state machine switch to CARRIER state in the minimum possible time. These additional SYNC symbols are discarded by the PCS Receive as described in 147.x.x.x.

When condition (3) is met the (minimum) time slot is wasted, time slot counter in incremented and timers are reset.

Note that the TS_TIMER is re-armed after a BEACON, after each wasted time slot and also after any successfully received packet. In such a way the worst case clock drift (200ppm) among PHYs is negligible compared to PLCA timings.





148.2.1.2 PLCA Control variables

plca_en — generated by management interface, enables PLCA functions. When set to FALSE the TX functions revert to standard CSMA/CD.
Value: TRUE or FALSE

link_control — generated by management interface, enables PCS TX and RX functions. When set to FALSE MII data from MAC is discarded and receiver functions are disabled.
Value: TRUE or FALSE

link_status — generated by PLCA reconciliation sublayer, informs the management interface that the PHY is ready to send/receive data via MII interface.

When PLCA function is not enabled/implemented link_status shall be continuously assigned to the link_control current value.
Value: TRUE or FALSE

myID — generated by the management interface, represents the PLCA time slot ID assigned to the PHY. Special value ‘0’ is assigned to the master node, indicating the PHY shall generate BEACON signals as described in ...
Value: integer value from 0 (master) to MAX_ID

MAX_ID — generated by the management interface, indicates the number of time slots to be allocated, that is the maximum number of PHYs that can join the multidrop network. This parameter is only meaningful for the master PHY (myID = 0), for slave PHYs is a don’t care.
Value: integer number from 0 to 255

committed — internal variable used to synchronize PLCA Control and Data functions as depicted in ... It is set by PLCA Control state machine to signal that the current time slot has been committed and the PLCA Data state machine is now allowed to convey MII data to the PCS.
Value: TRUE or FALSE

framePending — internal variable used to synchronize PLCA Control and Data functions as depicted in ... The PLCA Data state machine sets this variable when it detects the MAC is ready to send a packet in order to have the PLCA Control state machine actually commit the next available time slot.
Value: TRUE or FALSE

148.2.1.3 Functions

No functions are defined for the PLCA Control state machine.

148.2.1.4 Timers

BEACON_TIMER — represents the time for which the master PHY signals a BEACON condition on the line when a PLCA cycle starts. It shall be set to 20 BT to allow the slave PHYs to properly recover the signal.

RECV_TIMER — the time a PHY waits after PMA detects a carrier on the line (i.e. it is aligned at least on DME bit stream as described in ...) and the PCS RX actually achieves synchronization. The purpose of this timer is to allow early detection of carrier on the line to minimize time slot skew (see ...) allowing smaller time slots (see TS_TIMER) and increased efficiency. In presence of false carrier events, this timer expires and triggers a recovery function as described in ... (slave PHY waits for a new BEACON while master PHY waits for all slaves to be silent before sending a new BEACON). Timer value is implementation defined but shall be greater than PHY total RX latency including PMD, PMA and PCS RX.

TS_TIMER — this is the time slot timer, as defined in (...). It shall be set according to maximum allowed PHY TX and RX latencies and maximum MDI to MDI propagation

delay, as reported in (...).
For a 25m cable and 10BT of total RX+TX latency a safe default value is 20BT (see ...).

RECV_BEACON_TIMER

during a recovery operation (see ...) the master PHY needs to wait for all slave PHYs to be silent before sending a new BEACON.
This timer value shall be set at least to TS_TIMER * (MAX_ID + 1) for safe operations.

148.2.2 PLCA Data

148.2.2.1 PLCA Data State Diagram

PLCA Data state machine is responsible for detecting when the MAC is ready to send a packet and delay the transmission until the assigned time slot number is met, as described in 148.1.2.

The PLCA Data function shall conform to the PLCA Data state diagram in figure ... and associated state variables, functions, timers and messages.

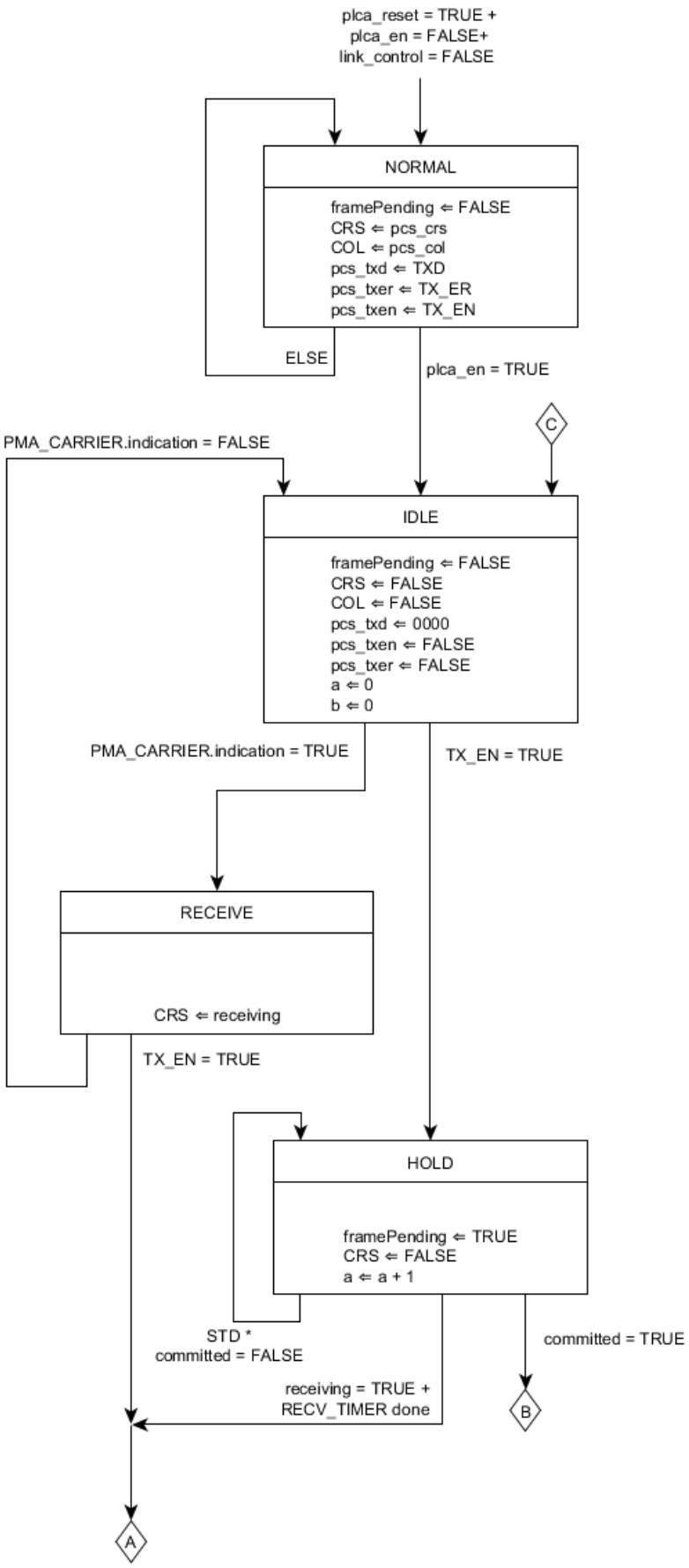
When PLCA functions are disabled, the PLCA data variables are reset to their default values and PCS signals are directly mapped to homonymous MII signals, having the PHY work in normal CSMA/CD mode.

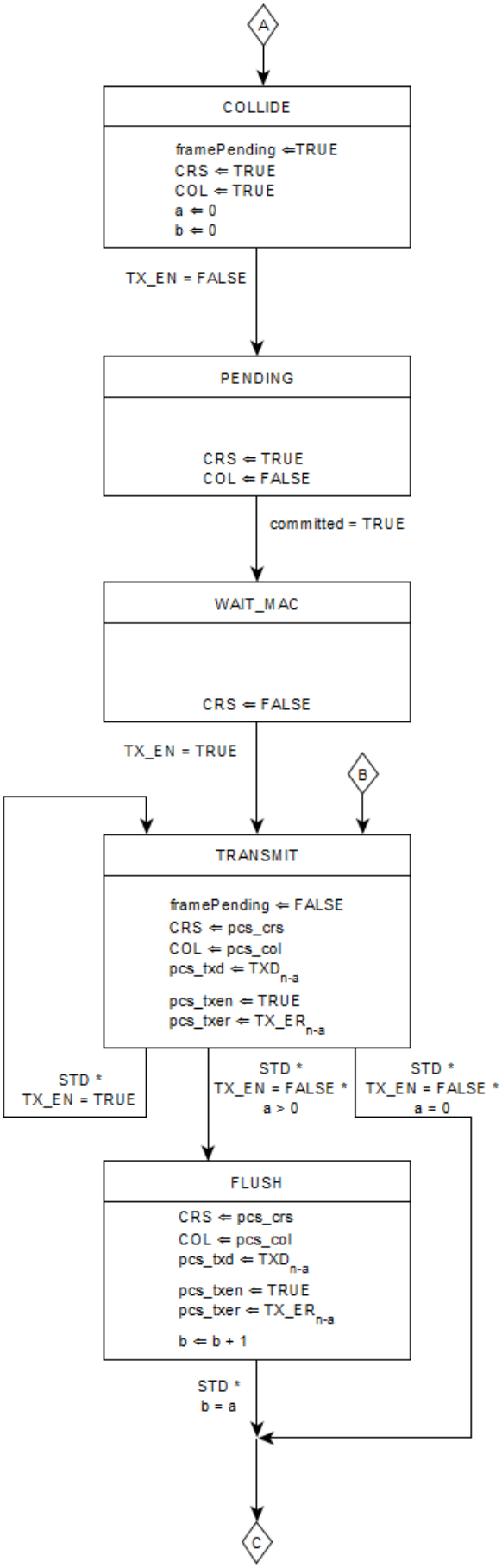
When PLCA functions are enabled the Data state machine waits for the MAC to start a transmission or the PMA to signal a carrier on the line via the PMA_CARRIER.indication primitive.
In the former case the incoming MII data is delayed by switching to HOLD state. In the latter case CRS is set to the MII to signal the presence of a carrier.

During RECEIVE state the CRS = TRUE condition prevents the MAC from sending a packet at that time. However there's a race condition where the MAC might have started a transmission right before the PHY asserts CRS but the TX_EN signal is still low due to the MAC internal latency (that would normally result in a physical collision when operating in CSMA/CD mode). In this case the Data state machine switches to the COLLIDE state to have the MAC perform a backoff and send the packet again later.

During the HOLD state the PLCA Control state machine is notified via the framePending variable that data is available to be transmitted and it's waiting for the appropriate time slot to unlock the transmission by setting the "committed" variable. In such case the PLCA Data state machine switches to TRANSMIT state to actually deliver the data to the PCS to encode and transmit on the line.
If another PHY starts a transmission during its time slot, it's not possible to still hold the data in the delay line and a logical collision is triggered as explained in 148.1.2 by switching to COLLIDE state.

From the COLLIDE state the PLCA Data state machine holds CRS asserted to prevent the MAC to make new attempts to transmit the packet, until PLCA Control state machine signals that it's time to deliver the packet. At that point CRS is de-asserted to have the MAC actually resend data after waiting one IPG period as described in clause 4.x.x.x


plca_reset = TRUE +
plca_en = FALSE+
link_control = FALSE
NORMAL
framePending ⇐ FALSE
CRS ⇐ pcs_crs
COL ⇐ pcs_col
pcs_txd ⇐ TXD
pcs_txer ⇐ TX_ER
pcs_txen ⇐ TX_EN
ELSE
plca_en = TRUE
C
PMA_CARRIER.indication = FALSE
IDLE
framePending ⇐ FALSE
CRS ⇐ FALSE
COL ⇐ FALSE
pcs_txd ⇐ 0000
pcs_txen ⇐ FALSE
pcs_txer ⇐ FALSE
a ⇐ 0
b ⇐ 0
PMA_CARRIER.indication = TRUE
TX_EN = TRUE
RECEIVE
CRS ⇐ receiving
TX_EN = TRUE
HOLD
framePending ⇐ TRUE
CRS ⇐ FALSE
a ⇐ a + 1
STD *
committed = FALSE
committed = TRUE
receiving = TRUE +
RECV_TIMER done
B
A


A
COLLIDE
framePending ⇐TRUE
CRS ⇐ TRUE
COL ⇐ TRUE
a ⇐ 0
b ⇐ 0
TX_EN = FALSE
PENDING
CRS ⇐ TRUE
COL ⇐ FALSE
committed = TRUE
WAIT_MAC
CRS ⇐ FALSE
TX_EN = TRUE
B
TRANSMIT
framePending ⇐ FALSE
CRS ⇐ pcs_crs
COL ⇐ pcs_col
pcs_txd ⇐ TXD n-a
pcs_txen ⇐ TRUE
pcs_txer ⇐ TX_ER n-a
STD *
TX_EN = TRUE
STD *
TX_EN = FALSE *
a > 0
STD *
TX_EN = FALSE *
a = 0
FLUSH
CRS ⇐ pcs_crs
COL ⇐ pcs_col
pcs_txd ⇐ TXD n-a
pcs_txen ⇐ TRUE
pcs_txer ⇐ TX_ER n-a
b ⇐ b + 1
STD *
b = a
C

148.2.2.2 PLCA Data variables

For the definition of pcs_reset, COL, CRS, TX_EN, TX_ER, TXD see ...
For the definition of pcs_txd, pcs_txen, pcs_txer see ...

148.2.2.3 Functions

No functions are defined for the PLCA Data state machine.

148.2.1.4 Timers

For the definition of RECV_TIMER see 148.2.1.4.

148.3 PLCA initialization

148.3.1 ID assignment

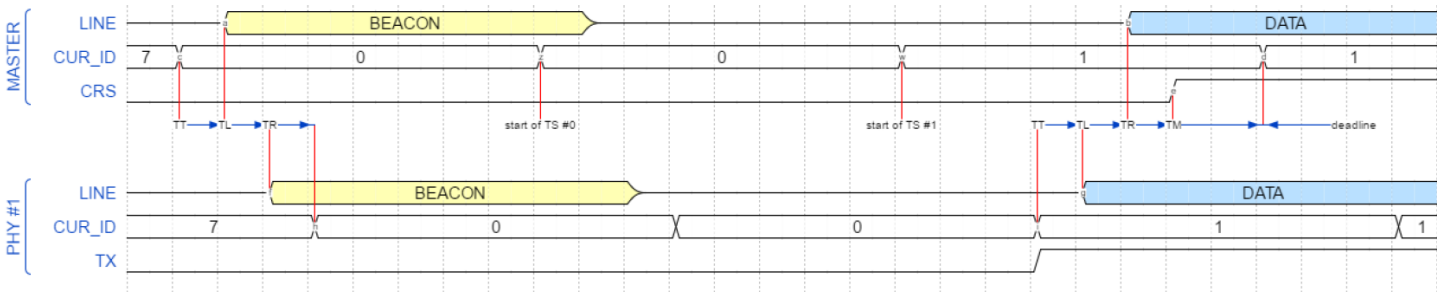
PLCA IDs have to be assigned by the management interface or equivalent method prior to asserting the link_control variable. Alternatively, PLCA IDs could be assigned using auto-negotiation protocol as described in clause 98.

148.3.2 Time Slot definition and requirements

The definition of the time slot timer (TS_TIMER) is critical for achieving the best PLCA performance and ensure a collision free multidrop bus.

Ideally the TS_TIMER should be as short as possible to minimize the waste of bandwidth due to yielded time slots. On the other hand, the TS_TIMER shall be long enough to compensate for:

1. worst case line propagation delay
2. worst case TX latency, defined as the time from pcs_txen asserted and the first bit of encoded pcs_txd data meeting the media.
3. worst case RX latency, defined as the time from the first bit of DME encoded data reaching the PMD and PMA_CARRIER.indication asserted.



TT: TX latency
TL: Line Propagation Delay
TR: RX Latency
TM: Margin

In the above picture the master PHY sends a BEACON which is received by the PHY #1 (i.e. with ID = 1) with a delay that includes the master's TX latency, the line propagation delay and its own RX latency. This is the base clock skew after a synchronization.

Subsequently PHY #1 transmits data during its own time slot and the master PHY receives with a delay that includes PHY #1 TX latency, the line propagation delay and its own RX latency.

For the PLCA to work properly each PHY needs to detect the carrier on the line within the limits of the proper time slot (in this example, time slot #1), that is TM > 0 for any transmission.

To satisfy the above condition TS_TIMER must be greater than the maximum clock skew, which is the above example is

MAX_SKEW = 2 * (TT + TL + TR)

Since the master PHY synchronizes its own TS_TIMER to the end of its received time slot (see PLCA Control State machine), the initial TX latency is compensated, thus the formula becomes:

MAX_SKEW = TT + 2 * (TL + TR).

Example:
In a typical scenario with a 25m long cable, considering two 10BASE-T1S PHYs at the edges, the TL parameter is ~1.7 bit times.
For most implementations a typical value for TT and TR parameters is respectively ~7 bit times and ~3 bit times, for a total SKEW of ~17 bit times.
Setting the MAX_SKEW parameter to 20 bit times (~1.6us) would yield a reasonable margin to allow proper PLCA operations.

148.3.2.2 Efficiency

The PLCA worst case efficiency depends on the maximum number of PHYs, the TS_TIMER and BEACON_TIMER settings.

When all PHYs are transmitting data in a single bus cycle, the actual efficiency can go up to
(N * AVG_PKT_SZ) / (N * AVG_PKT_SZ + BEACON_TMR)

where N is the number of PHYs, AVG_PACKET_SZ is the average size of the packet being transmitted in bit times.

For the minimum (72 bytes) and maximum (1542 bytes) possible value of AVG_PACKET_SZ, 8 nodes and a typical value of 20 bit times for BEACON_TIMER, the above equation yields
Emax = 99.9%, Emin = 99.5%. The efficiency loss in this case is due to the BEACON time alone.

The worst case is when only one PHY needs to transmit data while all other PHYs just yield the time slot. In such case the efficiency can be calculated as follows:
AVG_PKT_SZ / (AVG_PKT_SZ + (N-1) * TS_TIMER + BEACON_TIMER)

Repeating the above calculation for the min/max AVG_PKT_SZ and considering a typical value of TS_TIMER of 20 bit times, the above equation yields:
Emax = 98.7%, Emin = 78.3%

At any bus cycle, the instantaneous efficiency can be calculated as follow:

Eff = (A * AVG_PKT_SZ) / (A * AVG_PKT_SZ + (N – A) * TS_TIMER + BEACON_TIMER)

where
A is the number of PHYs that transmitted a packet during this bus cycle
AVG_PKT_SZ is the average size, in bits, of the packets that have been transmitted
N is the maximum number of PHYs
TS_TIMER and BEACON_TIMER are the parameters defined in x.x.x.x measured in bit times.

ANNEX TBD (PLCA Performance)

//// TODO: to be structured

A typical scenario where PLCA delivers high performance is a network of up to sixteen 10BASE-T1S PHYs connected by a single twisted pair copper cable up to 25m long, which yields propagation delays in the order of 2-bit times. For a performance comparison among PLCA, plain CSMA/CD and a generic TDMA based system see ...