University of New Hampshire
InterOperability Laboratory

UNH-IOL and **Dell EMC**

IEEE P802.3cg
Intra-System Proof-of-Concept

Madelyn Widger, UNH-IOL

www.iol.unh.edu

Agenda

- Overall goal: Proof-of-concept for Interoperable Backplane Intra-system
- Two simultaneous parts of project worked on at Dell EMC
  - Analysis of Backplane Channel
  - Developed FPGA emulator mounted Paddle Card

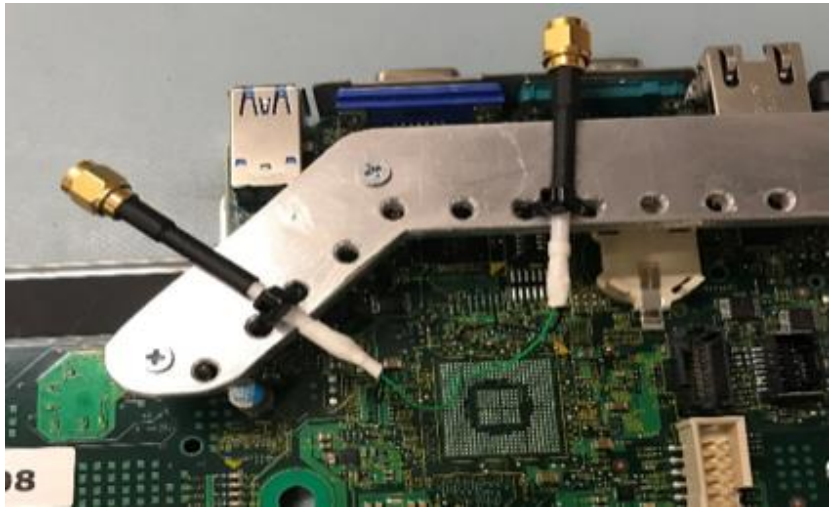
Proof-of-Concept Project and Goal

- Signal Integrity Measurements across existing planar
  - Backward-compatible feasibility with I2C
    - Traces were not routed specifically for optimizing the signal integrity
    - Measurements taken on ‘unbalanced’ I2C trace pairs within an existing system
    - **Goal: If results passed, routed traces would also pass for future emulation measurements**
- Developed a proof-of-concept platform to emulate future 10SPE PHYs
  - Built an FPGA system to emulate P802.3cg signaling
    - Signal Integrity testing of FPGA system mated with baseboard measuring varying trace lengths
    - **Goal: Examine the feasibility of running 10BASE-T1S signaling**

SI Measurements on an Existing Server Planar

- Measurements made on existing SCL & SDA trace pairs

Server Planar



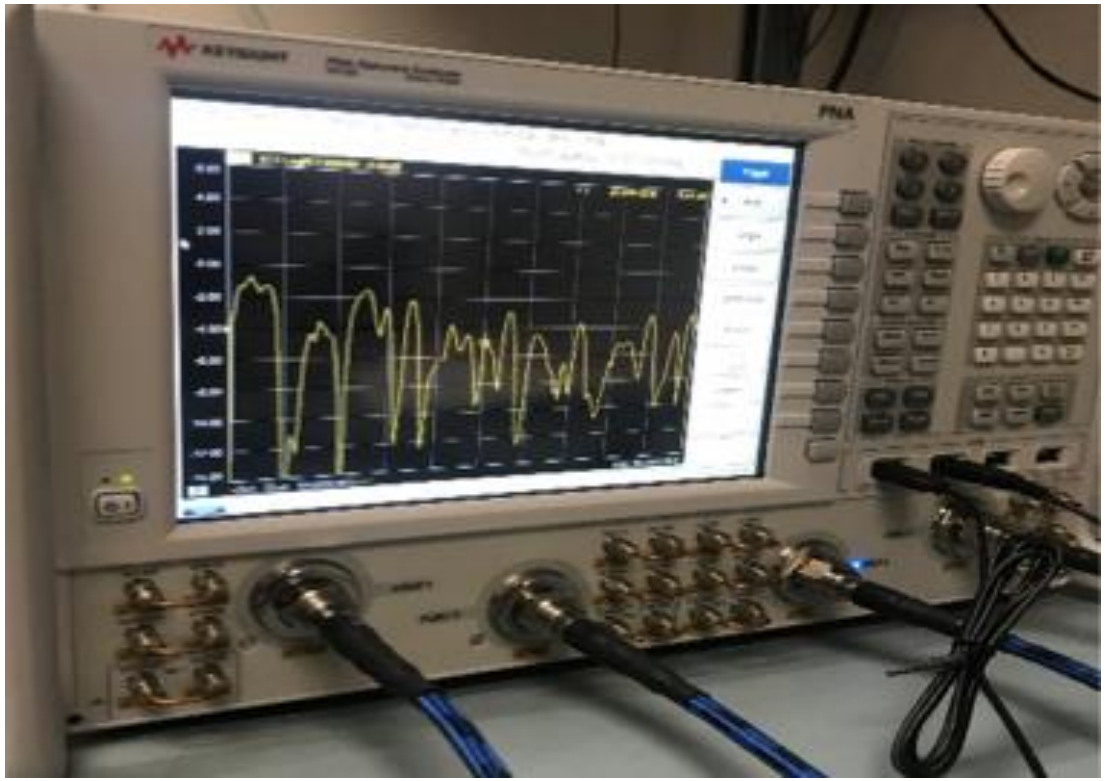
Board Management Controller (Bus Master)

Slave end points

SI Measurement Equipment Setup

- Keysight Vector Network Analyzers
  - E5063A: 300 KHz – 3 GHz
  - N5225A: 10 MHz – 50 GHz

- Analyzed S-Parameters
  - Return Loss: Sdd11, Sdd22
  - Insertion Loss: Sdd12, Sdd21



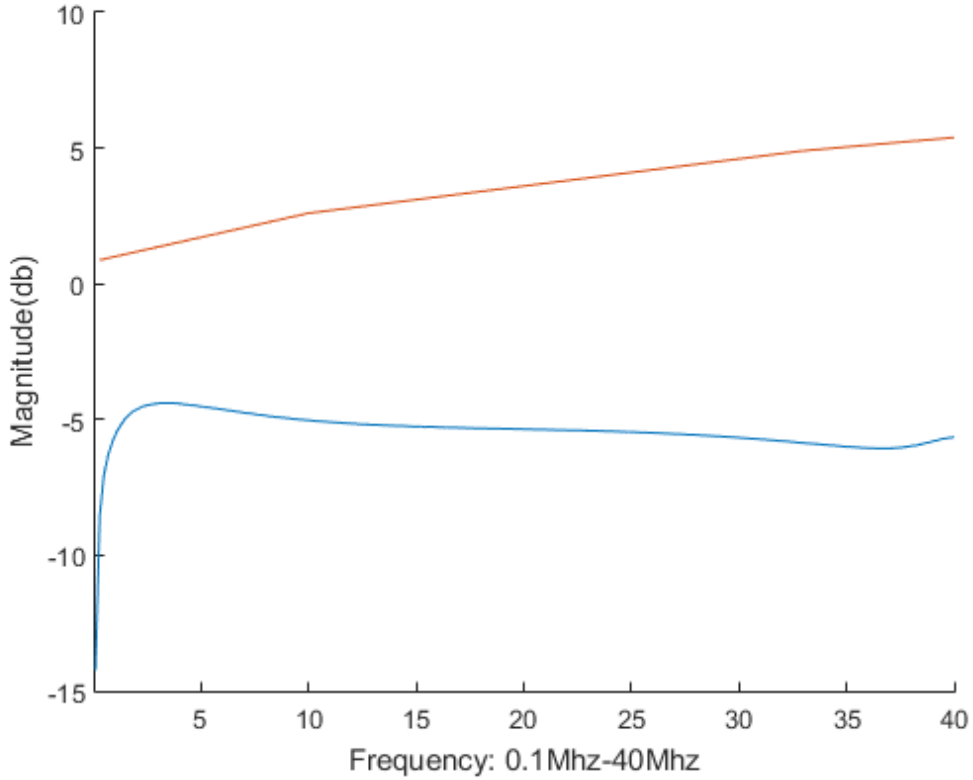
SI Measurement Results Based on Proposed Spec

Insertion Loss Limit for 10BASE-T1S: Clause 147.7.1

$$\text{InsertionLoss}(f) < \begin{cases} 1.0 + \dfrac{1.6(f-1)}{9} & 0.3 \le f < 10 \\ 2.6 + \dfrac{2.3(f-10)}{23} & 10 \le f < 33 \\ 4.9 + \dfrac{2.3(f-33)}{33} & 33 \le f \le 40 \end{cases} \text{ dB}$$

where

f is the frequency in MHz; $0.3 \le f \le 40$



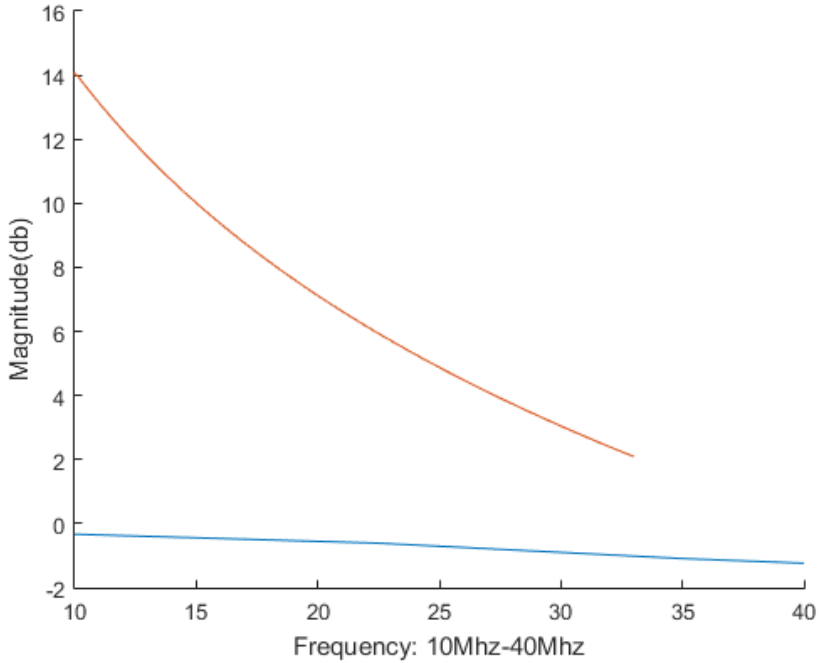
Measurement Results

Return Loss Limit for 10BASE-T1S: Clause 147.7.2

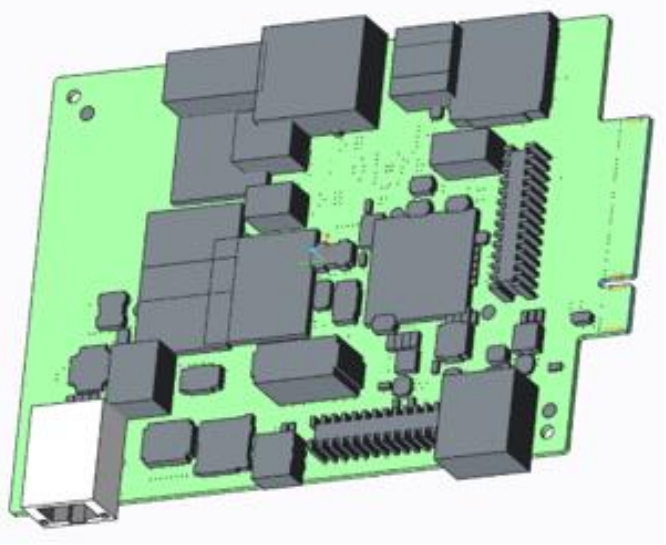
$$\text{ReturnLoss}(f) > \begin{cases} 14 & 0.3 \le f < 10 \\ 14 - 10\log_{10}\left(\frac{f}{10}\right) & 10 \le f \le 40 \end{cases} \text{ dB}$$

where

f is the frequency in MHz; $0.3 \le f \le 40$

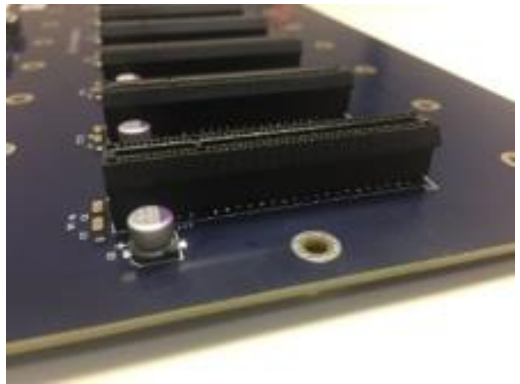


Development of Proof-of-Concept

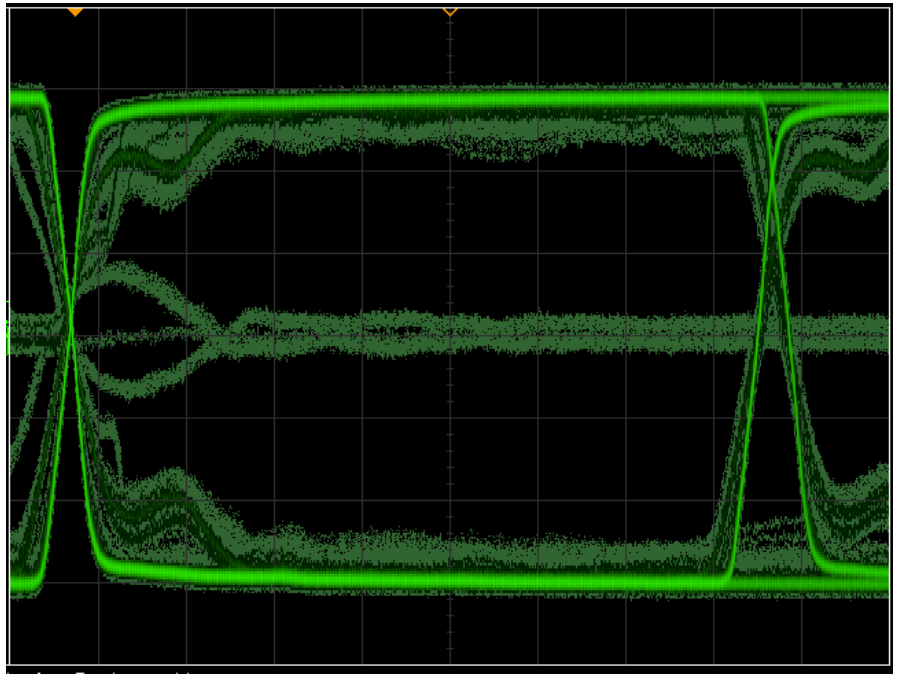
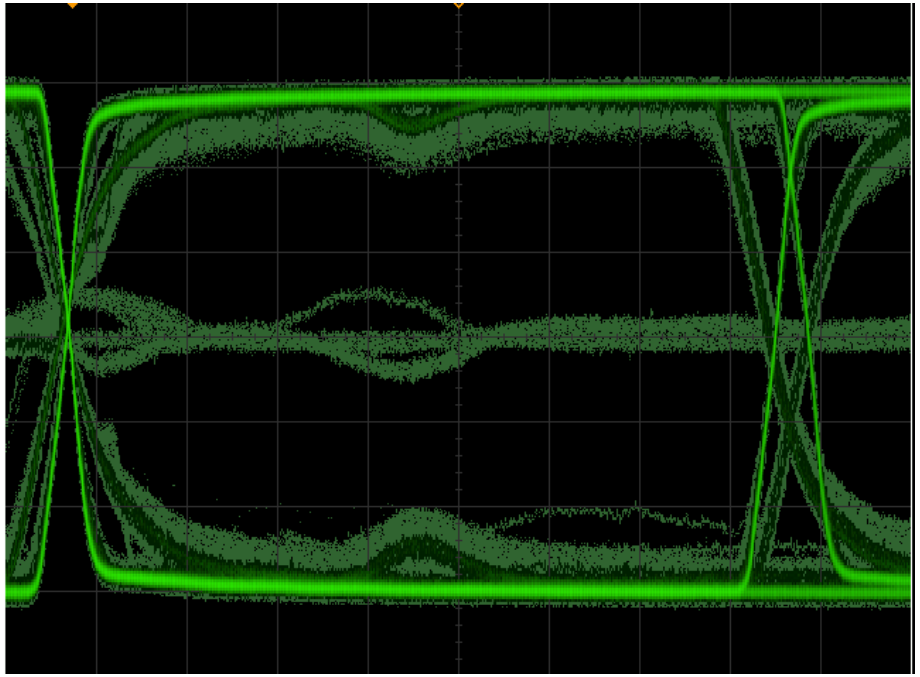


- FPGA development
  - Semiconductor company collaboration
  - OrCAD schematic design Layout

- Baseline Measurements
  - Due to timing constraints, prototype demo FPGA boards were obtained and used in measurements
  - Probed Multi-drop and Point-to-Point links, measuring TX Eye Diagram
  - Various channel lengths tested: 3” min and 48” max



Measured Eye Diagrams

3” trace	48” trace
	

Future Work & Summary

- Future Work
  - Collaboration with UNH-IOL for continued testing
  - Once finished, boards will be released and readily available.
- Foster multi-vendor Interoperability

Thank you all for you’re attention

Special Thank You to Jon Lewis and Dell EMC