Canova Tech

The Art of Silicon Sculpting

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IEEE 802.3cg

PLCA Burst mode fixes

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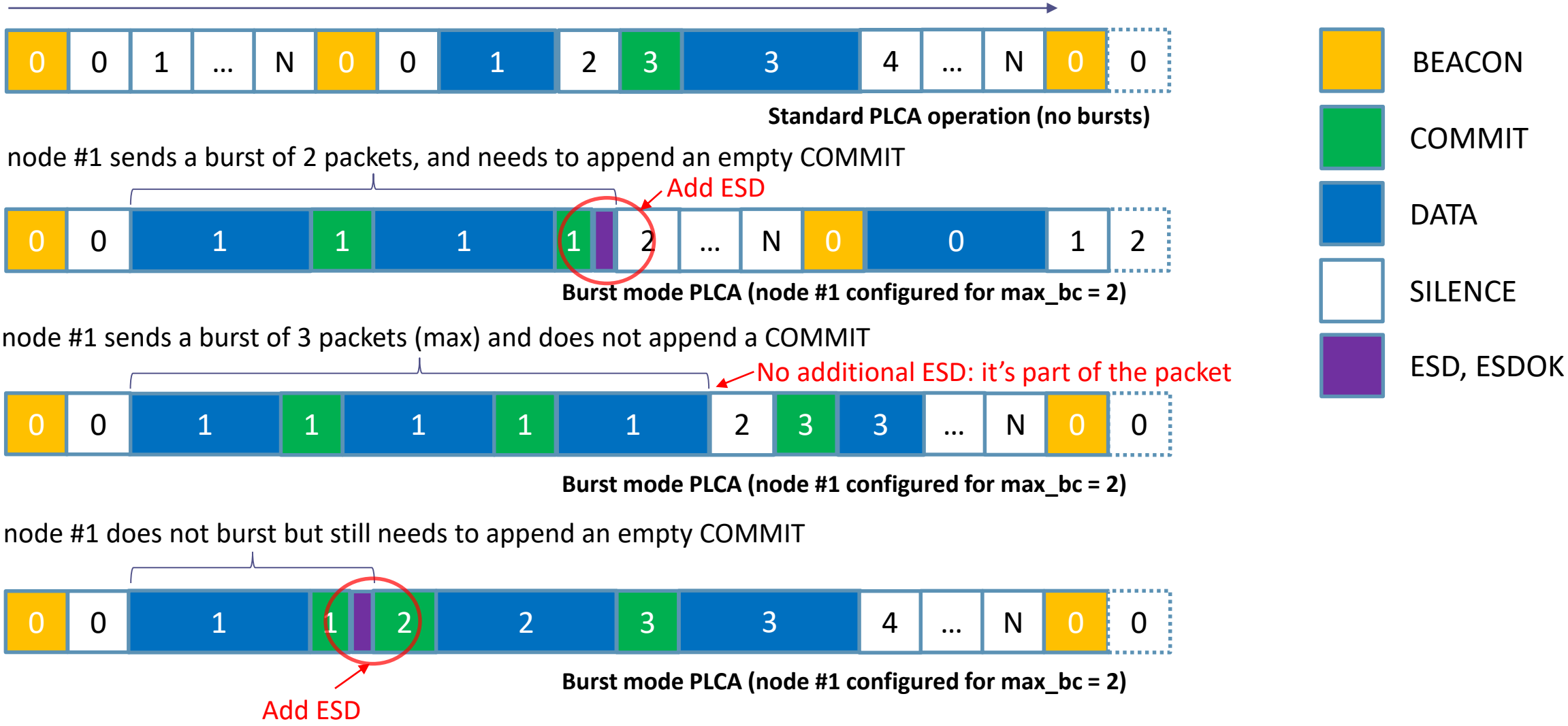
Outline

- PLCA burst mode has been added to Clause 148 in draft 2.2 as per http://www.ieee802.org/3/cg/public/Nov2018/beruto_3cg_PLCA_burst_mode_revB%20.pdf.
- The addition of this new feature created a (minor) problem in Clause 147
  - A COMMIT (coded as 'J' in 4B/5B) is added at the end of a packet when burst mode is enabled
    - Such COMMIT can be followed by either a packet or **silence**.
    - In the latter case the PCS RX signals a "False carrier" on the MII
      - This is not supposed to happen since it's normal burst mode behavior
- Besides, there was one missing change for Clause 148
  - Depending on implementation (internal delays), PLCA DATA State Diagram could detect a false reception when filling the IPG with idle.

Proposed solution

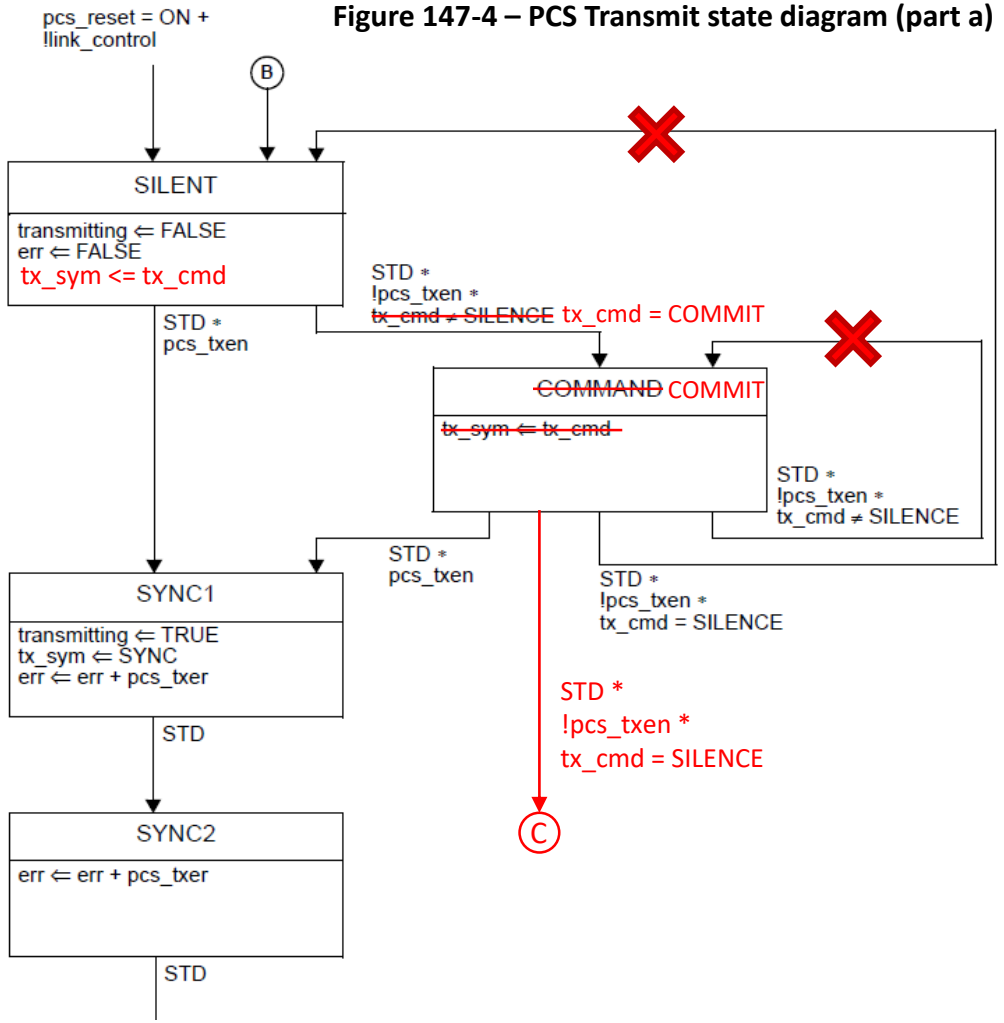
- Use explicit ESD, ESDOK 5B symbol sequence to end a COMMIT request when the MAC has no more packets to send in a burst
  - This prevents the spurious “FALSE carrier” indication
- Increase minimum DME silence period to guarantee at least one full 5B symbol of silence afterwards
- State diagram fix to Clause 147
  - The number of changes may look significant but the actual *–functional–* modification is very limited
- State diagram fix to Clause 148

Proposed solution



PCS TX state diagram changes

Figure 147-4 – PCS Transmit state diagram (part a)



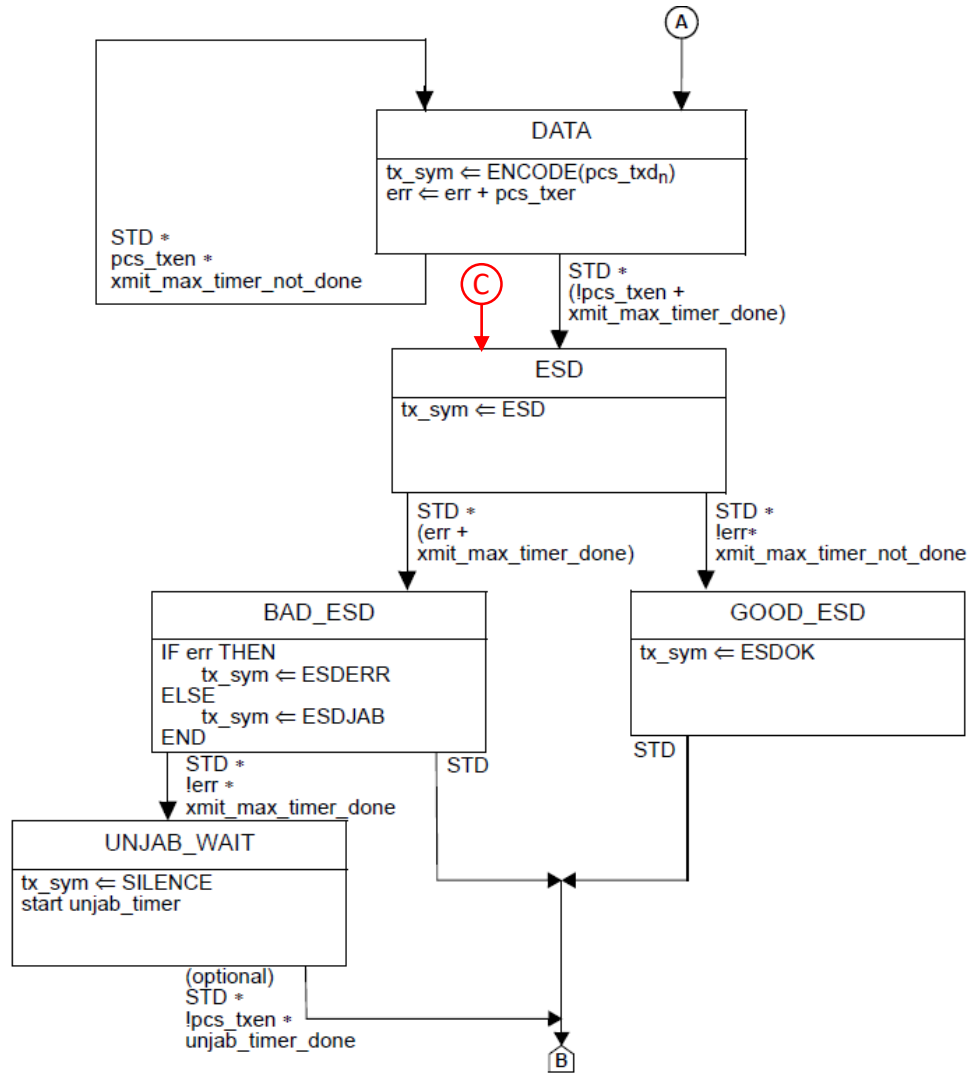


Figure 147–4—PCS Transmit state diagram (part b)

PMA and PCS RX state diagram changes

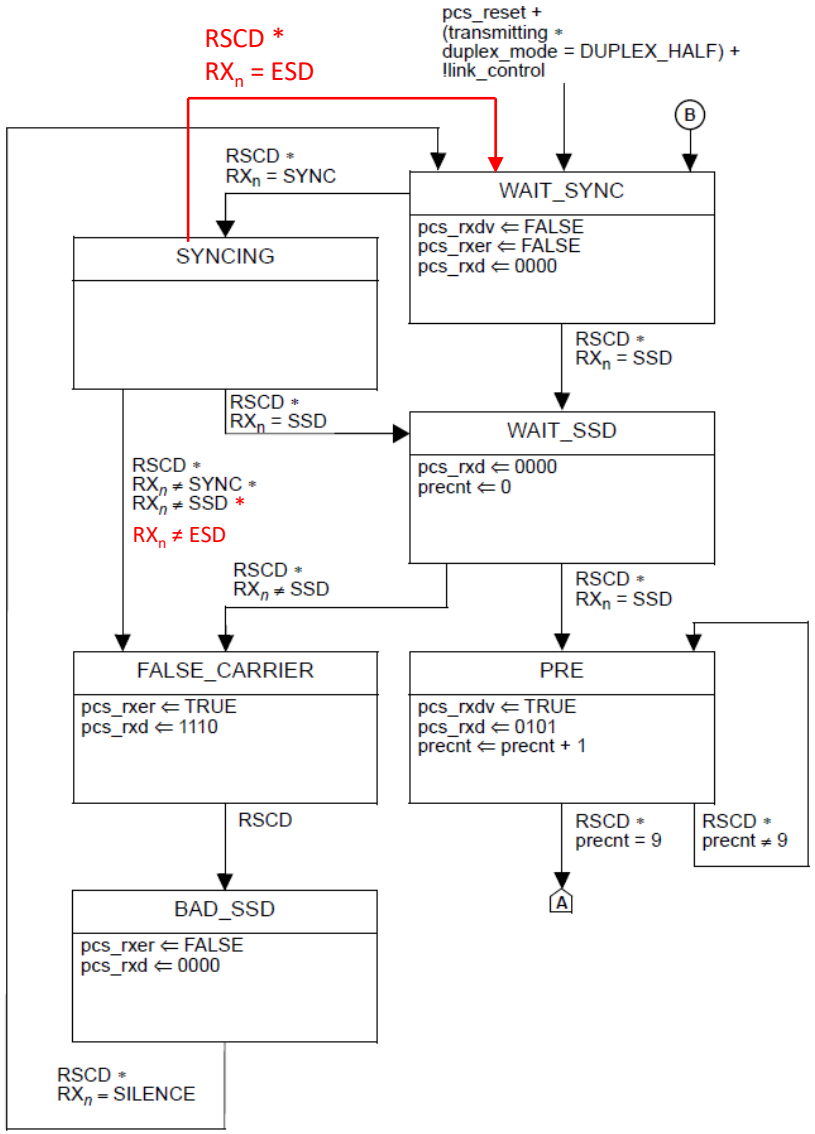
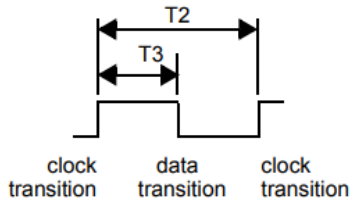


Figure 147–7—PCS Receive state diagram (part a)

Table 147–2—DME Timings

Parameter name	Description	Minimum value	Nominal value	Maximum value	Unit of measure
T1	Delay between transmissions	~~200~~ 480	—	—	ns
T2	Clock transition to clock transition	–100 ppm	80	+100 ppm	ns
T3	Clock transition to data transition (data = 1)	38	40	42	ns

480 ns is one 5B symbol + 1 DME encoded bit



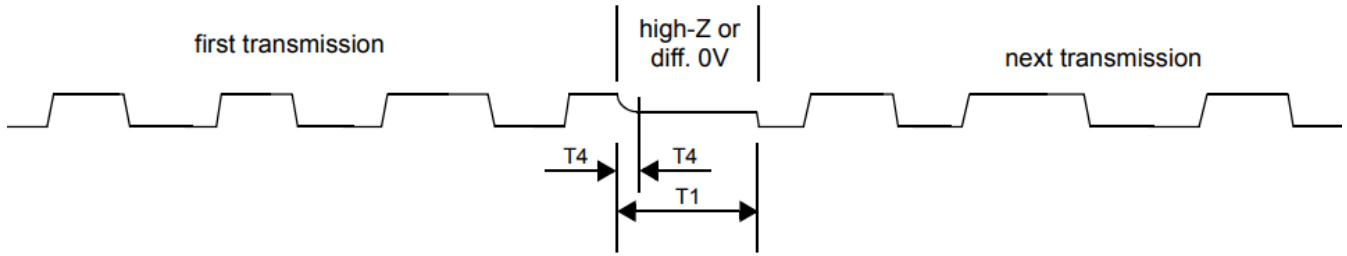


Figure 147–11—DME Encoding Scheme

PLCA DATA state diagram changes

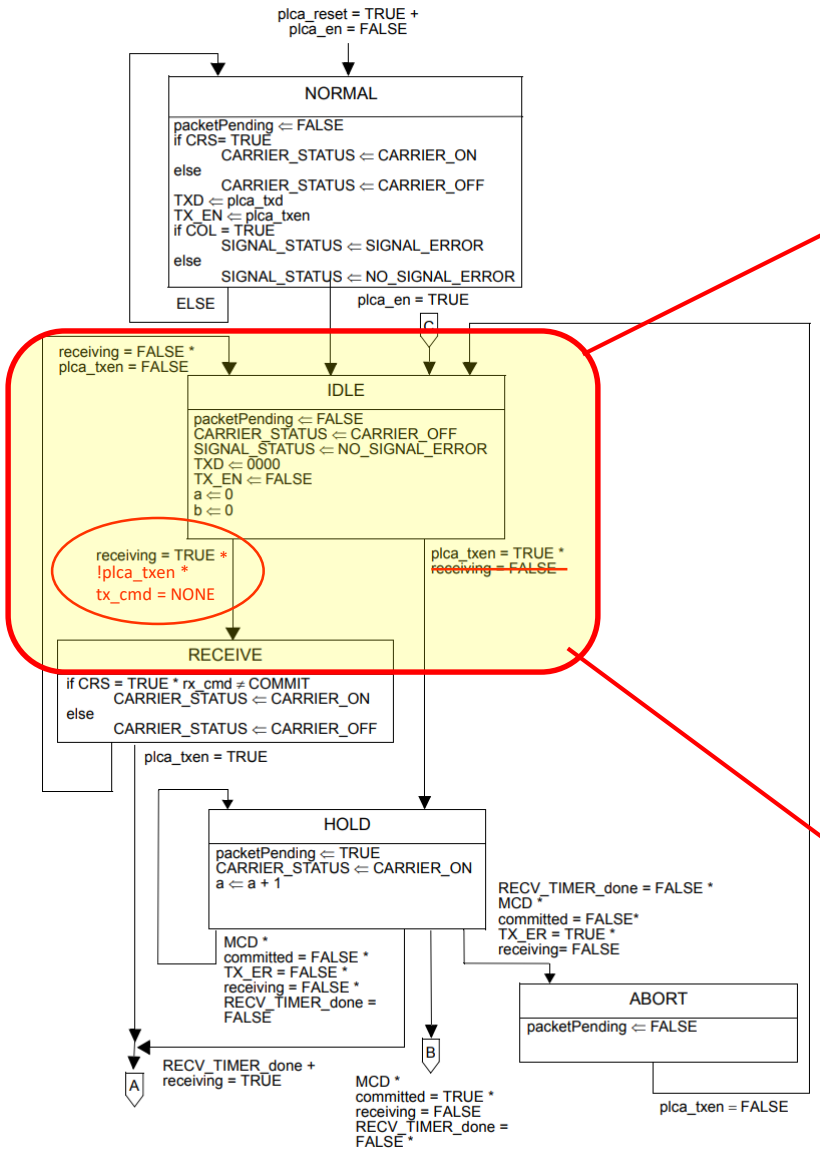
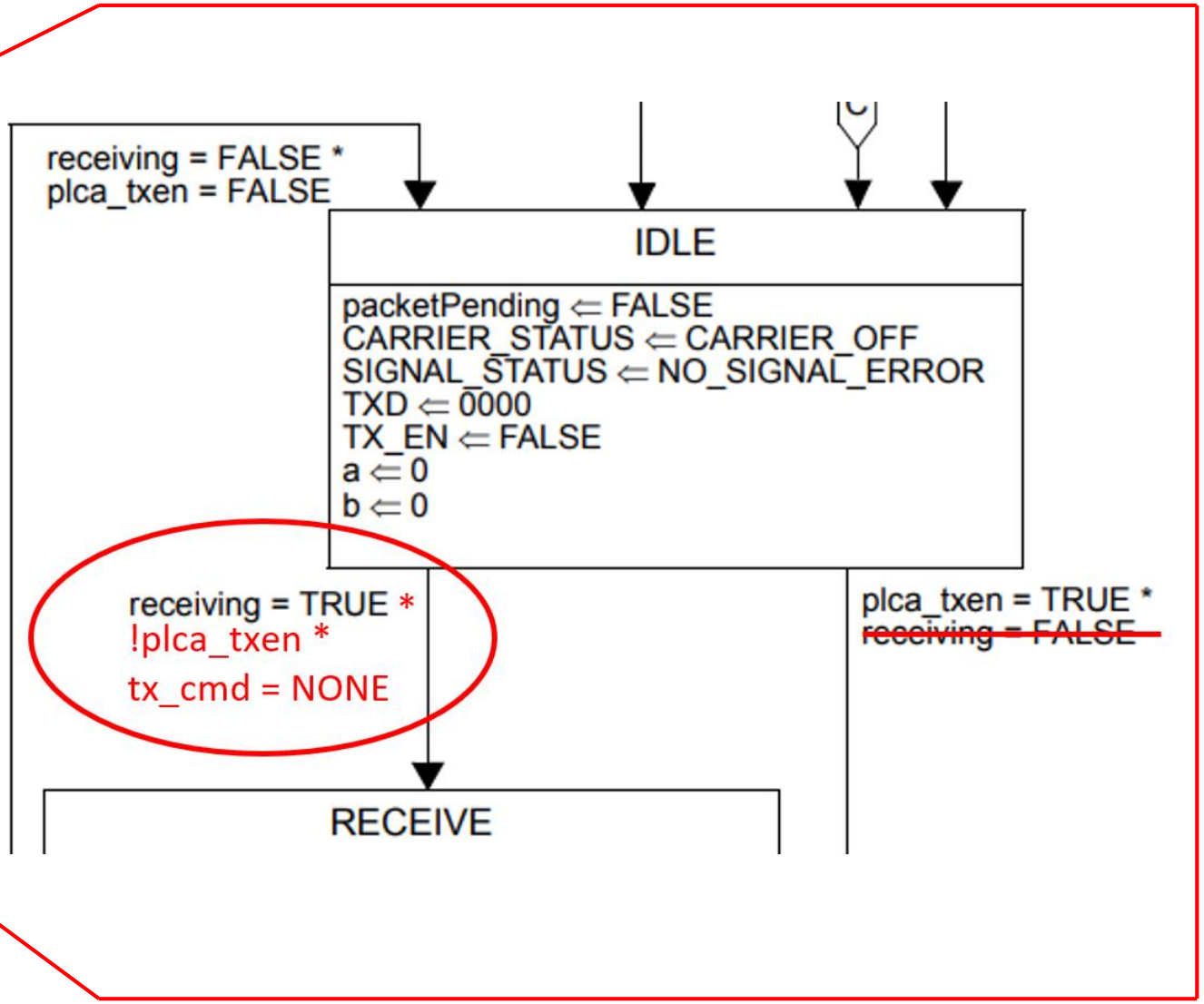


Figure 148–5—PLCA DATA state diagram



THANK YOU!