Transmitter Timing Jitter Proposal

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Test Mode 1 – Transmitter Clock Jitter

- Two PHYs linked and DUT provides access to reduced frequency transmit clock
- TX_TCLK175 = 5625MHz/32 = 175.7813 MHz
- ~ 200MHz preferred for pin output and test equipment
- Same TX_TCLK175 frequency used for all speeds, 10G, 5G & 2.5G
- Jitter limits scaled by $\frac{1}{\sqrt{S}}$, where S=1, 0.5 & 0.25 for 10G, 5G & 2.5G
- Follows jitter guidelines in 802.3an (10GBT) & 802.3bz (5G, 2.5G)
- Measure for 1ms with measuring device having bandpass BW > 200 MHz

Data Rate	Scaling Factor	Master Jitter rms	Master Jitter Peak to Peak	Slave Jitter rms	Slave Jitter Peak to Peak
10G	1	1 ps	10 ps	2 ps	20 ps
5G	$\frac{1}{\sqrt{0.5}}$	1.4 ps	14 ps	2.8 ps	28 ps
2.5G	$\frac{1}{\sqrt{0.25}}$	2 ps	20 ps	4 ps	40 ps

Test Mode 2 – Transmitter MDI Jitter

- One PHY configured as MASTER transmitting test sequence
- Same frequency 175.7813 MHz test pattern for all data rates, 10G, 5G & 2.5G
- 16*S symbols of +1 followed by 16*S symbols of -1 in MASTER timing mode.
- Jitter limits scaled by $\frac{1}{\sqrt{S}}$, where S=1, 0.5 & 0.25 for 10G-T1, 5G-T1 & 2.5G-T1
- Follows jitter guidelines in 802.3an (10GBT) & 802.3bz (5G, 2.5G)
- Measure for 1ms with measuring device having bandpass BW > 200 MHz

Data Rate	Scaling Factor	Master Jitter rms	Master Jitter Peak to Peak
10G	1	1 ps	10 ps
5G	$\frac{1}{\sqrt{0.5}}$	1.4 ps	14 ps
2.5G	$\frac{1}{\sqrt{0.25}}$	2 ps	20 ps

- 1000BASE-T1 Comparison:
  - $750\ MBd = \frac{5625\ MBd}{7.5}$
  - 5 ps master jitter rms / 7.5 < 1 ps
  - 50 ps master jitter peak to peak
  - 10 ps slave jitter rms
  - 100 ps slave jitter peak to peak
  - Measuring device BW > 2 MHz

Proposed Modifications to Draft Standard 1/3

149.5.1 Test Modes, replace page 152 lines 25-32 with the following text

Test mode 1 enables testing of timing jitter on MASTER and SLAVE transmitters. MASTER and SLAVE PHYs are connected over a link segment defined in 149.7. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_175. TX_TCLK_175 is equal to 5625MHz divided by 32.

Test mode 2 is for transmitter jitter testing on MDI when transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous pattern of 16*S {+1} symbols followed by 16*S {–1} symbols with the transmitted symbols timed from its local clock source.

[Note: From 149.1.1 Nomenclature, the parameter *S* is used for scaling. For 2.5GBASE-T1, *S* = 0.25; for 5GBASE-T1, *S* = 0.5; and for 10GBASE-T1, *S* = 1.]

[Changes from Draft are indicated in Red]

Proposed Modifications to Draft Standard 2/3

149.5.2.3 Transmit timing jitter, add the following lines

The transmitter timing jitter is measured by capturing the TX_TCLK175 waveform in both MASTER and SLAVE configurations while in test mode 1 using the transmitter test fixture 3 shown in Figure 149-35. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the MASTER TX_TCLK175 jitter relative to an unjittered reference shall be less than 1/sqrt(S) ps. The peak-to-peak value of the MASTER TX_TCLK175 jitter relative to an unjittered reference shall be less than 10/sqrt(S) ps.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the SLAVE TX_TCLK175 jitter relative to an unjittered reference shall be less than 2/sqrt(S) ps. The peak-to-peak value of the SLAVE TX_TCLK175 jitter relative to an unjittered reference shall be less than 20/sqrt(S) ps.

TX_TCLK175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be larger than 200 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

[Note: From 149.1.1 Nomenclature, the parameter *S* is used for scaling. For 2.5GBASE-T1, *S* = 0.25; for 5GBASE-T1, *S* = 0.5; and for 10GBASE-T1, *S* = 1.]

[Note: Changes from **802.3bp-2016** are indicated in Red]

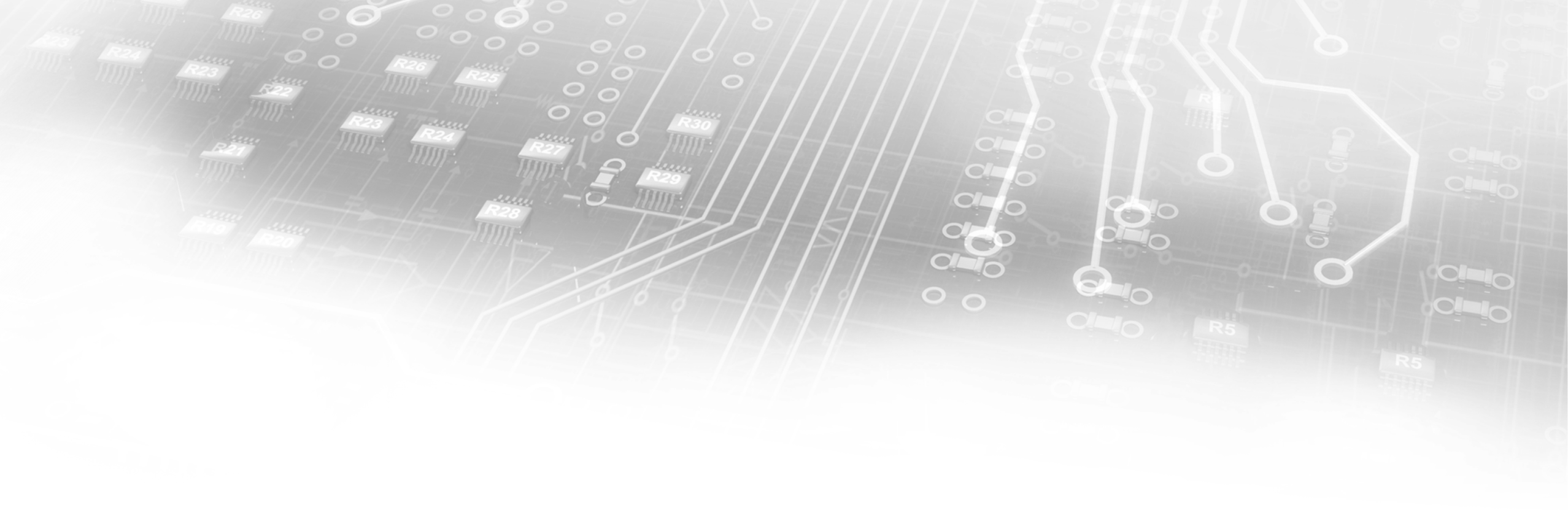
Proposed Modifications to Draft Standard 3/3

149.5.2.3 Transmit timing jitter, add the following lines (modified from IEEE Std 802.3bp-2016)

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 and using test fixture 4 as shown in Figure 149-36. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than 1/sqrt(S) ps. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than 10/sqrt(S) ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 200 MHz. Unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

[Note: From 149.1.1 Nomenclature, the parameter *S* is used for scaling. For 2.5GBASE-T1, *S* = 0.25; for 5GBASE-T1, *S* = 0.5; and for 10GBASE-T1, *S* = 1.]

[Note: Changes from **802.3bp-2016** are indicated in Red]



THANK YOU