Limiting Interleaving Options

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RS-Interleaving

- Cover ISO 7637-3 transients of 50ns
- 2 opinions: 60ns is sufficient, or 110ns sufficient
- RS (360, 326) with 1x, 2x, 4x, 8x interleaving

	Interleaving			
	1X	**2X**	**4X**	**8X**
10G	15	30	60	121
5G	30	60	121	242
2.5G	60	121	242	484

Protection (ns)

	Interleaving			
	1X	**2X**	**4X**	**8X**
10G	350	700	1401	2802
5G	700	1401	2802	5604
2.5G	1401	2802	5604	11207

Latency (ns)

Combinations

- Do we want all 4 interleaving options for every speed?

- Do we allow mix/match between 2 PHYs?

Theory vs Practice

- In theory once we build 8x interleaving for 10G, getting 4x, 2x, and 1x is no big deal.
- In practice the validation and interoperability testing gets complex
- In practice there is a cost to include all options

		Vendor A PHY			
		1X	**2X**	**4X**	**8X**
Vendor B PHY	**1X**	test	test	test	test
	2X	test	test	test	test
	4X	test	test	test	test
	8X	test	test	test	test

16 permutations each speed

Theory vs Practice

- It's actually worse
- Which permutations do you NOT test and still certify interoperability?

		Vendor A PHY			
		1X	**2X**	**4X**	**8X**
Vendor B PHY	**1X**	test	test	test	test
	2X	test	test	test	test
	4X	test	test	test	test
	8X	test	test	test	test

16 permutations interleave

X Master/Slave X

2 permutations

		Vendor A PHY			
		None	**1+D**	**1-D**	**1-D^2**
Vendor B PHY	**None**	test	test	test	test
	1+D	test	test	test	test
	1-D	test	test	test	test
	1-D^2	test	test	test	test

1 to 16 permutations precoding depending on what's supported

Let's Eliminate Unnecessary Options

- Delete options that cannot protect against ISO 7637-3 transients of 50ns
- Delete options that introduces excess latency that most likely will never be used

	Interleaving			
	1X	**2X**	**4X**	**8X**
10G	~~15~~	~~30~~	60	121
5G	~~30~~	60	121	242
2.5G	60	121	242	484

Protection (ns)

	Interleaving			
	1X	**2X**	**4X**	**8X**
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5G	700	1401	2802	~~5604~~
2.5G	1401	2802	~~5604~~	~~11207~~

Latency (ns)

Two Options at Each Speed

- Low Latency or High Protection

	Interleaving			
	1X	**2X**	**4X**	**8X**
10G			Low	High
5G		Low	High	
2.5G	Low	High		

- No mix and match
  - If one PHY advertises high protection then both PHYs must operate in high protection mode
  - Consistent superframe size can help simplify how we do LPI.

Helps with 2.5G only implementations

- Eliminates extra RS circuitry and buffering needed for 4x and 8x interleaving.

1X Option at 10G

- Natural clock cycle time for non-parallelized Reed Solomon implementation is 1 RS symbol per clock cycle.
- @ 10G no interleaving – 1 RS symbol time clock is 1.125 GHz.
- nX Interleaving allows this clock to slow down by 1/n (i.e. 10G 4x interleaving is 281.25 MHz)
- Depending on process technology 10G as 1X interleaving may be an issue at 1.125 GHz. Can do parallel design just for this case.
- May be a good idea to eliminate the 10G 1x interleave option – only 15ns burst protection, potential circuit timing issues.

If 60ns protection is sufficient then

- Eliminate 8x option

- One option per speed
  - 10G – 4x interleave
  - 5G – 2x interleave
  - 2.5G – 1x interleave

THANK YOU