Clause 45 PHY Registers for 802.3ch and Precoder Testing

IEEE P802.3ch MultiGigabit Automotive Ethernet PHY Task Force

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Basic Approach

- Reviewed and modeled after 1000BASE-T1 register set
- Since the 3 PHYs are in 1 clause, followed approach from 802.3bq/bz of having a single “MultiGBASE-T1” register for 2.5G/5G/10GBASE-T1 and not defining 3 separate register sets.
- Reviewed MultiGBASE-T Registers for additional functions

Definition, MultiGBASE-T1

Clause 1:

Insert new definition for MultiGBASE-T1 after 1.4.334 MultiGBASE-T

1.4.344a MultiGBASE-T1: PHYs that belong to the set of specific BASE-T1 PHYs at speeds in excess of 1000 Mb/s, including 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1. (See IEEE Std 802.3, Clause 149.)

PMA and PCS Registers

45.2.1 PMA/PMD Registers

Insert new rows to Table 45-3 for registers 1.2309 – 1.2316 after row for register 1.2308, and adjust reserved row as shown (unchanged rows not shown):

Table 45-3 PMA/PMD registers

Register address	Register name	Subclause
1.2309	MultiGBASE-T1 PMA control	45.2.1.192
1.2310	MultiGBASE-T1 PMA status	45.2.1.193
1.2311	MultiGBASE-T1 training	45.2.1.194
1.2312	MultiGBASE-T1 link partner training	45.2.1.195
1.2313	MultiGBASE-T1 test mode control	45.2.1.196
1.2314	MultiGBASE-T1 SNR operating margin	45.2.1.197
1.2315	MultiGBASE-T1Minimum margin	45.2.1.198
1.2316	MultiGBASE-T1 Rx signal power	45.2.1.199
~~1.2309~~1.2317 through 32767	Reserved	

45.2.3 PCS Registers

Insert new rows to Table 45-176 for registers 1.2318 – 1.2320 after row for register 1.2317, and adjust reserved row as shown (unchanged rows not shown):

Table 45-176 PCS registers

Register address	Register name	Subclause
3.2318	MultiGBASE-T1 PCS control	45.2.3.76
3.2319	MultiGBASE-T1 PCS status 1	45.2.3.77
3.2320	MultiGBASE-T1 PCS status 2	45.2.3.78
~~3.2318~~3.2321 through 32767	Reserved	

Text

- Text for the registers is found in zimmerman_3ch_02_1118.pdf

Margin reporting – like 10GBASE-T

Editor's Note (to be removed prior to Working Group ballot): Other PMA/PMD registers common in BASE-T PHYs which may be considered follow, if adopted, these would also need to be added to Table 45-3

45.2.1.197 MultiGBASE-T1 SNR operating margin register (Register 1.2314)

Register 1.2314 contains the current SNR operating margin measured at the slicer input for the PMAs in the MultiGBASE-T1 set. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.198 MultiGBASE-T1 Minimum margin register (Register 1.2315)

Register 1.2315 contains a latched copy of the lowest value observed in the MultiGBASE-T1 SNR operating margin register (1.2314) since the last read. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.199 MultiGBASE-T1 RX signal power register (Register 1.2316)

The MultiGBASE-T1 RX signal power register is read only and contains the receive signal power measured at the MDI. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or PMA_Training_Init_S (as appropriate, see 55.4.6.1, 113.4.6.1, and 126.4.6.1), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

Fault Reporting

- 1000BASE-T1 – adds optional PMA receive fault in PMA status, indicated by Ability bit, as well as (non-optional) PCS fault bit
  - Not latching – this is the model shown for 10G
- Follow 1000BASE-T1 model (only specify PMA receive fault)
  - It's simpler and provides functionality

Precoder Testing

- Addition of the precoder added some registers to the set reviewed in the ad hoc
- PMA Control sets the precoder for testing or to force
- PMA Training sets the precoder to request from the link partner
- Test mode 3 is used to generate a simple sequence to check the precoder

Easy precoder test

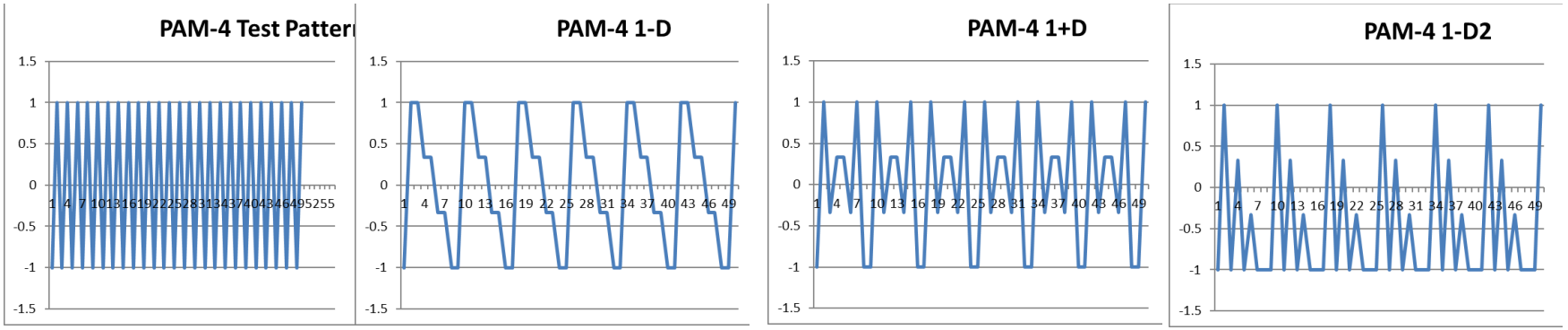
- Simple {0,3} repeating sequence generates nice periodic patterns from the precoder options – easily distinguishable

149.5.1 Test modes

Change Table 149-7 4th body row (value 011, page 89 line 10) to be "Test mode 3 – Precoder test mode"

Change text on page 89 line 34 as shown:

Test mode 3 is ~~not defined and the corresponding register is reserved for future use.~~for testing the precoder operation. When test mode 3 is enabled, the PCS shall generate a continuous pattern of {0, 3} symbols to be input to the PMA, precoded according to the Transmit precoder settings as determined by the value set in register 1.2309:10:9, or, equivalent functionality if MDIO is not implemented, and transmitted by the PMA timed from its local clock source.



REGISTER TABLES (BACKUP)

PMA Control

Table 45-155a MultiGBASE-T1 PMA control register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2309.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2309.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2309.13:12	Reserved	Value always 0	RO
1.2309.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2309.10:9	Transmit Precoder setting	00 = transmit with no precoder 01 = transmit with 1-D precoder 10 = transmit with 1+D precoder 11 = transmit with $1-D^2$ precoder	R/W
1.2309.8:0	Reserved	Value always 0	

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

PMA Status

Table 45-155b MultiGBASE-T1 PMA status register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2310.15:12	Reserved	Value always 0	RO
1.2310.11	MultiGBASE-T1 OAM Ability	1 = PHY has MultiGBASE-T1 OAM ability 0 = PHY does not have MultiGBASE-T1 OAM ability	RO
1.2310.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2310.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2310.8	Low-power ability	1 = PHY has low-power ability 0 = PHY does not have low-power ability	RO
1.2310.7:3	Reserved	Value always 0	RO
1.2310.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2310.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2310.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LL = Latching low

Training/ link partner training

Table 45-155c MultiGBASE-T1 training register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2311.15:11	Reserved	Value always 0	RO
1.2311.10:4	User field	7-bit user defined field to send to the link partner	R/W
1.2311.3:2	Precoder requested	00 = no precoder requested 01 = 1-D precoder requested 10 = 1+D precoder requested 11 = 1-D^2 precoder requested	R/W
1.2311.1	MultiGBASE-T1 OAM advertisement	1 = MultiGBASE-T1 OAM ability advertised to link partner 0 = MultiGBASE-T1 OAM ability not advertised to link partner	R/W
1.2311.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

Table 45-155d MultiGBASE-T1 link partner training register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2312.15:11	Reserved	Value always 0	RO
1.2312.10:4	Link partner user field	7-bit user defined field received from the link partner	RO
1.2311.3:2	Link partner precoder requested	00 = no precoder requested 01 = 1-D precoder requested 10 = 1+D precoder requested 11 = 1-D^2 precoder requested	RO
1.2312.1	Link partner MultiGBASE-T1 OAM advertisement	1 = Link partner has MultiGBASE-T1 OAM ability 0 = Link partner does not have MultiGBASE-T1 OAM ability	RO
1.2312.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

PMA Test Mode Control

Table 45-155e MultiGBASE-T1 test mode control register bit definitions

Bits(s)	Name	Description	R/W[a]
1.2313.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2313.12:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write

PCS Control

Table 45-244a MultiGBASE-T1 PCS control register bit definitions

Bits(s)	Name	Description	R/W[a]
3.2318.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2318.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2318.10:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

PCS Status 1

Table 45-244b MultiGBASE-T1 PCS status 1 register bit definitions

Bits(s)	Name	Description	R/W[a]
3.2319.15:12	Reserved	Value always 0	RO
3.2319.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2319.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2319.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2319.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2319.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2319.6:3	Reserved	Value always 0	RO
3.2319.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2319.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

PCS Status 2

Table 45-244c MultiGBASE-T1 PCS status 2 register bit definitions

Bits(s)	Name	Description	R/W[a]
3.2320.15:11	Reserved	Value always 0	RO
3.2320.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2320.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2320.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2320.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2320.6	Latched block lock	1 = PCS has not lost block lock 0 = PCS has lost block lock	RO/LL
3.2320.5:0	BER count	1 = Fault condition detected 0 = Fault condition not detected	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

What if we do OAM as in Sept?

Editor's Note (to be removed prior to Working Group ballot): Registers for OAM channel need to be added here once the group decides. Additionally, if registers read latching bits, a shadow register for reading those bits remotely is recommended. A model for the register to be read by the OAM channel is shown below.

45.2.u.v MultiGBASE-T1 PHY status register (Register x.yyyy)

The assignment of bits in the MultiGBASE-T1 PHY status register is shown in Table 45–zzz. All the bits in the MultiGBASE-T1 PHY status register are read only; a write to the MultiGBASE-T1 PHY status register shall have no effect.

Table 45-zzz MultiGBASE-T1 PHY status register bit definitions

Bits(s)	Name	Description	R/W[a]
x.yyyy.15:13	Alarm Status Word	15 14 13 1 1 1 All notifications false (no issues) 1 1 0 Transmission lines swapped 1 0 1 Reserved 1 0 0 Degraded link segment 0 1 1 No messages from MAC 0 1 0 PHY internal temperature warning 0 0 1 PHY power supply warning 0 0 0 Status Invalid	RO
x.yyyy.12:11	PMA SNR alarm	12 11 1 1 PHY SNR is good 1 0 PHY SNR is marginal 0 1 Request link partner exit EEE to improve SNR 0 0 PHY link is failing	RO
x.yyyy.10:0	Reserved	Value always 0	RO

Thank You!