Chiplet package study

IEEE 802.3 100 Gb/s Electrical Lane Study Group (.ck)

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Kandou Bus SA

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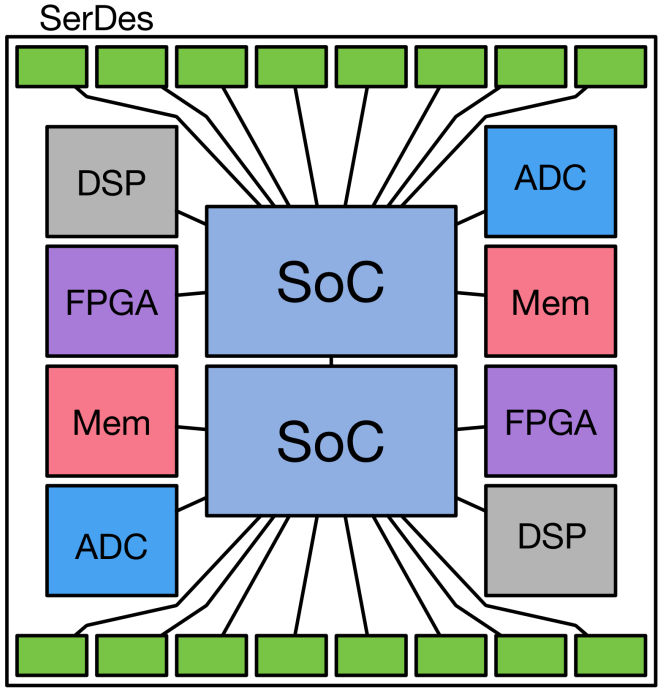
Chiplet Technology

- A trend in IC technology is to more away from monolithic chips toward the use of chiplets tied together on an MCM
- Chiplets allow the:
  - Combination of many dies into large packages
  - **Improvement in yield and cost** because of a smaller central die(s) – a major factor
  - Distribution of heat away from a single die
  - Use of the best semiconductor process for each die
  - Enabling of multi-vendor ecosystems
  - **I/O subsystem dies containing SerDes to be placed around the perimeter, creating smaller virtual packages**

Big, 70mm packages are routine



Non-interposer MCMs can easily use 20 or more dies plus passives

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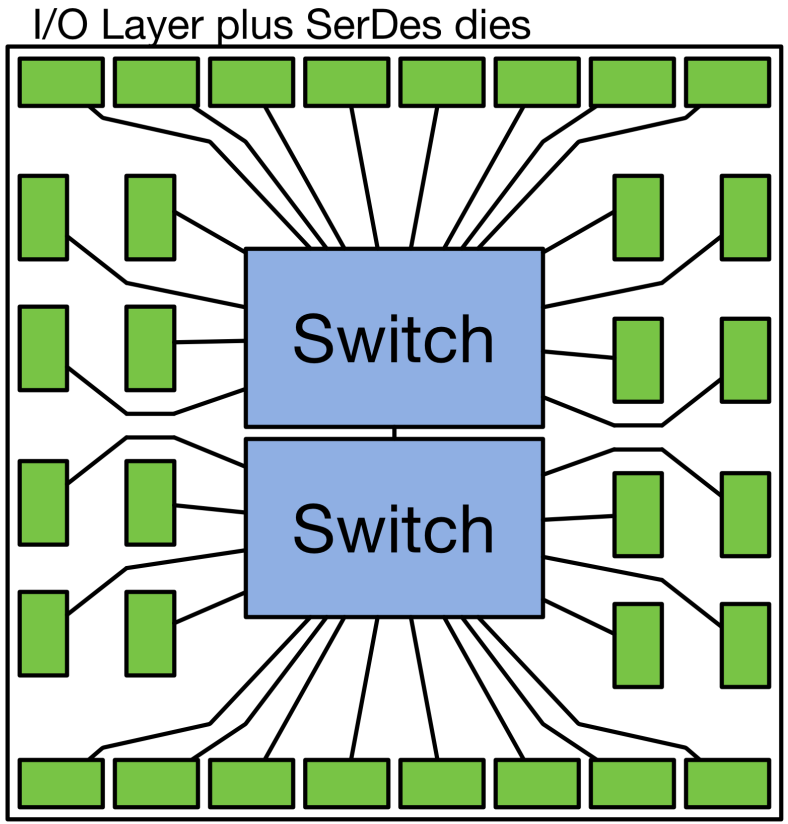
Chiplets in Switches

- The Ethernet I/O Subsystem including the SerDes can be put on a chiplet
  - Chiplet can have the PCS, FEC and long-reach SerDes and use a fat-pipe packet protocol between devices with a little speed-up factor
  - **Raises yield of switch device**
  - **Use of thin-pipe protocol (i.e. PCS/FEC on main chip) wastes this possible yield gain**
  - 1600 Gb/s is one useful chiplet size
  - Switch-to-chiplet link can use a Femto SerDes
    - A chord signaling Femto SerDes is one example
    - Femto SerDes can reach to the corners of a 70 mm package



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Fat-pipe link error control

- CNRZ-5 is ideal for the switch chip to the chiplet link
  - Fat-pipe packet link with some overspeed
  - Line protocol not yet applied, so not protected by link FEC
  - CNRZ-5 can use just a lightweight FEC
- PAM-4 has inferior native performance
  - The ISI-Ratio (largest eye/smallest eye) of PAM-4 = 3
  - This makes PAM-4 vulnerable to reflections and ISI
  - PAM-4 will need substantially more equalization and/or FEC coverage

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Detailed package study

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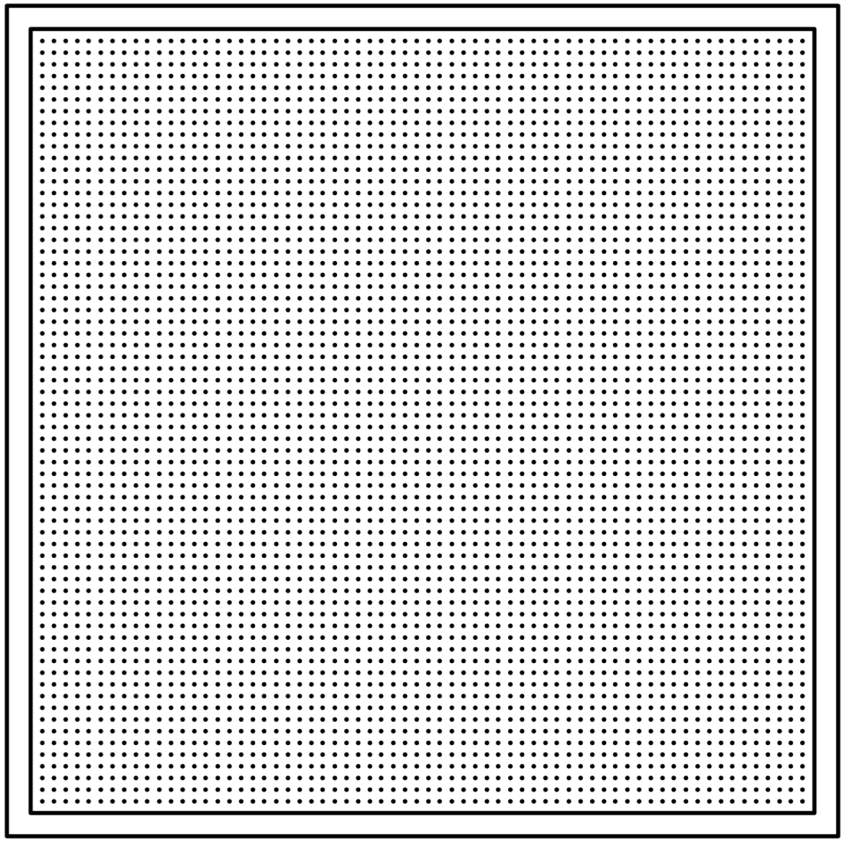
Package analyzed

- 70 mm BGA package analyzed
- 1 mm ball pitch
- 2.5 mm keep-out



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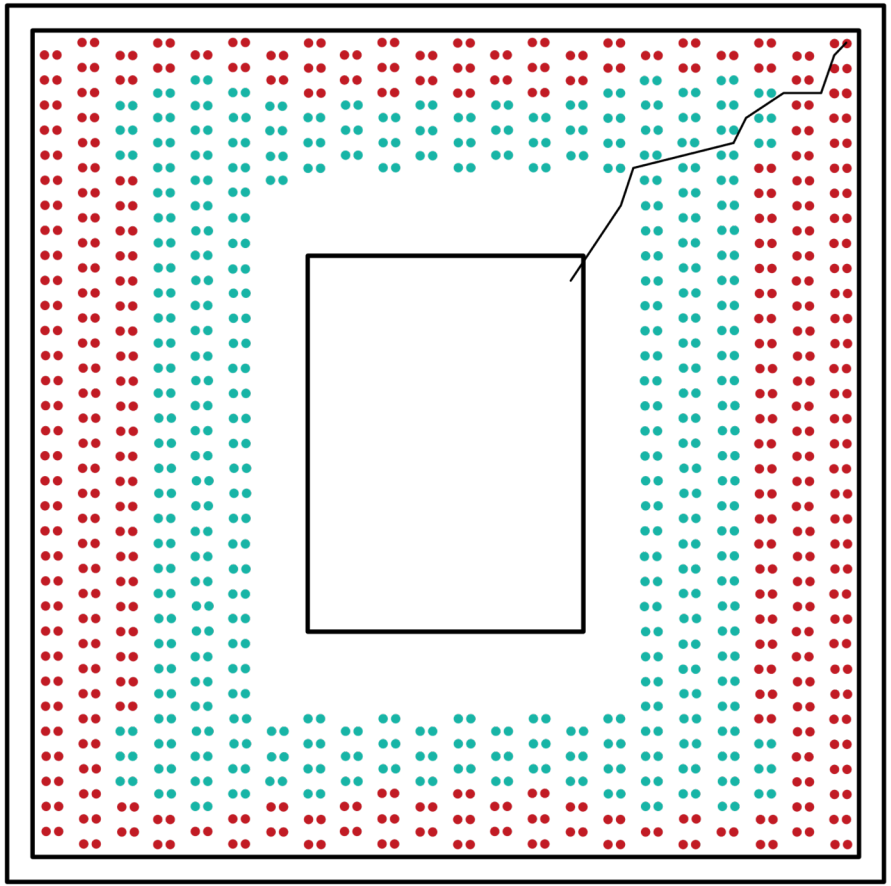
25.6 Tb/s Switch Chip analyzed

- 256 Tx and 256 Rx pairs
- Used 6-deep design rule for pairs

- Max trace length ~ 31mm



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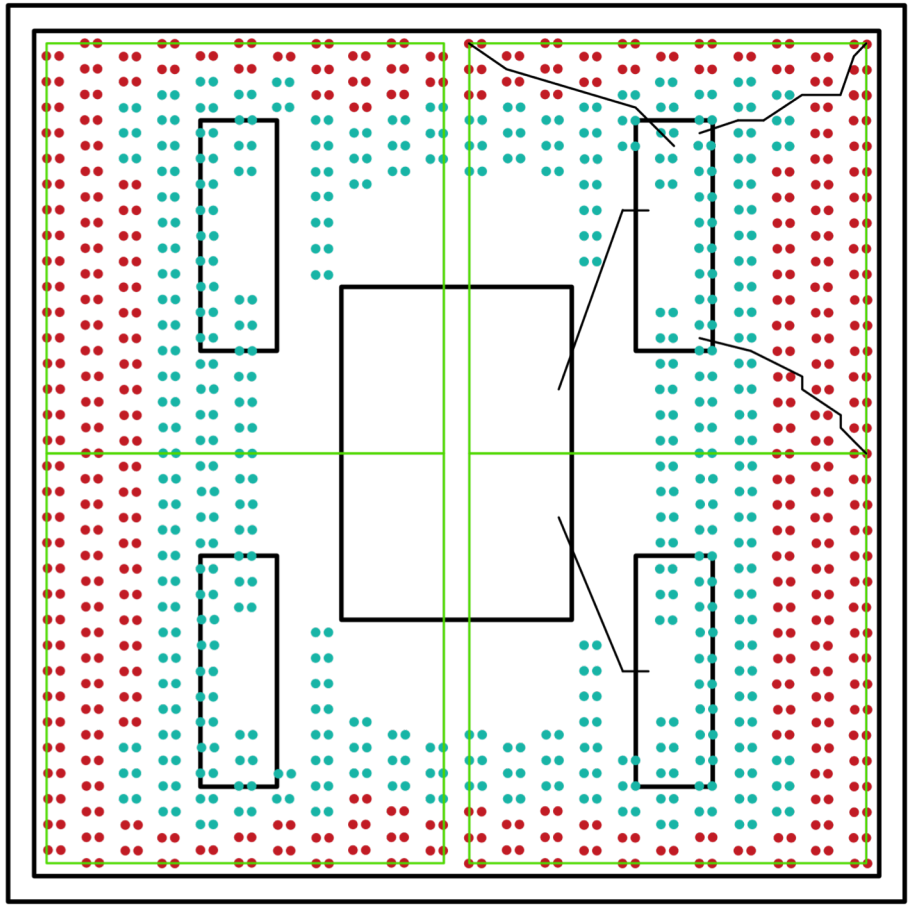
With 4 chiplets

- 256 Tx and 256 Rx pairs
- Max trace length ~ 21mm



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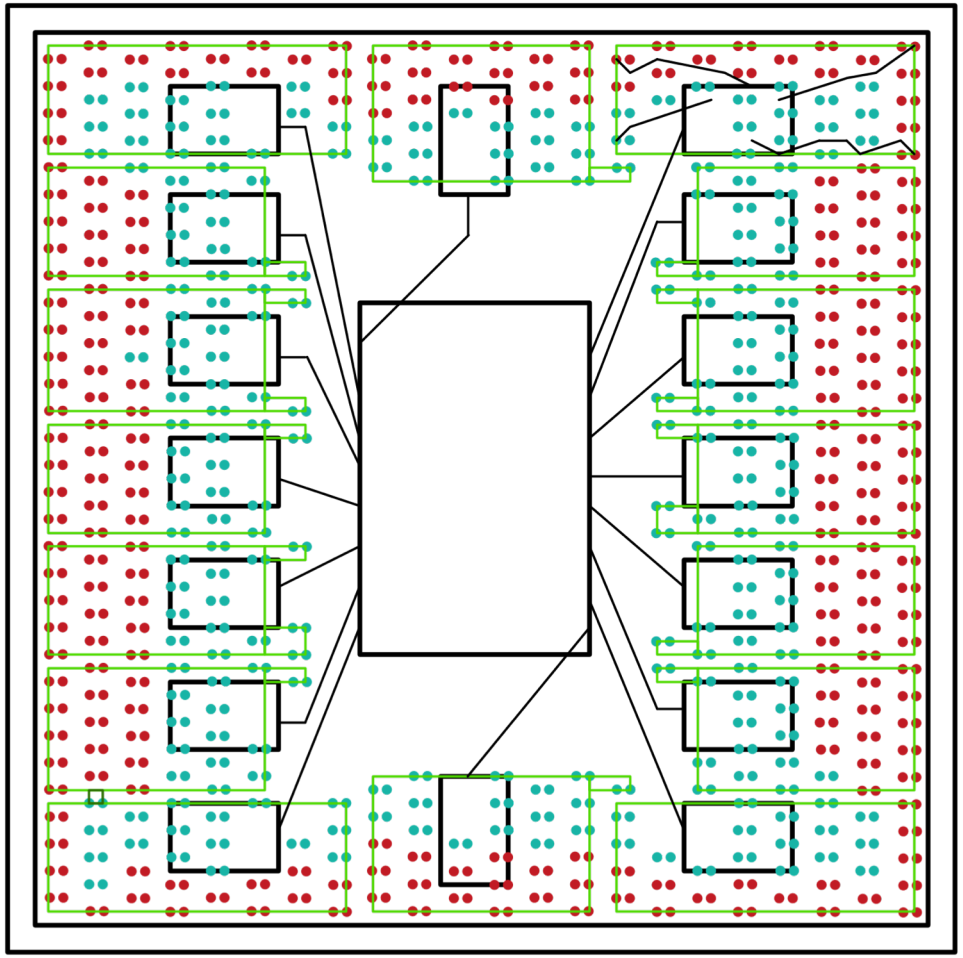
With 16 chiplets

- 234 Tx and 234 Rx pairs with this pinout
  - Can get to 256 with a different pinout
- Reserved space for chiplet power & CNRZ-5 traces
- Max trace length ~ 14mm



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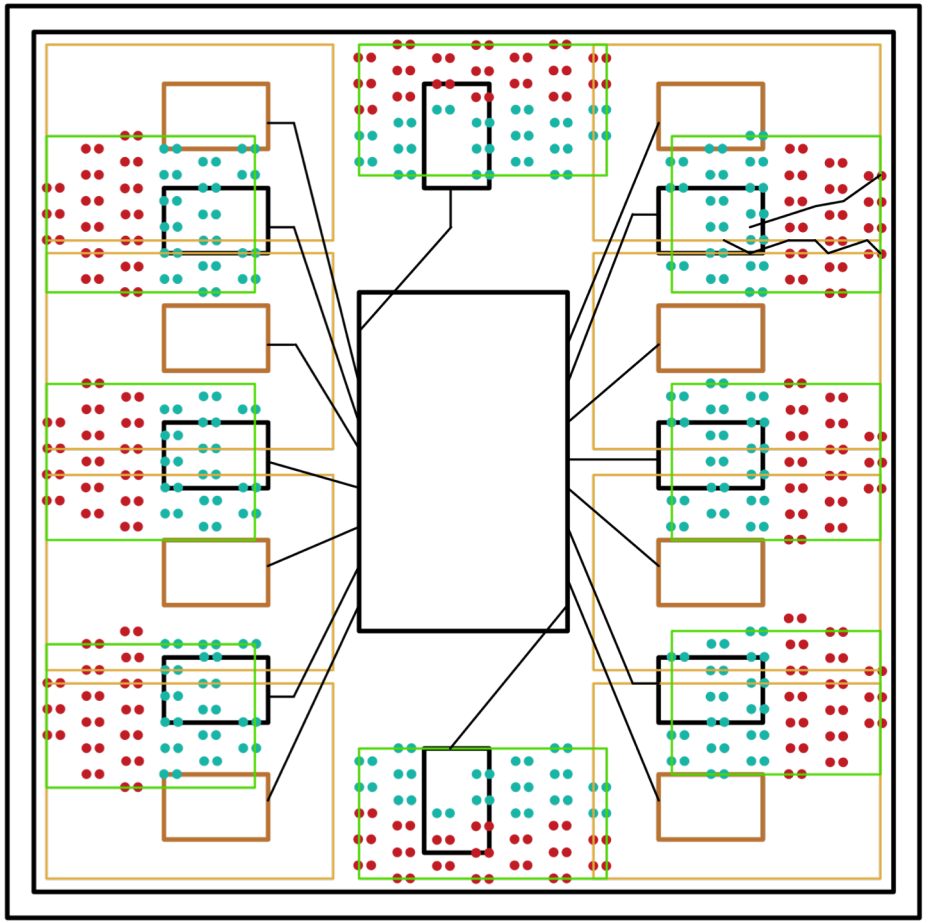
With 8 electrical & 8 EO chiplets

- 128 Tx and 128 Rx electrical pairs from the bottom
- 128 Tx and 128 Rx optics connections from EO chiplets plus optics from the top
- Max trace length ~ 12mm
  - Pads can be in a tighter cluster



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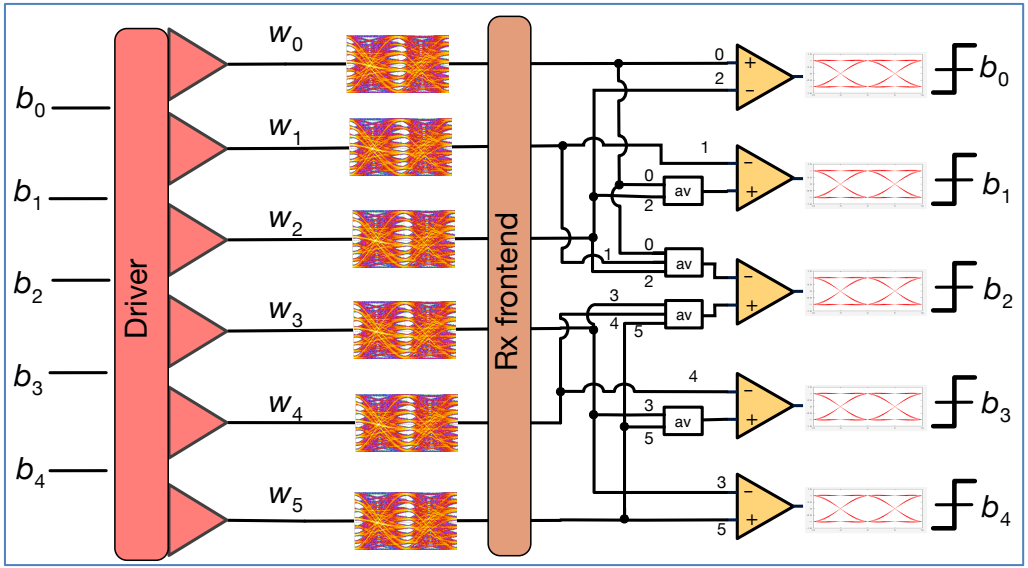
Example Femto SerDes technology
Chord signaling

CNRZ-5



Advantages:

- Ideal for shorter connections including die-to-die interconnect inside a package.
- Balanced values on wires reduce SSO Noise and EMI.
- Tolerates common mode noise similar to differential signals.
- Values at slicers are binary.
  - Similar to NRZ signaling
  - ISI Ratio = 1
- Comparators are self-referencing.

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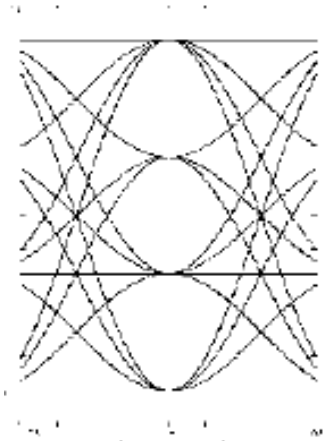
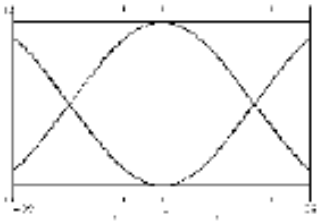
Key Advantage of CNRZ-5 over PAM-4: ISI Ratio

- Inter Symbol Interference Ratio (ISI Ratio):
  - Inherent property of any given code
  - A rough definition is that it is the code's ratio between the largest and smallest eyes at the decision point
- Energy from the larger eyes bleeds over and tends to close the smaller eyes
  - High ISI Ratio codes require more energy to be spent on ISI equalization
  - High ISI Ratio codes are more vulnerable to reflections



PAM-4's ISI Ratio = 3



CNRZ-5's ISI Ratio = 1

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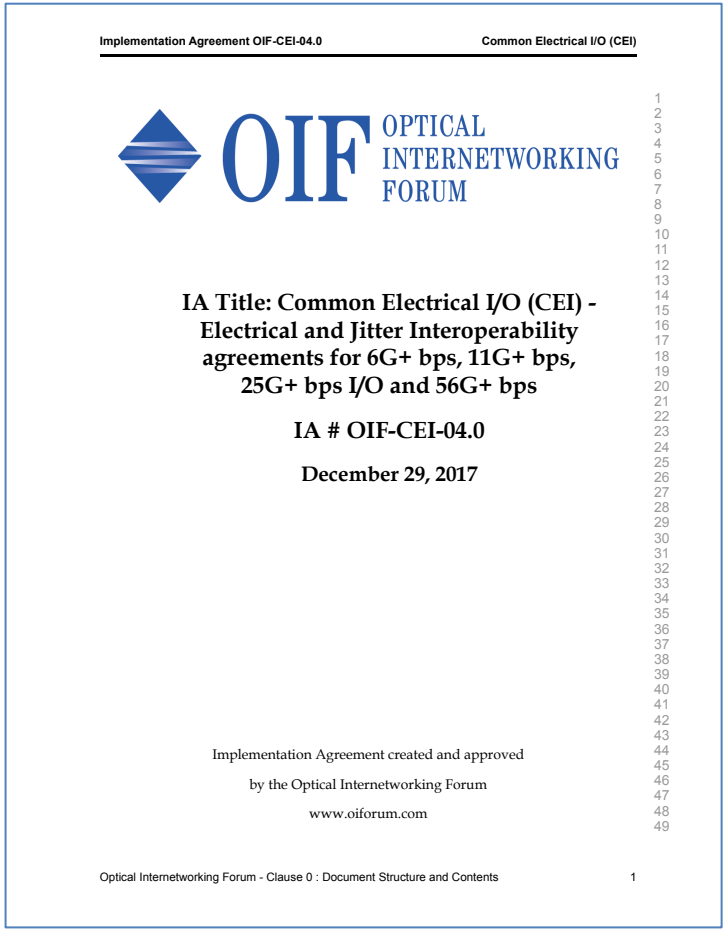
OIF & JEDEC

- OIF: ENRZ, CNRZ-5's cousin code, is a part of the OIF's published CEI 4.0 specification
  - Full Interoperability Agreement at 56 Gb/s equivalent throughput
- The OIF announced the CEI-112 in MCM project
  - Kandou has been active in this project
- JEDEC: Both ENRZ & CNRZ-5 published in JESD-247



Implementation Agreement OIF-CEI-04.0 Common Electrical I/O (CEI)

OIF OPTICAL INTERNETWORKING FORUM

IA Title: Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps I/O and 56G+ bps

IA # OIF-CEI-04.0

December 29, 2017

Implementation Agreement created and approved

by the Optical Internetworking Forum

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Optical Internetworking Forum - Clause 0 : Document Structure and Contents 1

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  - We are committed to adhering to the bylaws of all standards organizations to which we contribute and maintain membership including RAND licensing of our intellectual property.
  - We are committed to being good corporate citizens.

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Thank you!

QUESTIONS?

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