A possible receiver architecture and preliminary COM Analysis with 802.3 100GEL Channels

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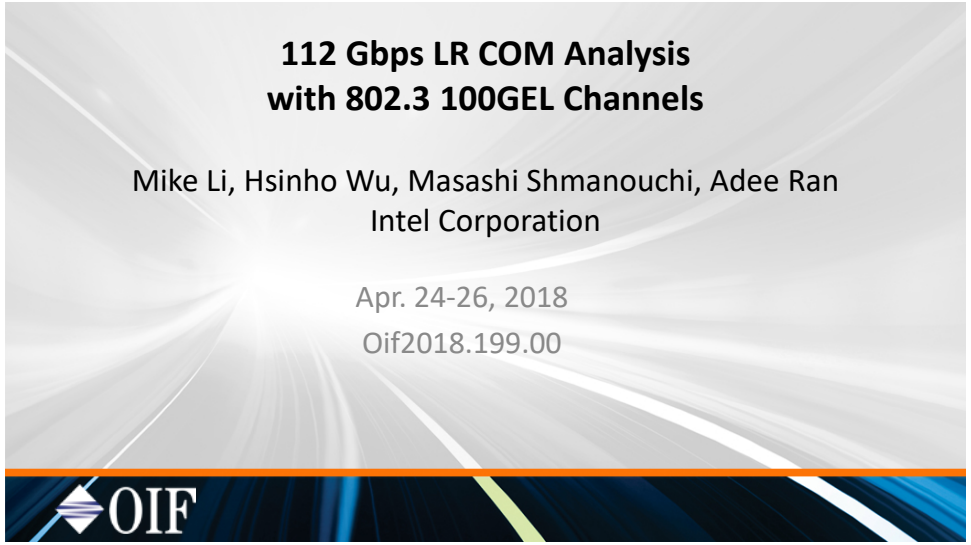
Agenda

- Possible receiver architecture for 100GEL
- Proposed 100GEL COM
- Package
- Die Capacitance Estimate
- 100GEL Test Channels
- COM Results
- Conclusions and Next Steps

Based on OIF presentation



Possible receiver architecture for 100GEL

- Assumed modulation: PAM4 at f_b=53.125 GBd
- Analog front end
  - High-frequency CTLE: $f_{p1}=f_z=0.4\times f_b$; $f_{p2}=f_b$; g_{DC} from -20 to 0 dB
  - Low-frequency CTLE: $f_{LF}=f_b/80$; g_{DC2} from -6 to 0 dB
- Digital receiver
  - Long FFE + short DFE
  - FFE Configuration
    - 3 pre- and 12-post cursor taps
    - Main tap: ≥0.7
    - Pre-cursor tap 1 coefficient: ≤ 0.3 (absolute)
    - Post-cursor tap 1 coefficient: ≤ 0.3 (absolute)
    - Other taps: ≤ 0.1 (absolute)
  - DFE Configuration
    - 1 post-cursor tap

CTLE poles are modified from 802.3cd and earlier; more suitable for digital Rx

Proposed 100GEL COM

Baseline

- 802.3cd COM
  - mellitz_080217_3cd_01_adhoc
  - mellitz_3cd_0817_COM.zip

Details and change highlights

- Device Package and termination models
  - Using Annex 93A TL model
  - Zc: 90 Ω
  - Trace length: max 30 mm
  - Cd: 130 fF
  - Cp: 110 fF
  - Rd: 50 Ω
- TX
  - Scale with UI: TX rise/fall time (T_r), jitter (A_{DD}, σ_{RJ})
  - Same: TX EQ (2 pre- + 1 post-cursor taps), R_{LM}, noise (SNR_{TX})
- RX
  - One-sided noise spectral density (η_0): 8.2e-9 V^2/GHz
  - 3 dB bandwidth (f_r): 0.75×f_b
- Rx Equalization
  - CTLE
    - f_p1=f_z=0.4×f_b; f_p2=f_b
    - F_HP_PZ: f_b/80
  - Digital Long FFE + short DFE architecture
    - New equalization and optimization algorithms
    - Tap configuration and limits: (see previous slide)

Proposed COM Spreadsheet (preliminary)

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	56	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.3e-4 1.3e-4]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[30]	mm	[test cases]
z_p (NEXT)	[30]	mm	[test cases]
z_p (FEXT)	[30]	mm	[test cases]
z_p (RX)	[30]	mm	[test cases]
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX] or selected
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.28:0.025:0]		[min:step:max]
c(-2)	[0:0.025:0.1]		[min:step:max]
c(1)	[-0.28:0.025:0]		[min:step:max]
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	22.4	GHz	
f_p1	22.4	GHz	
f_p2	56	GHz	
A_v	0.41	V	tdr selected
A_fe	0.41	V	tdr selected
A_ne	0.6	V	tdr selected
L	4		
M	32		
N_b	1	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
sigma_RJ	0.01	UI	
A_DD	0.02	UI	
eta_0	8.20E-09	V^2/GHz	
SNR_TX	32.5	dB	tdr selected
R_LM	0.95		
DER_0	1.00E-04		
Operational control			
COM Pass threshold	3	dB	
Include PCB	0	Value	0, 1, 2

g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.7	GHz	

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
Display frequency domain	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\D1p2_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	v165_d1p0a	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
IDEAL_TX_TERM	0	logical
T_r	0.006160714	ns
FORCE_TR	1	logical

RX FFE		
ffe_enable	1	logical
ffe_pre_tap_len	3	
ffe_post_tap_len	12	
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.3	
ffe_post_tap1_max	0.3	
ffe_tapn_max	0.1FFE	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	90	Ohm (tdr sel)

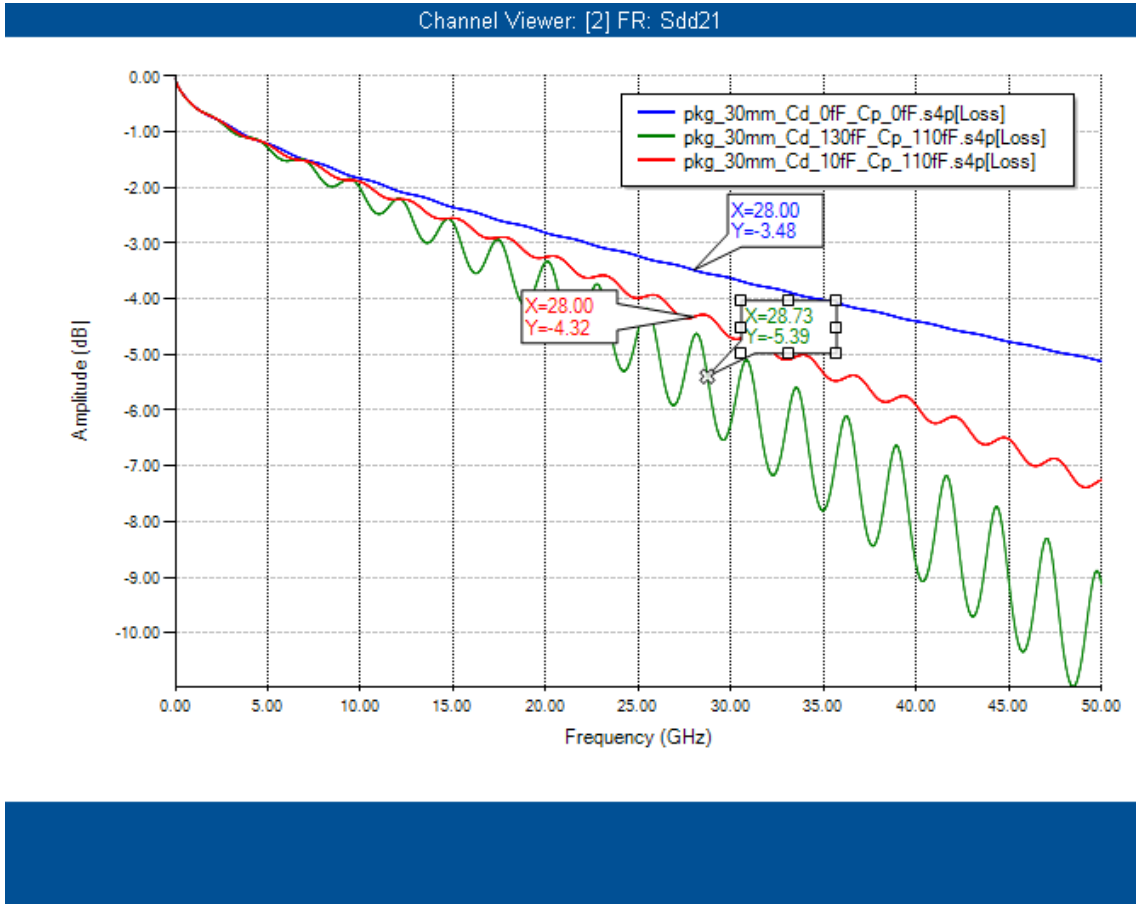
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	110	Ohm
z_bp (TX)	151	mm
z_bp (NEXT)	72	mm
z_bp (FEXT)	72	mm
z_bp (RX)	151	mm

Red: New or modified entries

Note: This sheet and results in the remainder of this presentation are from OIF, for **112 Gbps**

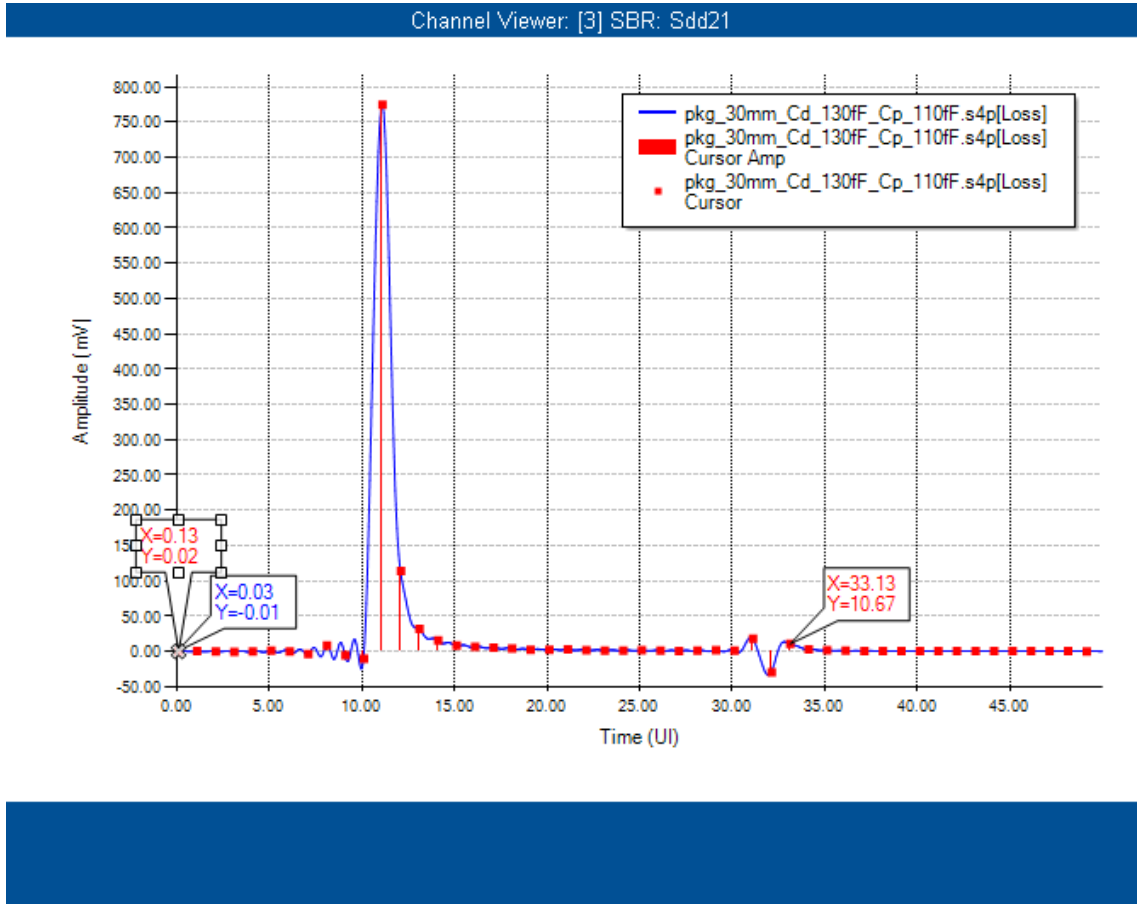
112Gbps Package Model

- Modified from 802.3cd COM package model
  - Length: 30mm
  - TL: No change
    - Zc: 90 ohms
  - Cd: 130 fF (Changed from 802.3cd)
  - Cp: 110 fF
  - Rd: 50 Ohms
- Insertion loss @ 28GHz
  - TL: ~3.5 dB
  - TL w/ 10% Cd + full Cp: ~4.3 dB
  - TL w/ full Cd + full Cp: ~5.4 dB

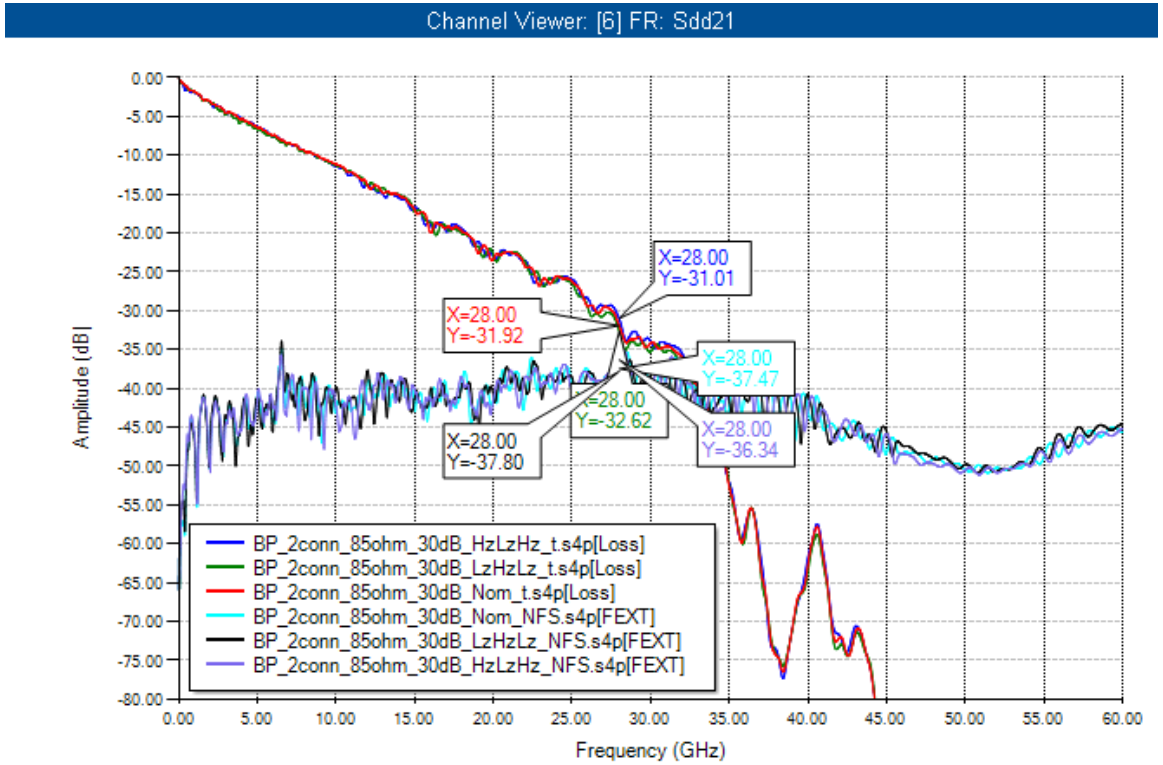


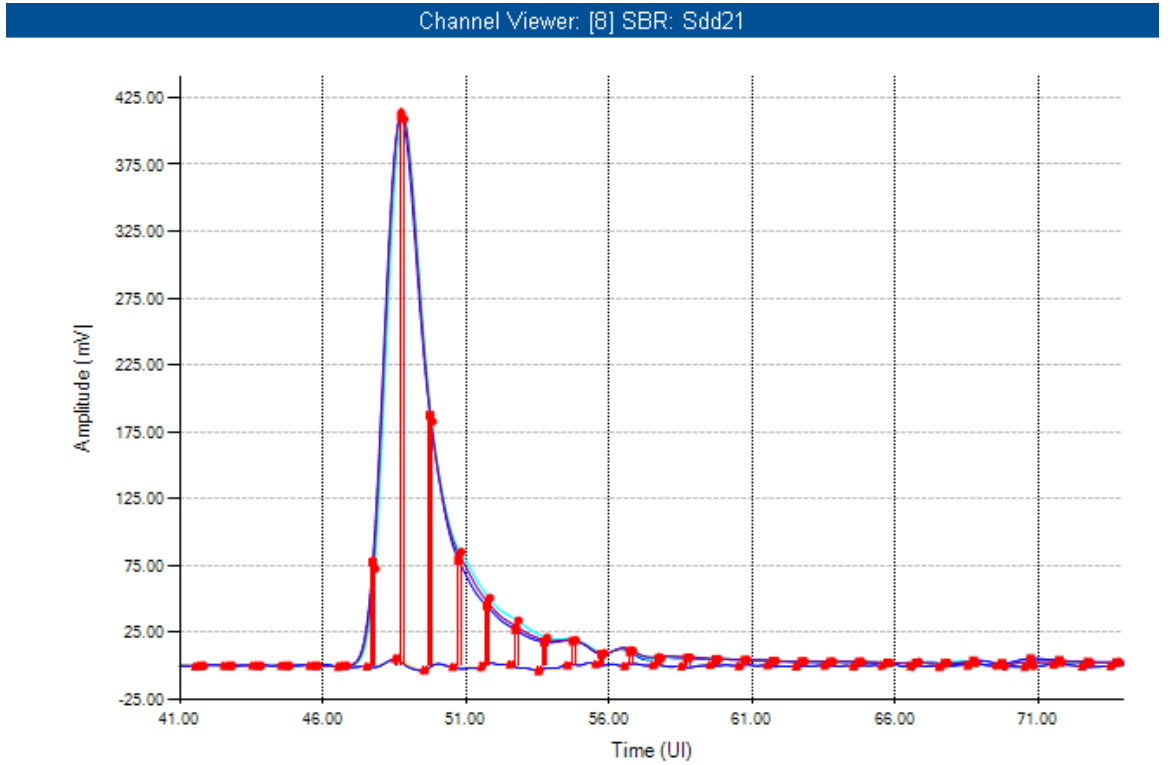
112Gbps Package Model (cont.)

- Potential ISI/EQ issue from the package
  - 30mm package has discontinuities at >20UI location (56Gbaud)
  - Indicate the need for >20 EQ taps



100GEL Test Channels – Intel

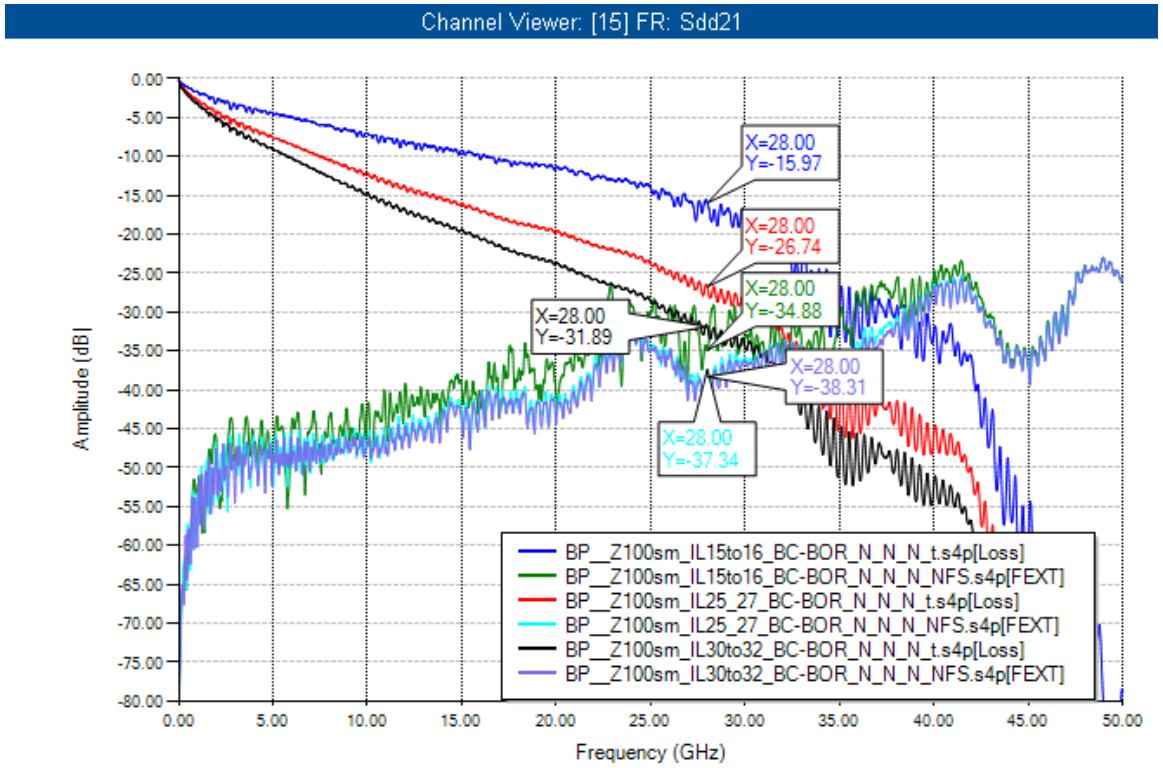


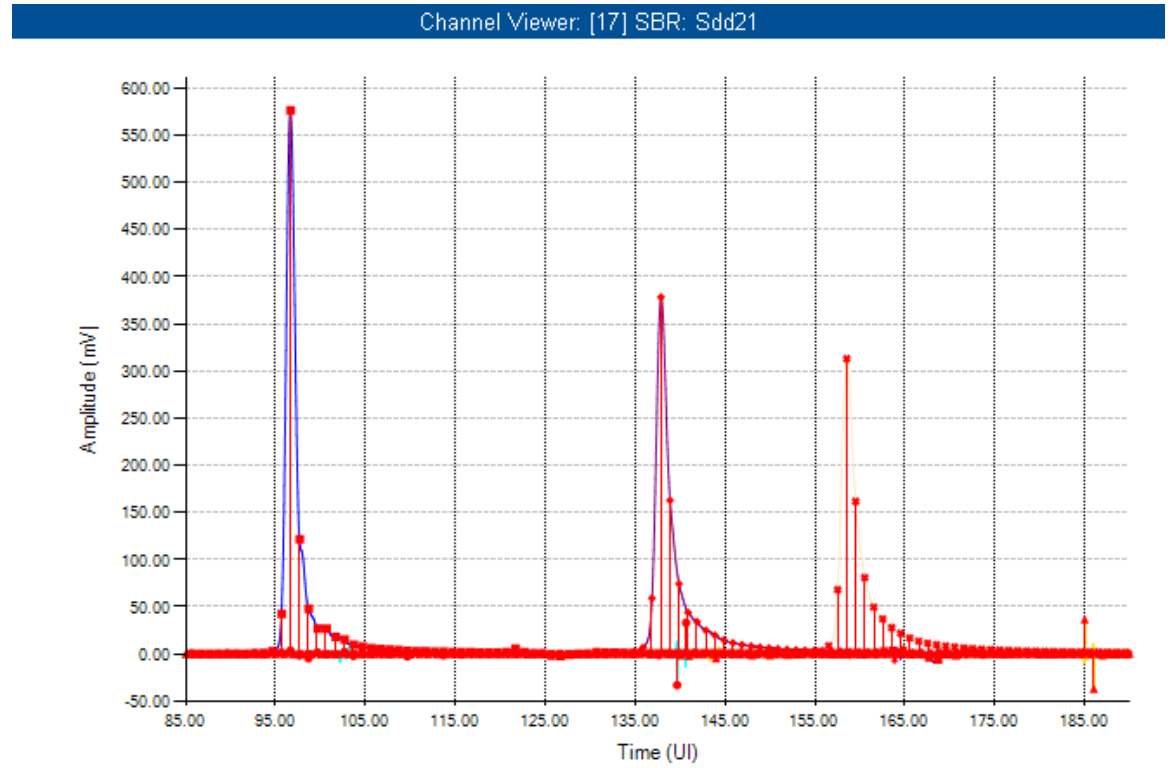


Channel	IL (dB)	ILD (dB)	RL (dB)	ICR (dB)	ICN* (mV-rms, NRZ)	ICN (mV-rms, PAM4)
BP_2conn_85ohm_30dB_Nom	31.92	-2.3/1.5	-6	5.56	4.95	3.69
BP_2conn_85ohm_30dB_HzLzHz	31.01	-1.5/1.7	-6	5.3	4.94	3.68
BP_2conn_85ohm_30dB_LzHzLz_f1	32.62	-2.2/1.4	-6	5.2	5.95	3.69

*Note: *: ICN is calculated using CEI 3.0 methodology with modulation scheme adjustment.*

100GEL Test Channels – Samtec BP

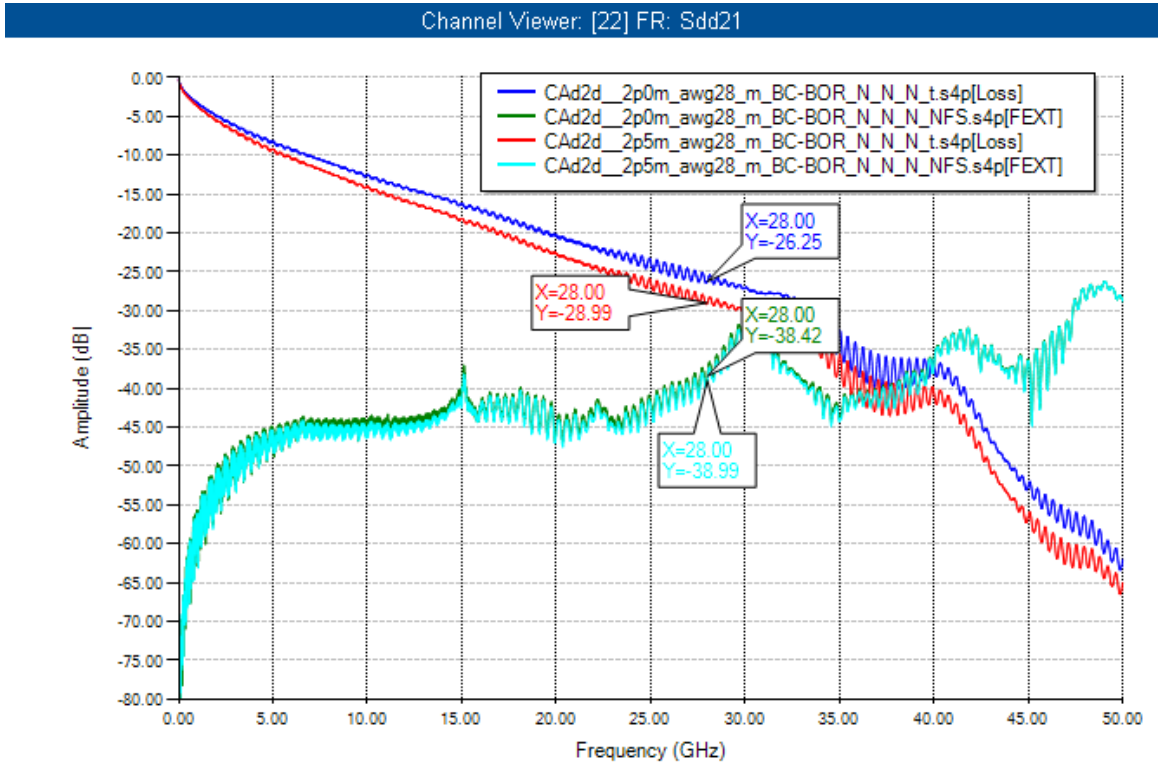


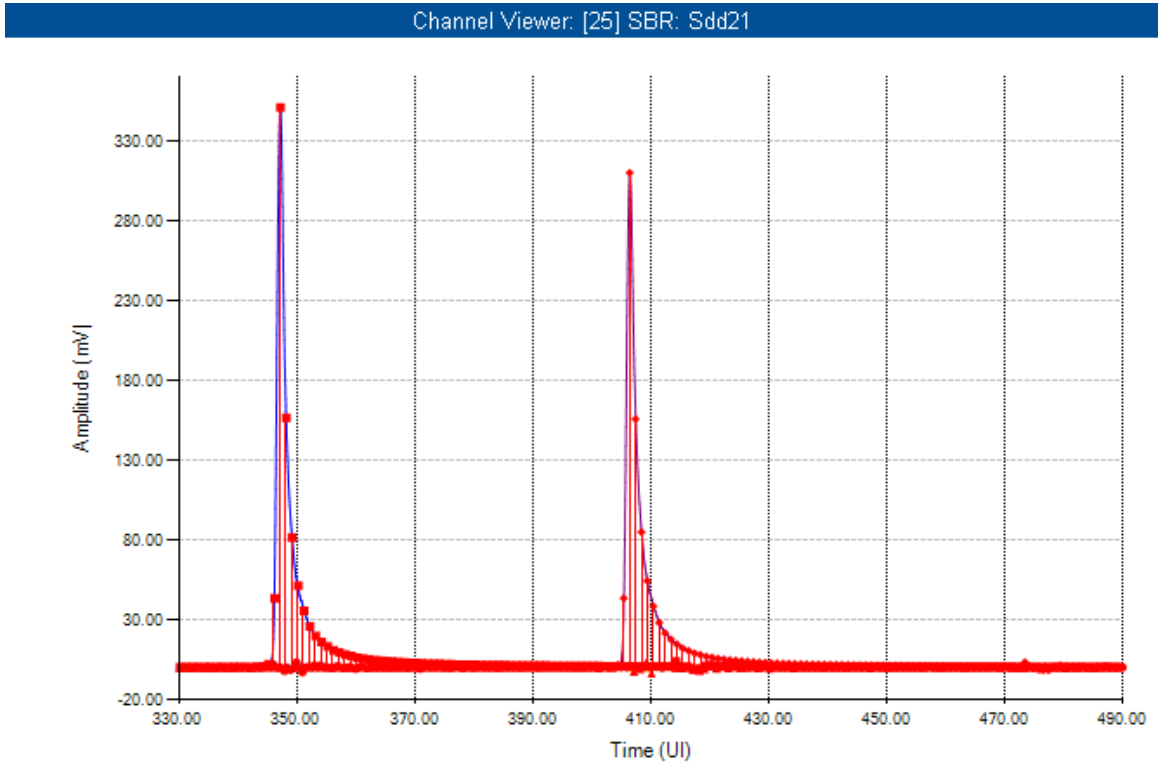


Channel	IL (dB)	ILD (dB)	RL (dB)	ICR (dB)	ICN* (mV-rms, NRZ)	ICN* (mV-rms, PAM4)
BP__Z100sm_IL15to16_BC-BOR_N_N_N	15.97	-3/0.6	-9	19	7.77	5.79
BP__Z100sm_IL25_27_BC-BOR_N_N_N	26.74	-2.2/0.6	-10	10	5.13	3.82
BP__Z100sm_IL30_32_BC-BOR_N_N_N	31.89	-1.9/0.6	-10	4.83	4.84	3.60

*Note: *: ICN is calculated using CEI 3.0 methodology with modulation scheme adjustment.*

100GEL Test Channels – Samtec CR Cable

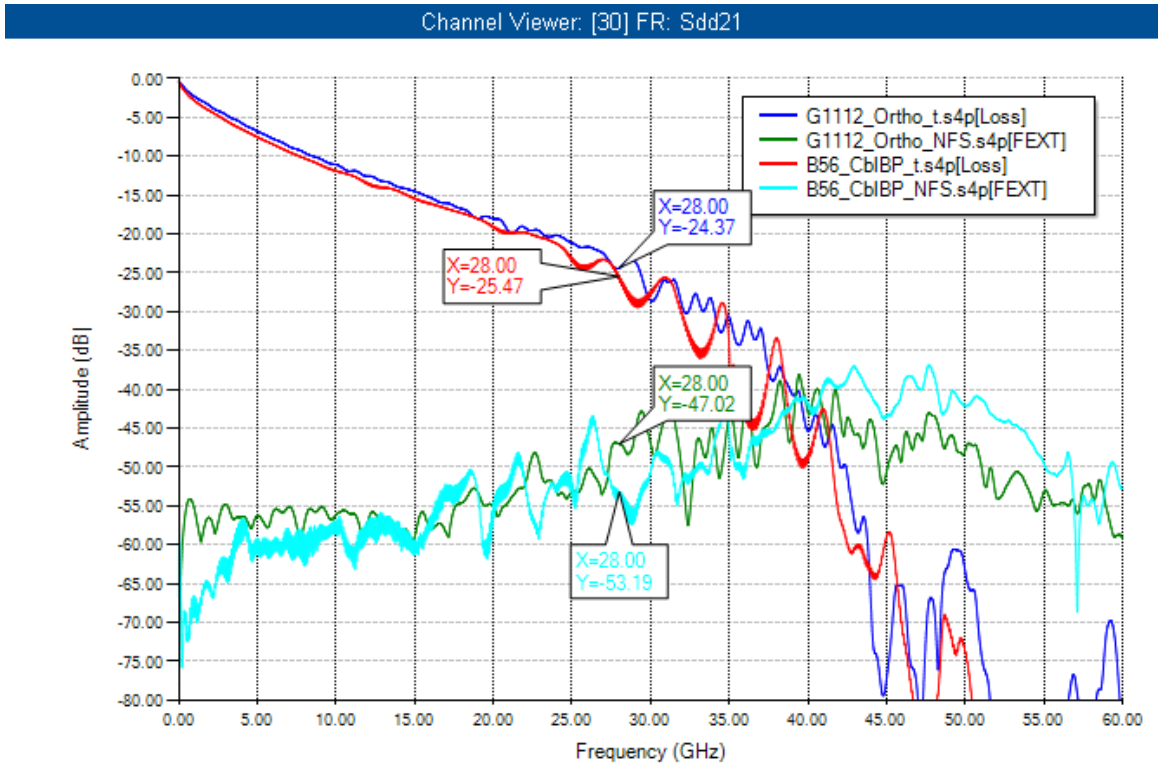


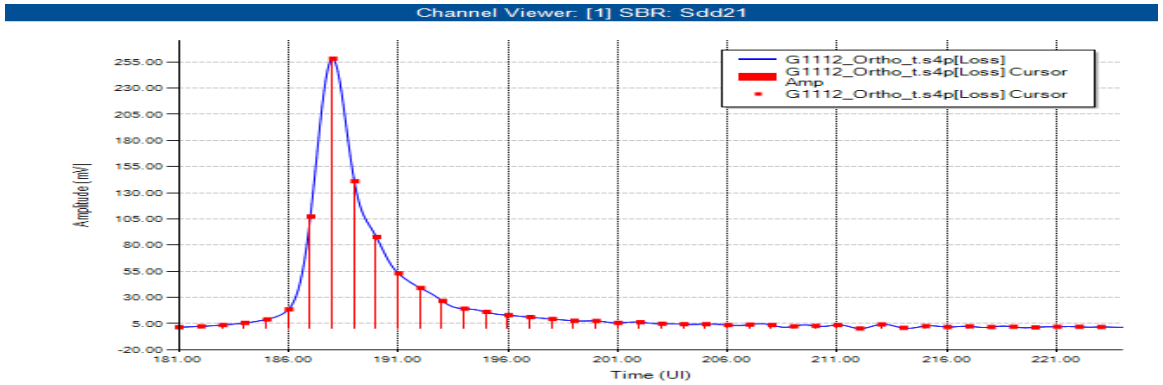


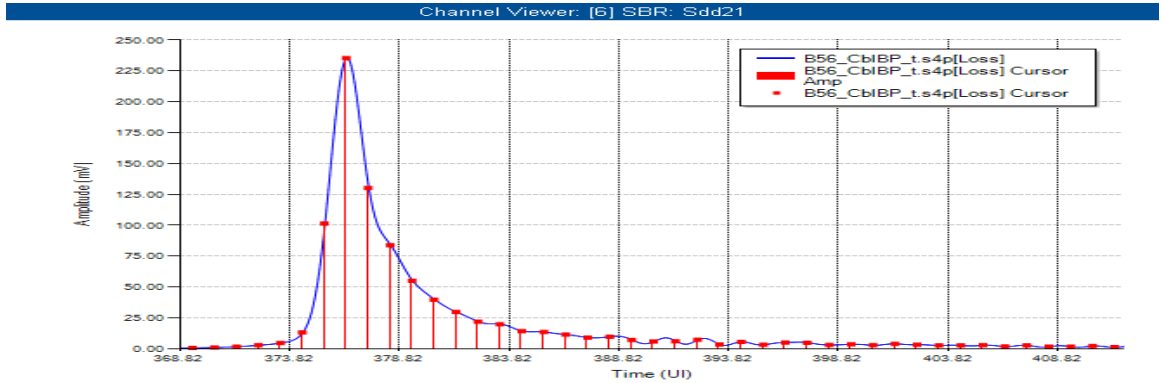
Channel	IL (dB)	ILD (dB)	RL (dB)	ICR (dB)	ICN* (mV-rms, NRZ)	ICN (mV-rms, PAM4)
CAd2d__2p0m_awg28_m_BC-BOR_N_N_N	26.25	-0.9/0.9	-11	12	4.12	3.07
CAd2d__2p5m_awg28_m_BC-BOR_N_N_N	28.99	-0.75/0.9	-12	10	3.87	2.88

*Note: *: ICN is calculated using CEI 3.0 methodology with modulation scheme adjustment..*

100GEL Test Channels – TE BP







Channel	IL (dB)	ILD (dB)	RL (dB)	ICR (dB)	ICN* (mV-rms, NRZ)	ICN (mV-rms, PAM4)
G1112_Thru_Ortho	24.37	0.7/-1	-22	22	1.25	0.93
B56_Thru_CblBP	25.47	-2.1/0.5	-18	19	1.09	0.82

*Note: *: ICN NRZ is calculated using CEI 3.0 methodology with modulation scheme adjustment.*

100GEL Test Channel COM Results w/o Crosstalk

Vendor	Channel w/o XTLK	FFE Tap Length				
		16	20	24	28	32
Intel	BP_2conn_85ohm_30dB_Nom_t	-0.95	-0.56	0.63	1.14	1.23
Intel	BP_2conn_85ohm_30dB_HzLzHz_t	-1.3	-0.72	0.31	1.01	1.2
Intel	BP_2conn_85ohm_30dB_LzHzLz_t	-0.56	-0.05	1.04	1.58	1.63
Samtec	BP__Z100sm_IL15to16_BC-BOR_N_N_N_t	0.62	0.77	1.27	3.86	4.14
Sametc	BP__Z100sm_IL25_27_BC-BOR_N_N_N_t	0.6	0.87	1.34	2.89	3.09
Sametc	BP__Z100sm_IL30to32_BC-BOR_N_N_N_t	-1.03	-0.8	0.18	0.88	1.11
Samtec	CAd2d__2p0m_awg28_m_BC-BOR_N_N_N_t	0.93	1.02	1.84	3.12	3.27
Samtec	CAd2d__2p5m_awg28_m_BC-BOR_N_N_N_t	0.41	0.5	1.32	2.43	2.5
TE	G1112_Ortho_t	1.68	1.74	2.72	5.15	5.13
TE	B56_CblBP_t	2.56	2.97	4.01	5.08	5.08

- Small solution space when 12~20 post-cursor FFE/DFE taps
- Passing channels generally have IL < 28dB @ 28GHz

Note: FFE is with 3 pre-cursor taps. DFE tap length is 1.

100GEL Test Channel COM Results w/ Crosstalk

Vendor	Channel w/ XTLK	FFE Tap Length				
		16	20	24	28	32
Intel	BP_2conn_85ohm_30dB_Nom_t	-1.91	-1.57	-0.45	-0.05	0.03
Intel	BP_2conn_85ohm_30dB_HzLzHz_t	-2.25	-1.7	-0.75	-0.2	-0.05
Intel	BP_2conn_85ohm_30dB_LzHzLz_t	-1.54	-1.05	-0.06	0.35	0.41
Samtec	BP__Z100sm_IL15to16_BC-BOR_N_N_N_t	-0.08	0.07	0.57	2.94	3.15
Samtec	BP__Z100sm_IL25_27_BC-BOR_N_N_N_t	-0.85	-0.6	0.07	1.19	1.39
Samtec	BP__Z100sm_IL30to32_BC-BOR_N_N_N_t	-2.77	-2.29	-1.89	-0.84	-0.76
Samtec	CAd2d__2p0m_awg28_m_BC-BOR_N_N_N_t	0.47	0.49	0.8	2.63	2.07
Samtec	CAd2d__2p5m_awg28_m_BC-BOR_N_N_N_t	-0.76	-0.68	0.12	1.07	1.12
TE	G1112_Ortho_t	1.6	1.66	2.65	5.04	5.02
TE	B56_CblBP_t	2.48	2.89	3.92	4.96	4.96

- Solution space reduces as Intel and Samtec channels are with substantial amount of crosstalk

Note: FFE is with 3 pre-cursor taps. DFE tap length is 1.

Summary

- Progresses so far
  - Added RX FFE support and FFE/DFE co-adaptation in COM
  - Updated COM package model
  - Updated COM parameters
  - Evaluated latest 100GEL channels

Summary (cont.)

Observations and implications

- To accommodate the reflection caused by the 30mm reference package (whose transmission line (TL) model is based on 802.3cd) and 112G 100GEL channels, FFE/DFE post tap length of ~24 is needed, which is serious power concern.
  - What are the plausible paths to overcome this gap w/o long FFE/DFE post taps (>= 24) and overburden the SERDES power?
    - A: Shorten package length 30 mm to smaller values (e.g., 25 mm)
    - B: Improve the package medium propagation speed (i.e., better dielectric constant materials)
    - C: Improve the package loss
    - D: Combination of A&B&C
- Large crosstalk in Intel and Samtec channels lower the link performance, and reducing them would enable larger solution space

Summary (cont.)

Next Steps

- Continue investigation on 112Gbps package
  - Explore 112Gbps COM ref package model improvement that is aligned with technology advancement pace
- Other COM improvements
  - CTLE modeling methodology
    - Determine the maximum CTLE bandwidth supported by today's technology
  - RX FFE/DFE optimization methods
  - ERL for 112G

THANK YOU