Test Results for “Balanced SERDES Architecture”

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Introduction

- 100G single lane SERDES complexity and power has been a concern based on channel simulation results and FEC choices.

- sun_100GEL_01b_0118 proposed “Balanced Architecture” for SERDES to reduce power by about 30%.

- This contribution is to report preliminary test results, help understand TX Equalization, and provide reference data for SERDES architecture considerations.

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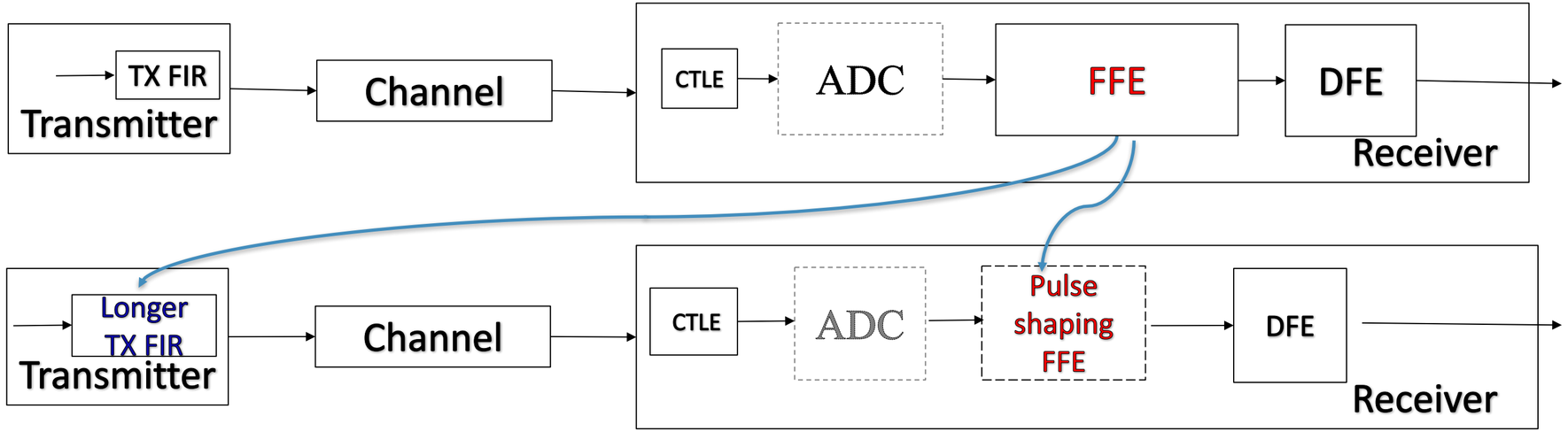
What is “Balanced SERDES Architecture”?

- “Balanced SERDES Architecture” proposes to move most of FFE to TX
  - Balanced EQ
- As TX FIR is much lower cost than its counter part on RX side
  - SERDES complexity and power is significantly reduced
  - As a result, RX front end nonlinearity is also improved



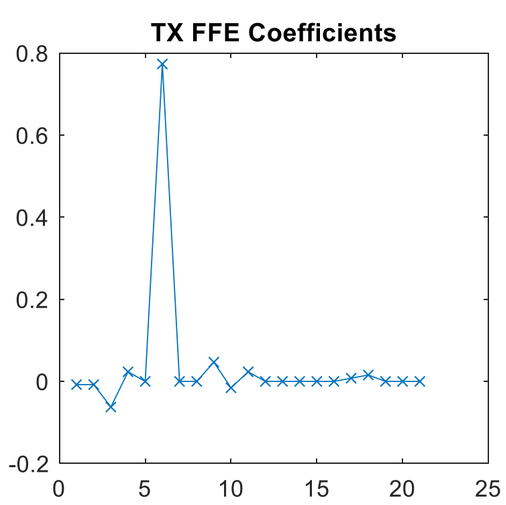
Conventional SERDES Architecture

FFE taps for ISI cancellation are moved to TX

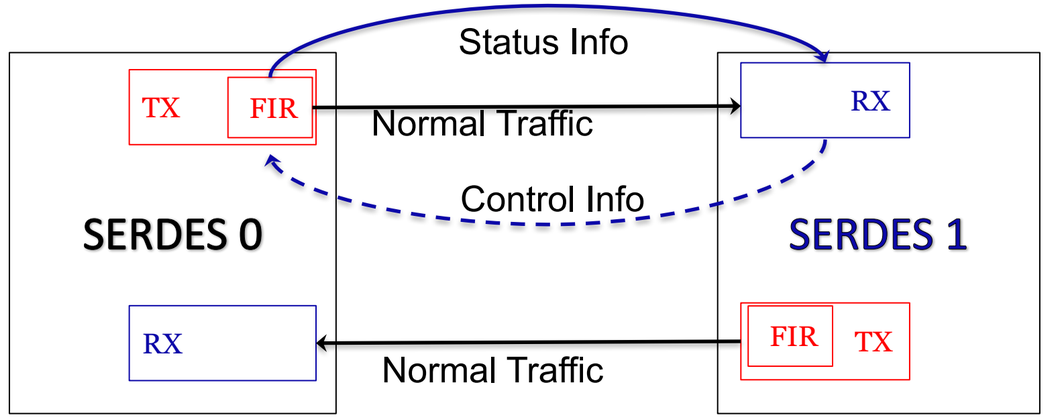
A Low-power SERDES Architecture with simpler RX

How Balanced EQ works?

- TX FIR is used to cancel reflections
- Channel material loss is equalized by RX.
- Linkup training interface is close to 50G SERDES, but with more TX FIR taps.
- A “back channel” is proposed for real-time adaptation.

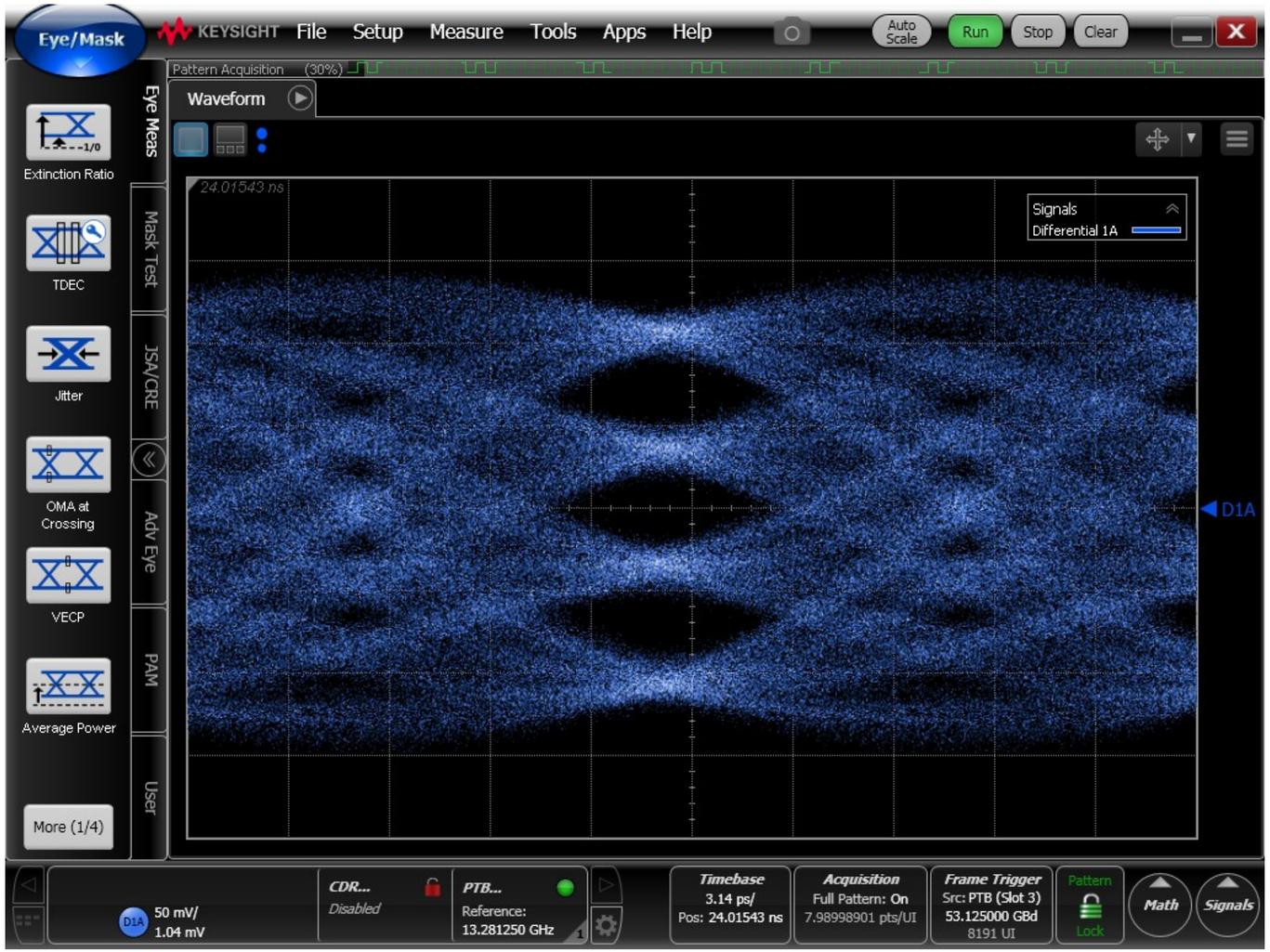


An example of TX FIR Coefficients



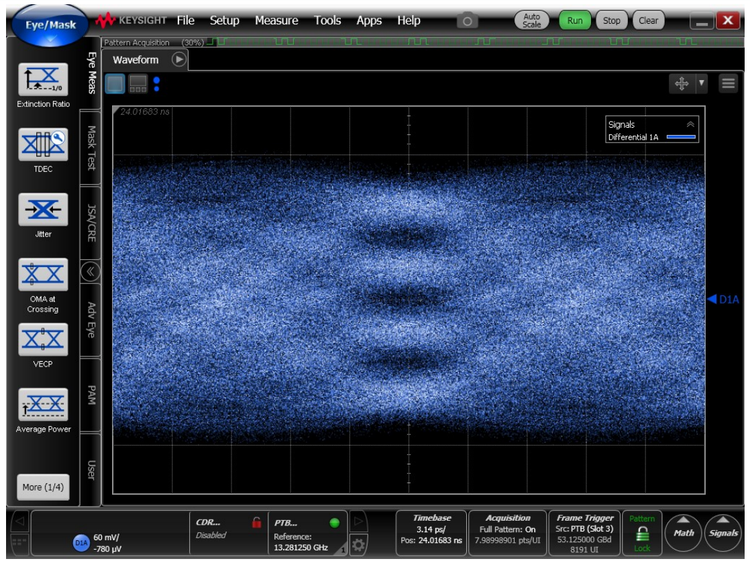
Block Diagram for Real-time Adaptation

100G PAM4 Eye at the Channel output

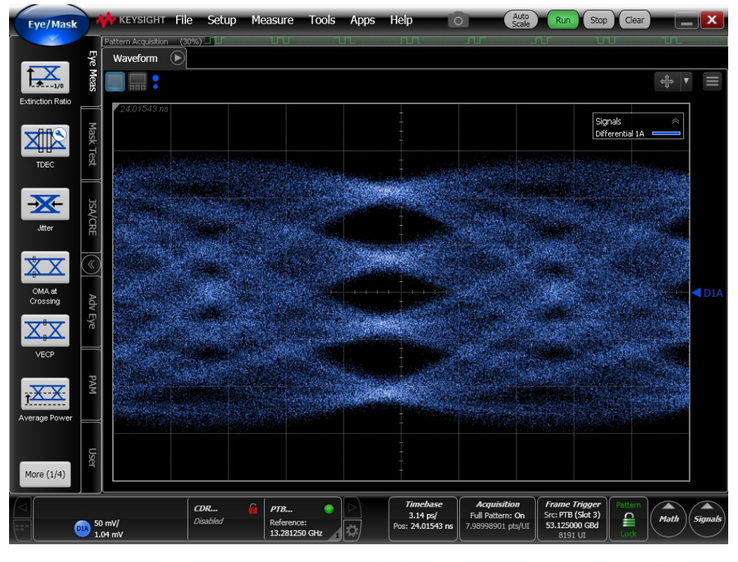


Eye after 13.2dB Ball to Ball Channel

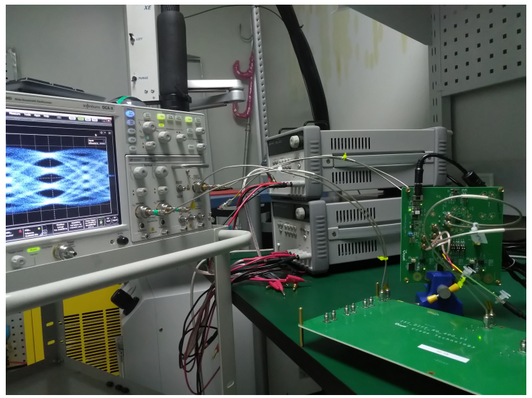
100G PAM4 Setup and Test Results



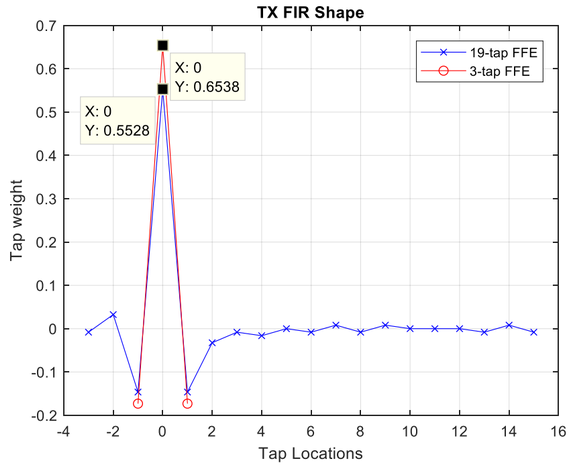
Eye after 3 Tap TX FFE



Eye after 19 Tap TX FFE



Total channel loss is 13.2dB (Ball-to-Ball)



TX FIR Shape

- Taps [-1 0 1 2] has 88% weight of TX FFE.
- Note, tail taps are very small and some are zeros.

Conclusions

- TX FIR effectively cancels reflections.
- “Balanced SERDES Architecture” is an option to keep SERDES power under envelope, for both long and short reach.

Thanks!