100GEL C2M Channel Reach Update

Jane Lim, Cisco

Pirooz Tooyserkani, Cisco

Upen Reddy Kareti, Cisco

Joel Goergen, Cisco

Marco Mazzini, Cisco

7/11/2018

List of Supporters

- Gary Nicholl, Cisco
- Mark Nowell, Cisco
- Matt Traverso, Cisco
- David Chen, AOI
- Kohichi Tamura, Oclaro
- Rajesh Radhamoha, Maxlinear
- Phil Sun, Credo
- Jeff Twombly, Credo
- Geoff Zhang, Xilinx
- Jan Filip, Maxim
- Ali Ghiasi, Ghiasi Quantum LLC
- Takeshi Nishimura, Yamaichi
- Thananya Baldwin, Keysight
- Sudeep Bhoja, Inphi
- Karthik Gopalakrishnan, Inphi
- Nathan Tracy, TE
- Chris DiMinico, MC Communications/PHY-SI LLC

100GEL C2M & CR Link Budget Original Proposal - in Rosemont meeting

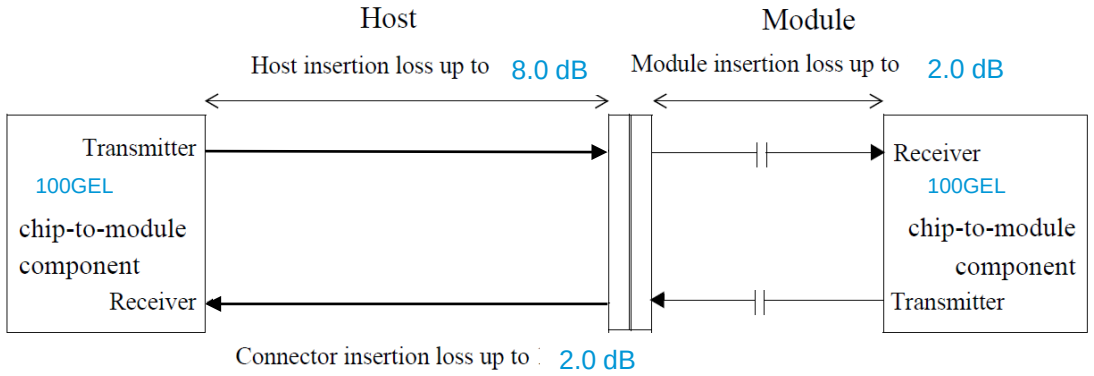


Figure 1: 100GEL C2M insertion loss budget at 26.56 GHz

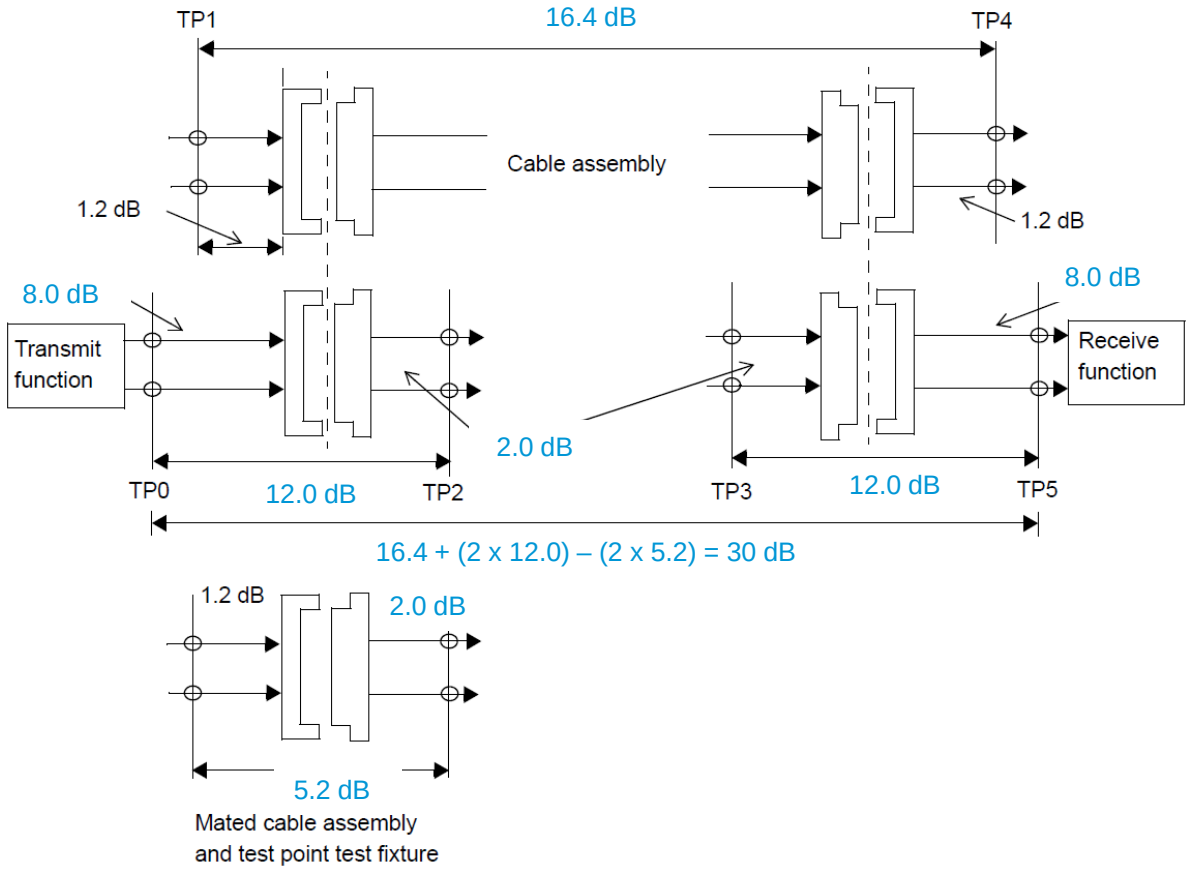


Figure 2: 100GEL CR 30dB insertion loss budget at 26.56 GHz

100GEL C2M & 100GEL CR Link Budget Adjusted Proposal - in Pittsburgh meeting

- Tighten host PCB budget, from 8.0 dB to 7.5dB
- Tighten connector only loss, from 2.0 dB to 1.5 dB
- Loosen Module PCB or HCB loss, from 2.0dB to 2.5dB

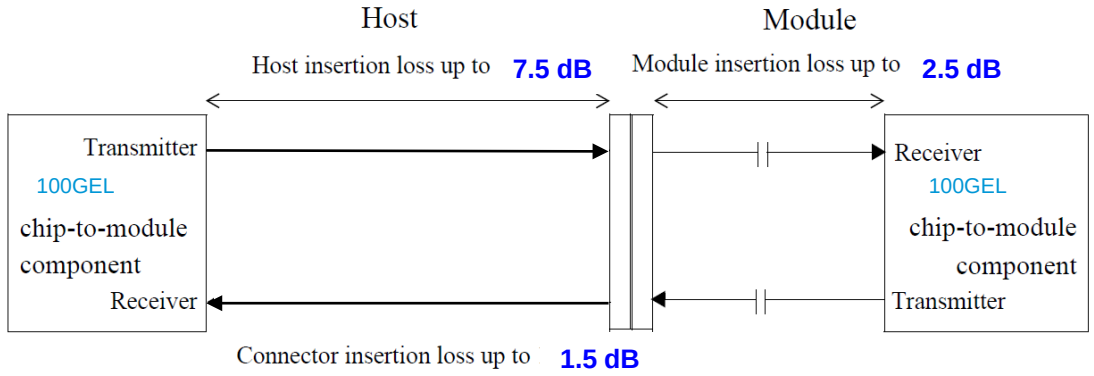


Figure 1: 100GEL C2M **11.5dB** insertion loss budget at 26.56 GHz

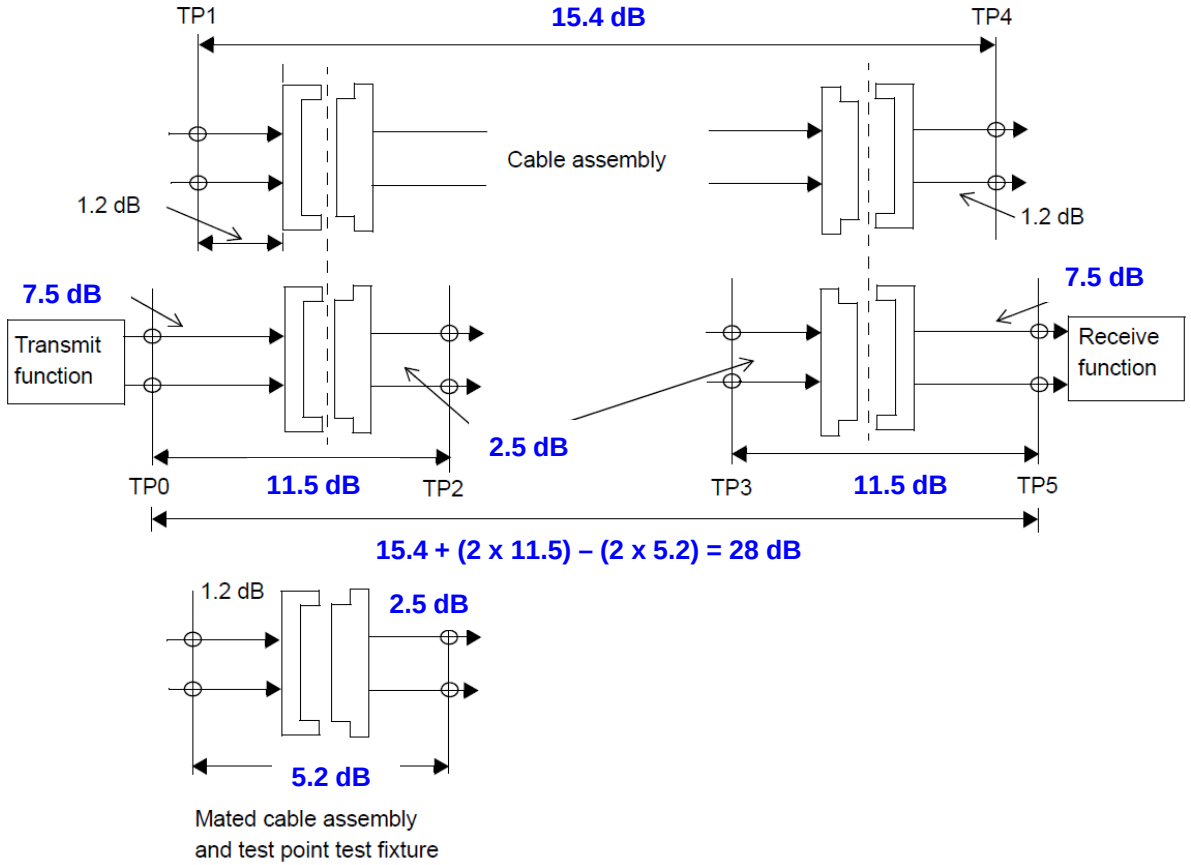


Figure 2: 100GEL CR **28dB** insertion loss budget at 26.56 GHz

C2M Channel Reach Update

- 1.5dB is not sufficient to account for I/O connector based on supplier feedback, would like to go back to 2.0dB
- Module PCB loss would be 2.5dB not 2.0dB
- To stay within host PCB channel budget (7dB), is getting too tight for system board design
- Increasing C2M reach (TP0-TP1a) upto 16dB offers a choice for system designers to optimize the non-DAC case (see slide 7)
  - Allow longer host PCB trace for Optics (upto 8”), much fewer retimers or intra-box cables are required
- However, SR serdes requires more complex Rx design (in terms of # of FFE taps) in module CDR to achieve reasonable BER (see slide 9)
  - Serdes power penalty? How much?
  - Can CDR stay within module power envelope?

100GEL C2M TP0-TP1a & Cu MDI TP0-TP2 Updated Proposal

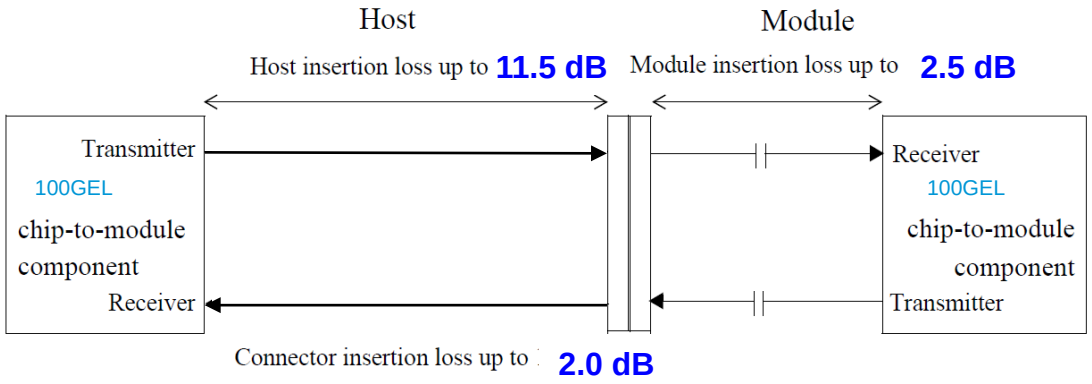


Figure 1: 100GEL C2M **TP0-TP1a** insertion loss budget at 26.56 GHz

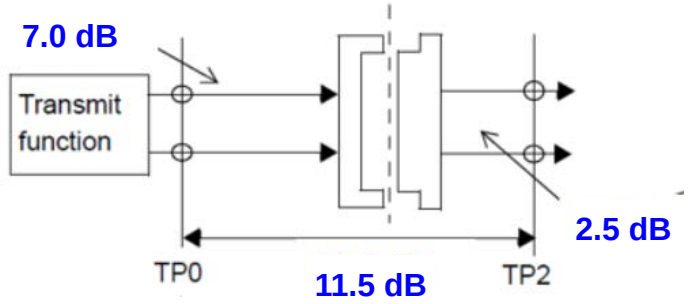
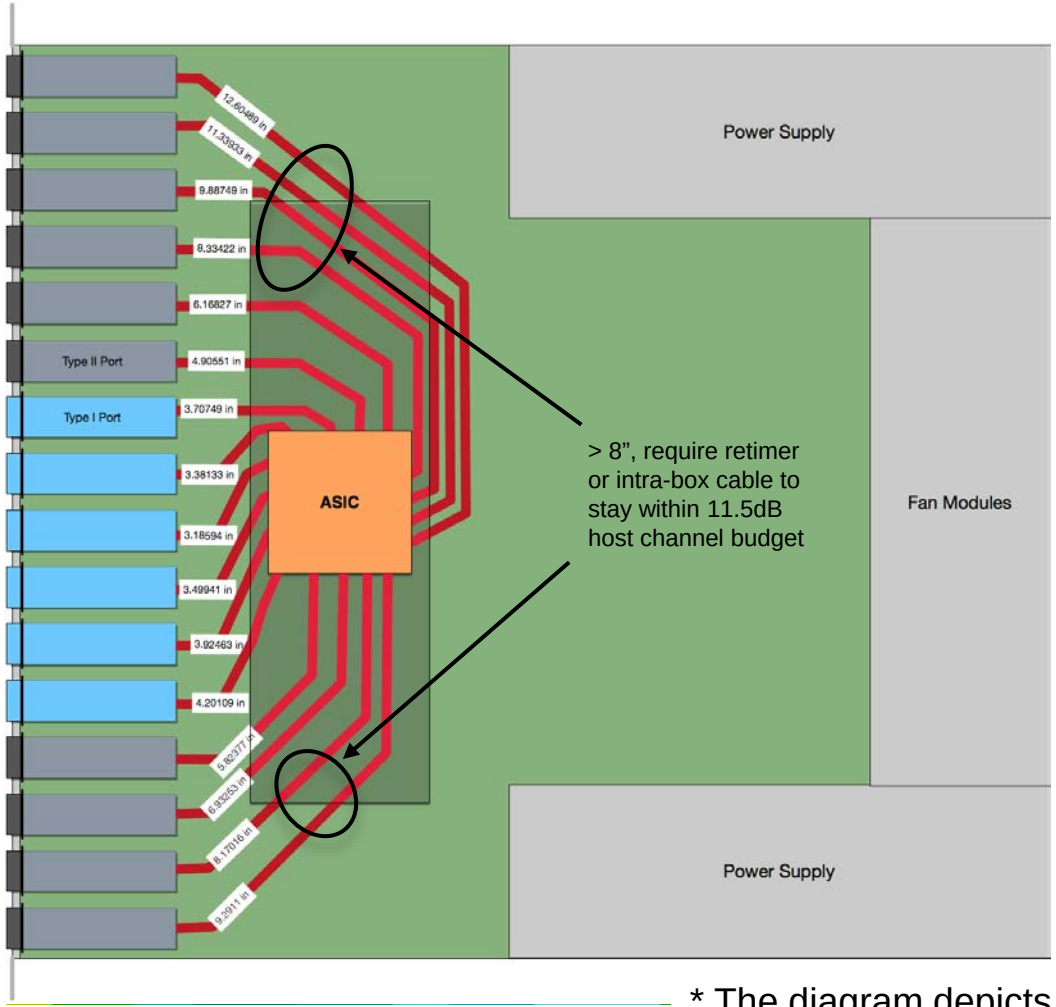
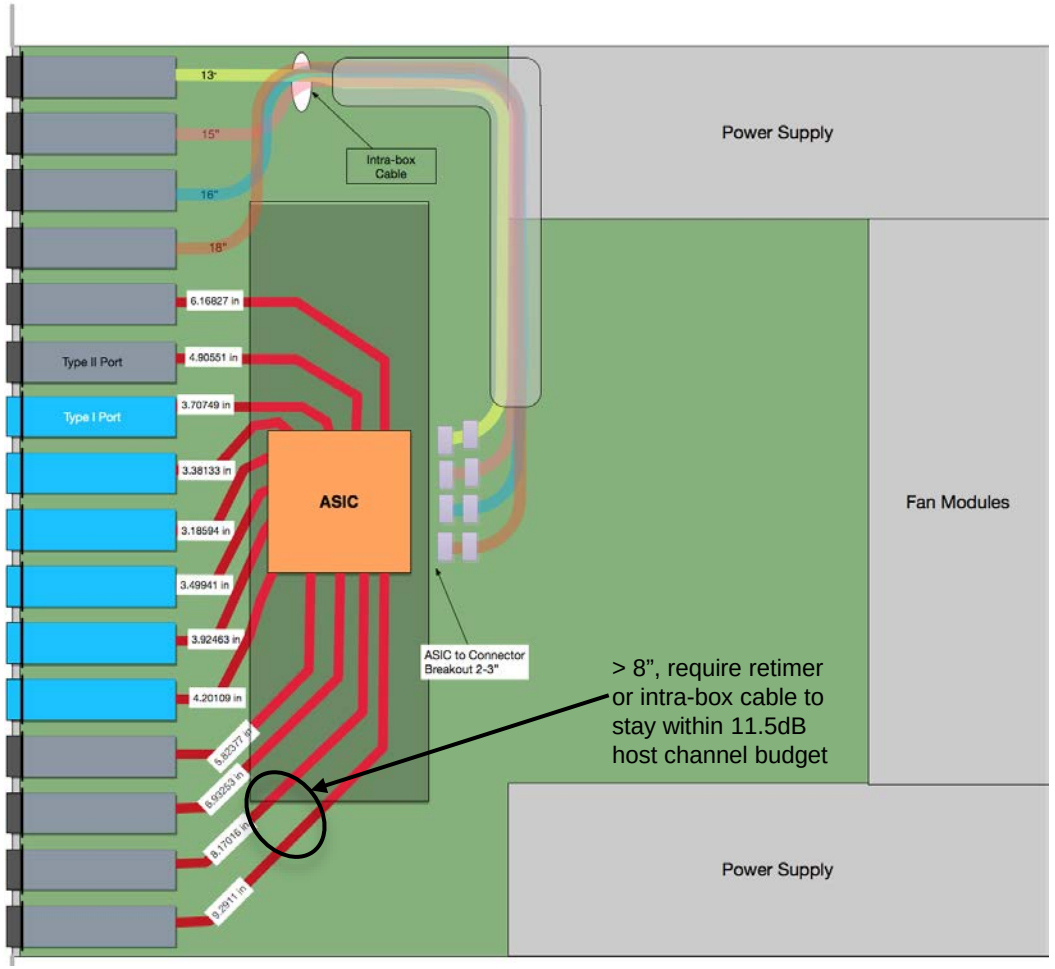


Figure 2: 100GEL CR **TP0-TP2** insertion loss budget at 26.56 GHz

Example TOR Board Placements

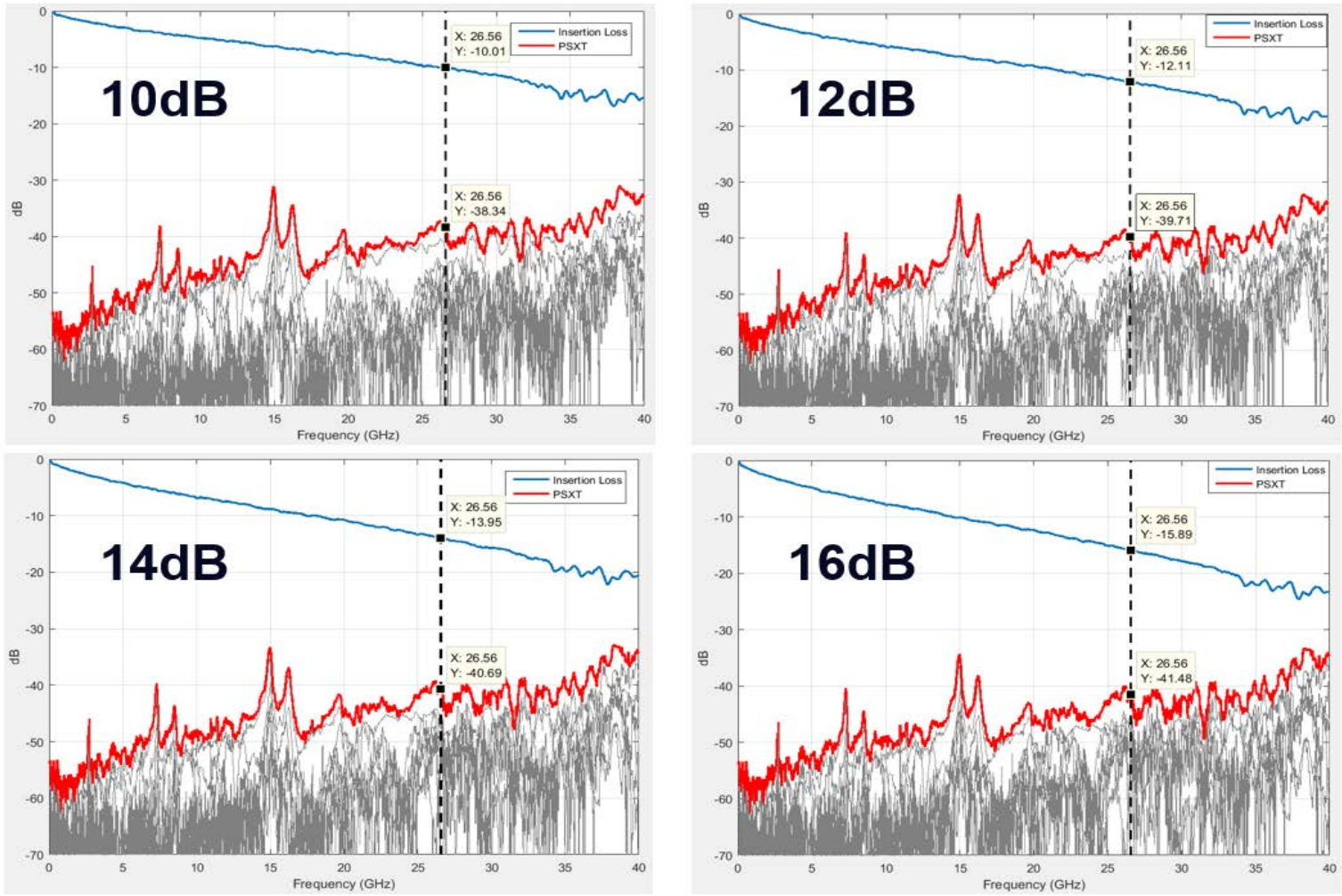
- Symmetric dual port types:
  - Type I: Universal port for both Optics and DAC cables
  - Type II: Optics/AOC/ACC, no DAC cables





* The diagram depicts the actual placement and routed trace length

Cisco C2M Ball-to-Ball Channels



Remark: Package footprint, Host PCB trace and QSFP Test Fixture included.
S-parameter files with 3 different trace lengths can be found at :
http://www.ieee802.org/3/ck/public/tools/c2m/lim_3ck_01_0718.zip

Channel Analysis

- Simulation Setup:
  - Supplier Serdes IBIS-AMI model, run in ADS tool, 1M simulated Bits
  - Data rate: 106.25Gbps PAM4; PRBS23 pattern and Gray-coded
  - TX swing = 900mVpdd, TX FIR (2-pre, 1-main, 1-pst) [0.0625 -0.2500 0.5875 -0.1000]
  - TX jitter added (TX_Dj = 0.05 p-p; TX_Rj = 0.008 UI-rms; TX_DCD = 0.02 p-p)
  - RX EQ/CDR/calibrations are all adaptive; RX noise and jitter are included
  - RX FFE taps (0-pre, 3 pst taps settings: 16, 8 and 4 taps are swept)
  - Package: ~3dB TX and ~2dB RX
- Simulation Results:
  - To achieve better than 1e-6 BER requires 8-pst FFE or higher for upto 16dB ball-ball channel

Channel	16dB	14dB	12dB	10dB
0-pre/16-pst FFE	5.70e-7	5.63e-7	6.24e-7	4.90e-9
0-pre/8-pst FFE	8.07e-7	7.27e-7	9.62e-7	9.97e-9
0-pre/4-pst FFE	1.87e-6	2.06e-6	3.37e-6	4.56e-7

Summary

- C2M reach budget is getting very tight for system design, suggest to break it to 2 port types:
  - Port type 1 with 11.5dB (TP0-TP1a or TP0-TP2) supporting both Optics and DAC cable on a single port
  - Port type 2 with 14-16dB (TP0-TP1a) for Optics/AOC/ACC

- We are still studying Serdes design feasibility and module design implication for Port type 2, areas require feedback:
  - Serdes power impact - Need module/PHY vendors to feedback on Serdes power
  - System cost vs. module cost optimization

Thank You !