
Baseline proposals for copper twinaxial cable specifications

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Background

- Baseline proposals for copper twinaxial cable specifications presented (Sept 2018)
http://www.ieee802.org/3/ck/public/18_09/diminico_3ck_01_0918.pdf
- Straw poll taken to assess support;
http://www.ieee802.org/3/ck/public/18_09/minutes_3ck_0918_unapproved.pdf

Straw Poll #8:

I would support adopting the following baseline proposals for copper twinaxial cable as presented in diminico_3ck_01_0918.pdf

- Figure 136-2 –revised to 100GBASE (slide 8)
- Tx/Rx –PCB IL with TBD (slide 11-13)
- Host Channel IL @ 26.56 GHz with TBD (slide 14)
- Channel and Cable Assembly IL @ 26.56 GHz with TBD (slide 15-16)
- Cable assembly parameters with TBD (slide 17)
- TP0 or TP3 Test Fixture IL: For $0.01 \text{ GHz} \leq f \leq 40(\text{TBD}) \text{ GHz}$ with TBD (slide 18-19)
- Cable assembly test fixture IL with TBD: For $0.01 \text{ GHz} \leq f \leq 40(\text{TBD}) \text{ GHz}$ (slide 20)
- Cable assembly test fixture reference IL with TBD: For $0.01 \text{ GHz} \leq f \leq 40(\text{TBD}) \text{ GHz}$ (slide 21)
- Mated test fixture parameters with TBD (slide 22-23)

Y: 17, N: 3, Need More Information: 27

Background

- Additional information requested
http://www.ieee802.org/3/ck/public/18_09/minutes_3ck_0918_unapproved.pdf

Chair asked for a show of hands regarding moving Straw Poll #8 to a similar motion. Discussion of benefits of framework -style baselines ensued. Conclusion was to not move into motion at this time.

Chris Diminico ask for participants to share what information they would like to see on the copper twin-axial cable baseline. The feedback included:

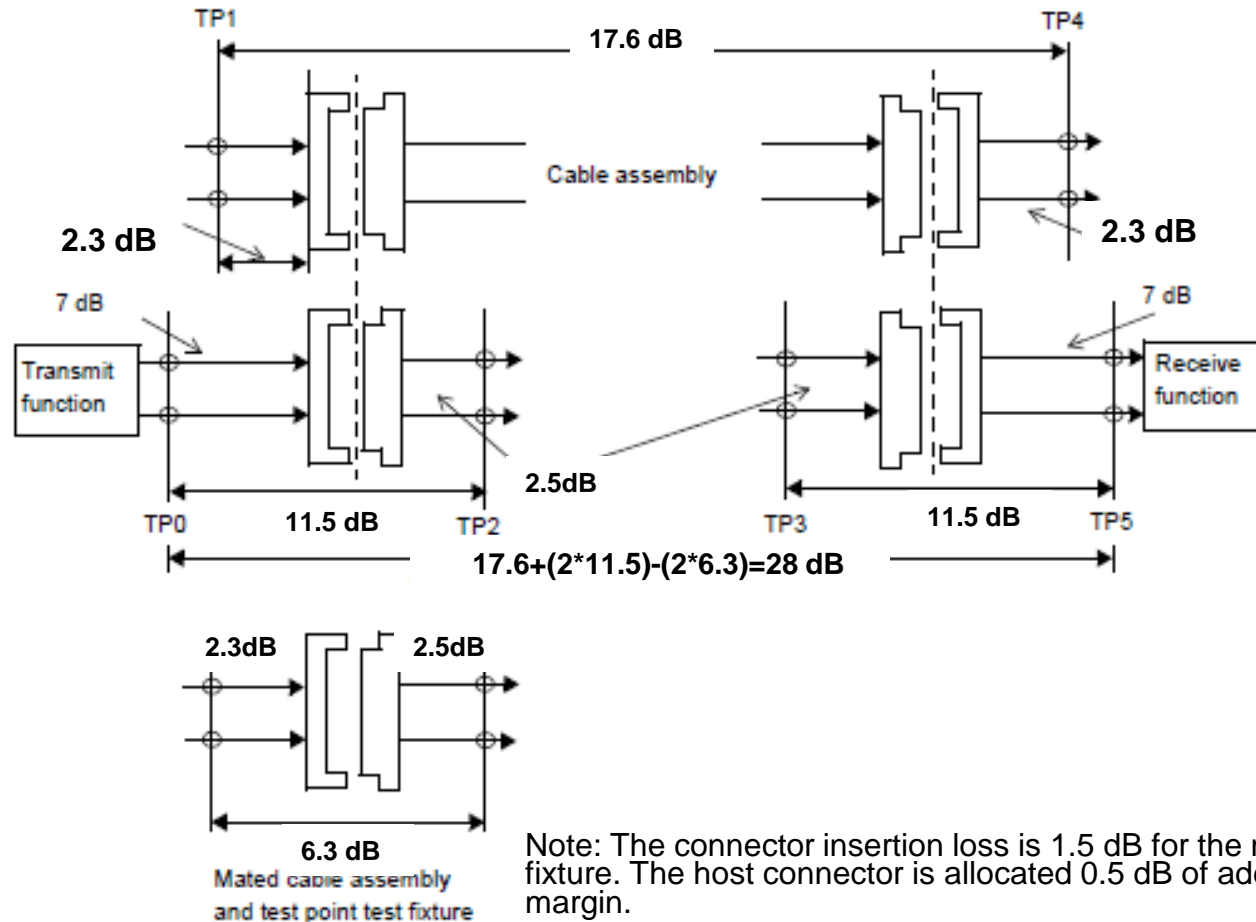
- Remove the TBDs in the framework.
- Example of an end-to-end channel and realistic MDI connectors. Data to support manufacturing feasibility.

Scope

- Provide additional information in support of baseline proposal
http://www.ieee802.org/3/ck/public/18_09/diminico_3ck_01_0918.pdf
- COM results with Cable Assembly S-parameters from Rich Mellitz
 - Baseline proposal cable assembly IL = 17.6 dB @26.56 GHz
 - Synthesized Cable
 - QSFP-DD crosstalk
 - 12 mm and 30 mm package

Cable assembly and Channel IL - Baseline

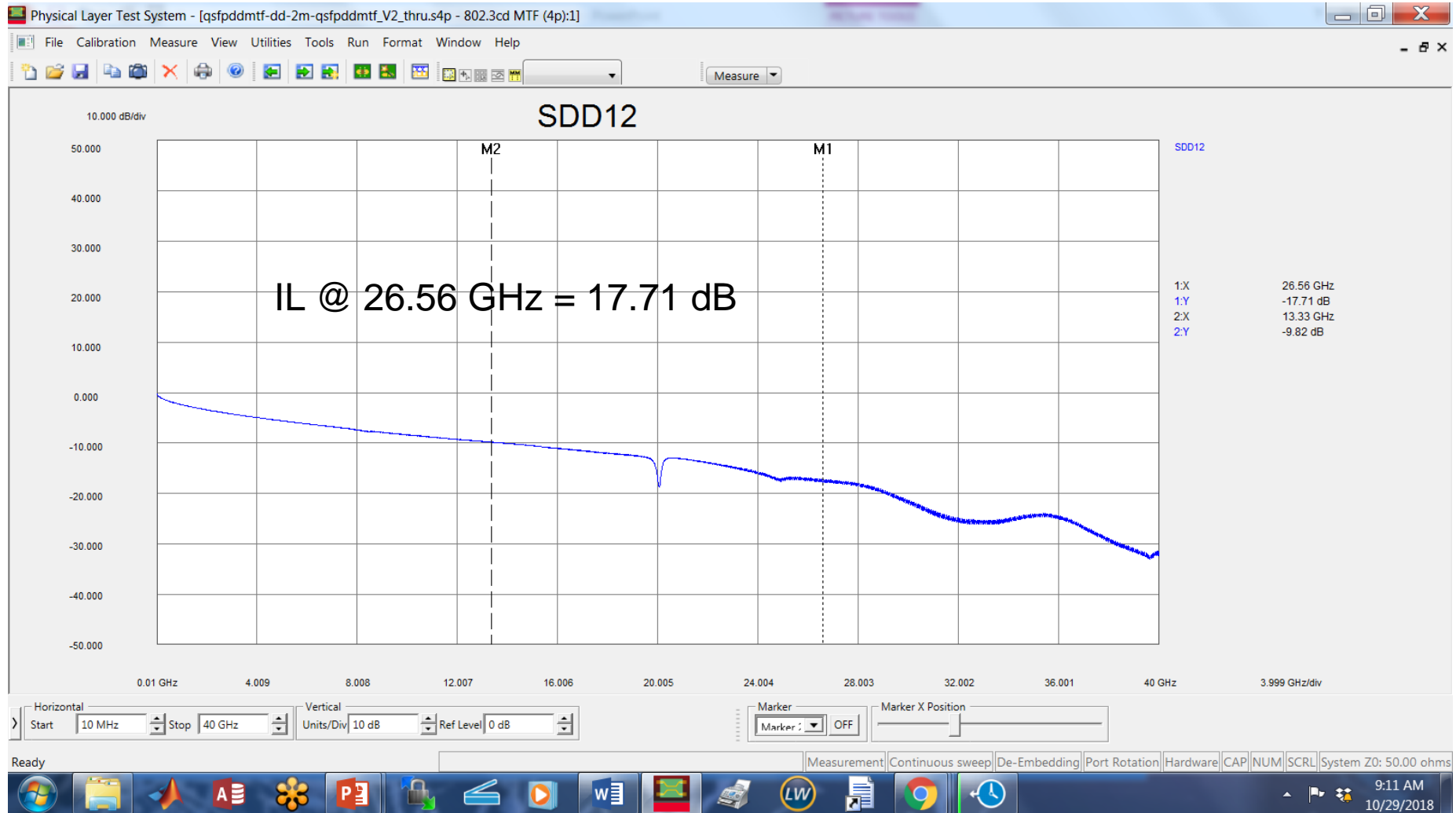
- Cable assembly IL dB @ 26.56 GHz = 10 (bulk cable) + (2*2.3) (TF) + (2*1.5) (connector) = 17.6 dB
- Channel IL dB @ 26.56 GHz = 17.6 (Cable assembly) + 2*11.5 (TP0-TP2) - (2*6.3) MTF = 28 dB
- Channel IL dB @ 26.56 GHz = 10 (bulk cable) + (2*7) Host IL + (2*2) Host connector IL = 28 dB



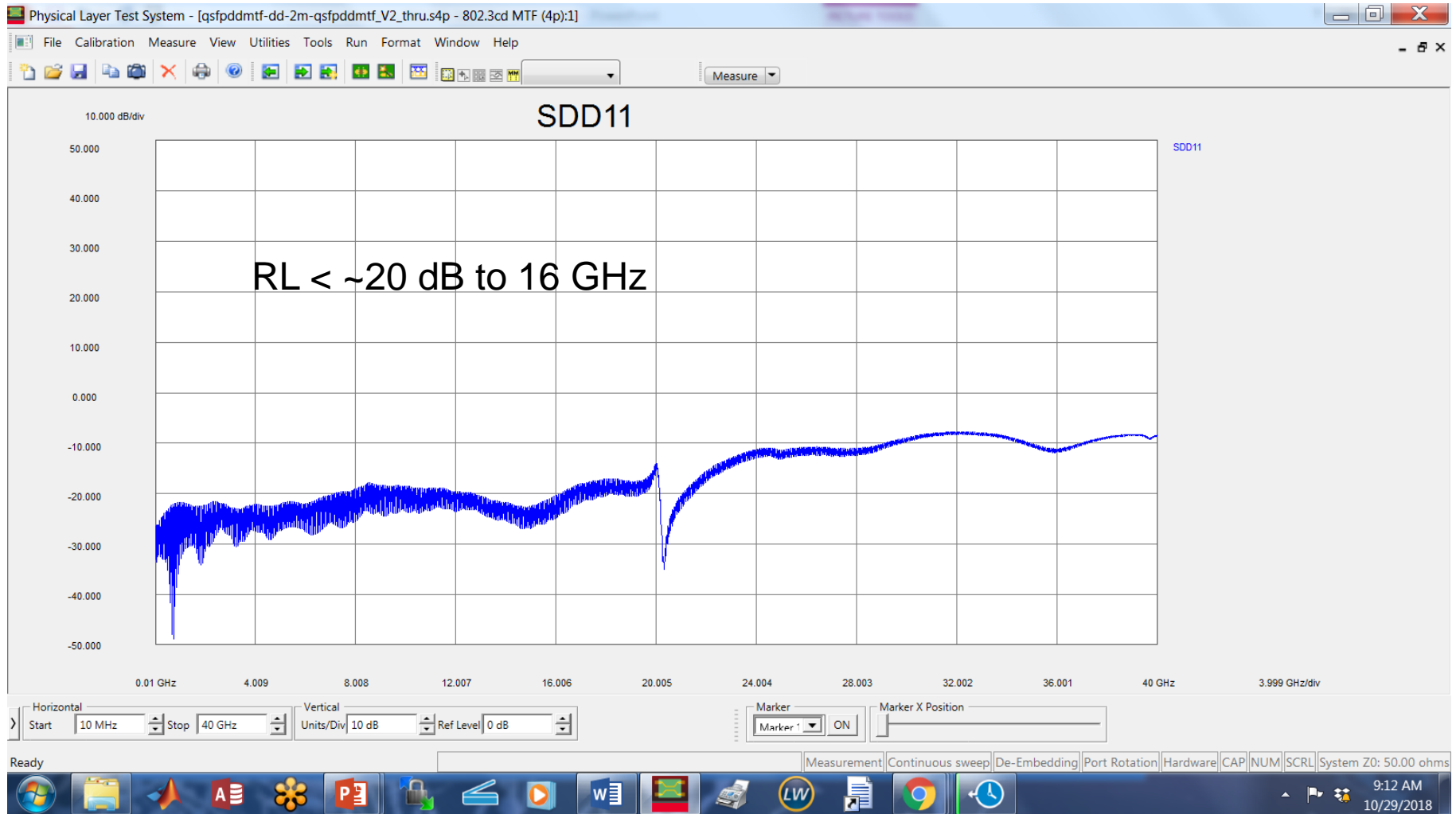
Adopt Channel and Cable Assembly IL @ 26.56 GHz

– use 5 dB @ 26.56 GHz for cable assembly min IL – generate closed form equation

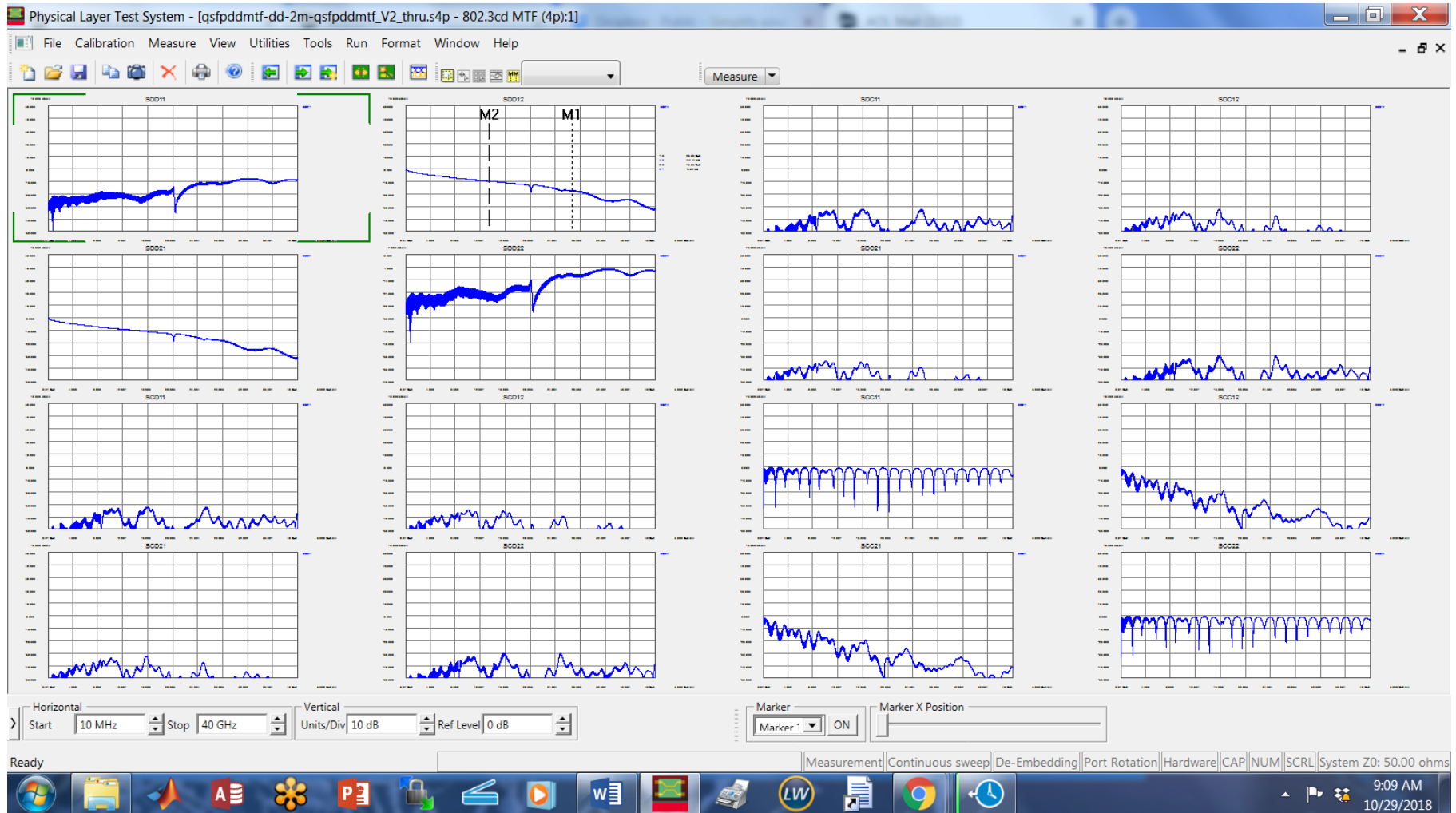
Cable assembly IL



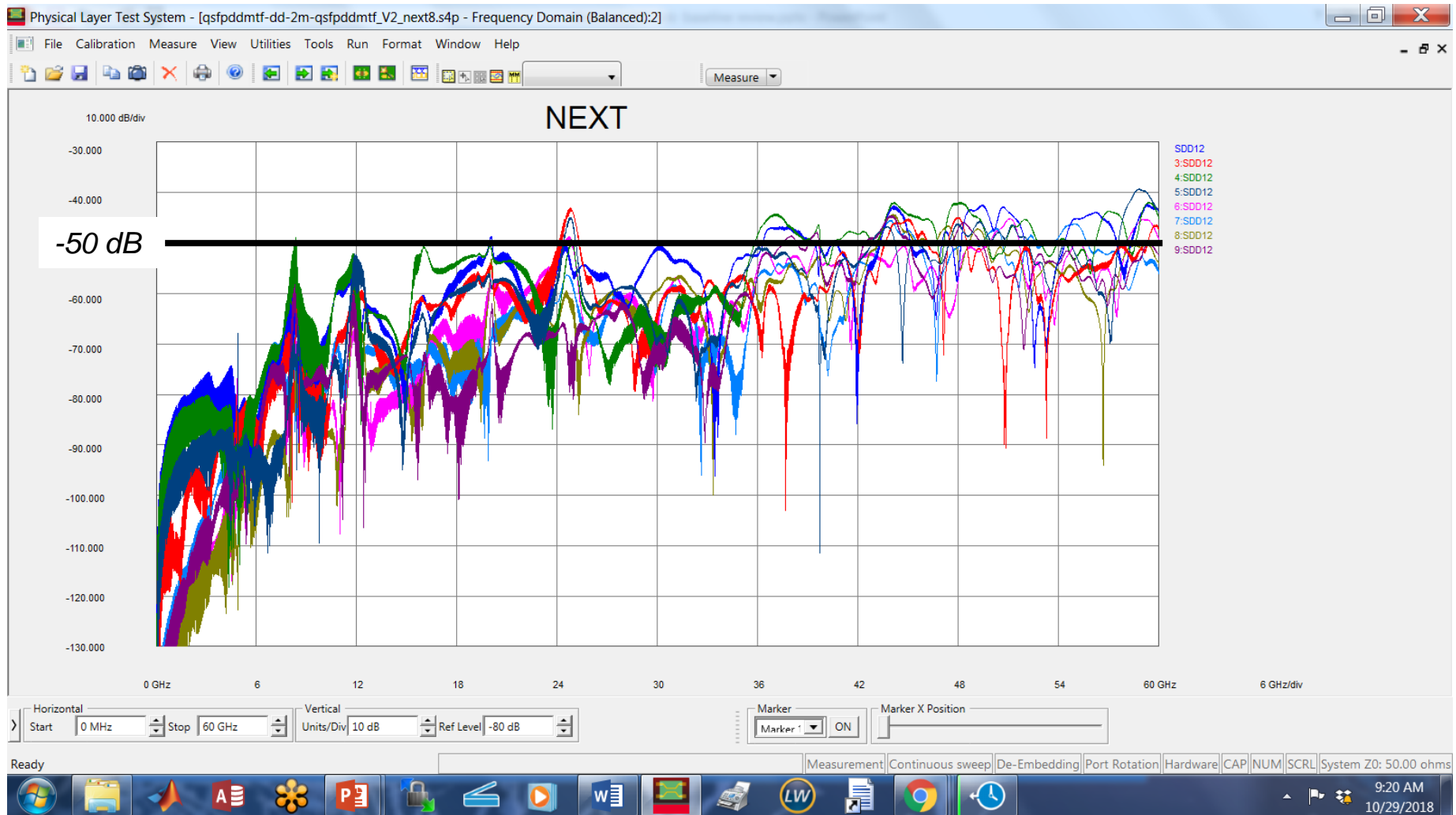
Cable assembly RL



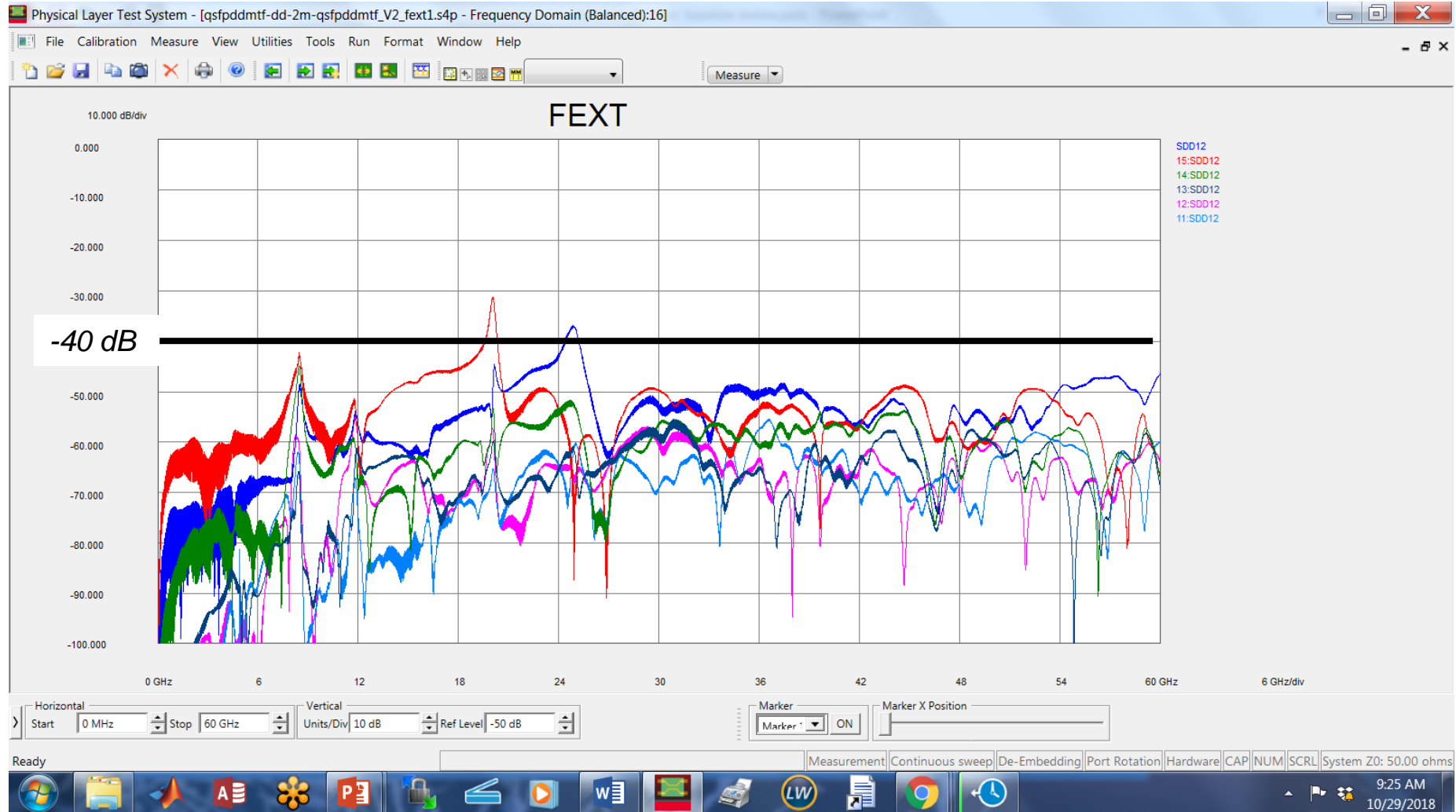
Cable assembly S-parameters



Cable assembly NEXT



Cable assembly FEXT



COM Configuration

Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.1e-4 1.1e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 30; 1.8 1.8; 0 0; 0 0]	mm	[test cases]
z_p (NEXT)	[12 30; 1.8 1.8; 0 0; 0 0]	mm	[test cases]
z_p (FEXT)	[12 30; 1.8 1.8; 0 0; 0 0]	mm	[test cases]
z_p (RX)	[12 30; 1.8 1.8; 0 0; 0 0]	mm	[test cases]
C_p	[0.0e-4 0.0e-4]	nF	[TX RX]
C_v	[0 0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.41	V	
A_fe	0.41	V	
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3 0.025 0]		[min:step:max]
c(-2)	[0.025 0.1]		[min:step:max]
c(-3)	[0 1]		[min:step:max]
c(-4)	[0 1]		[min:step:max]
c(1)	[-0.3 0.05 0]		[min:step:max]
N_b	24	UI	
b_max(1)	0.7		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_P2	0.6640625	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
Include PCB	1	logical	

DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_WG_(date)\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical

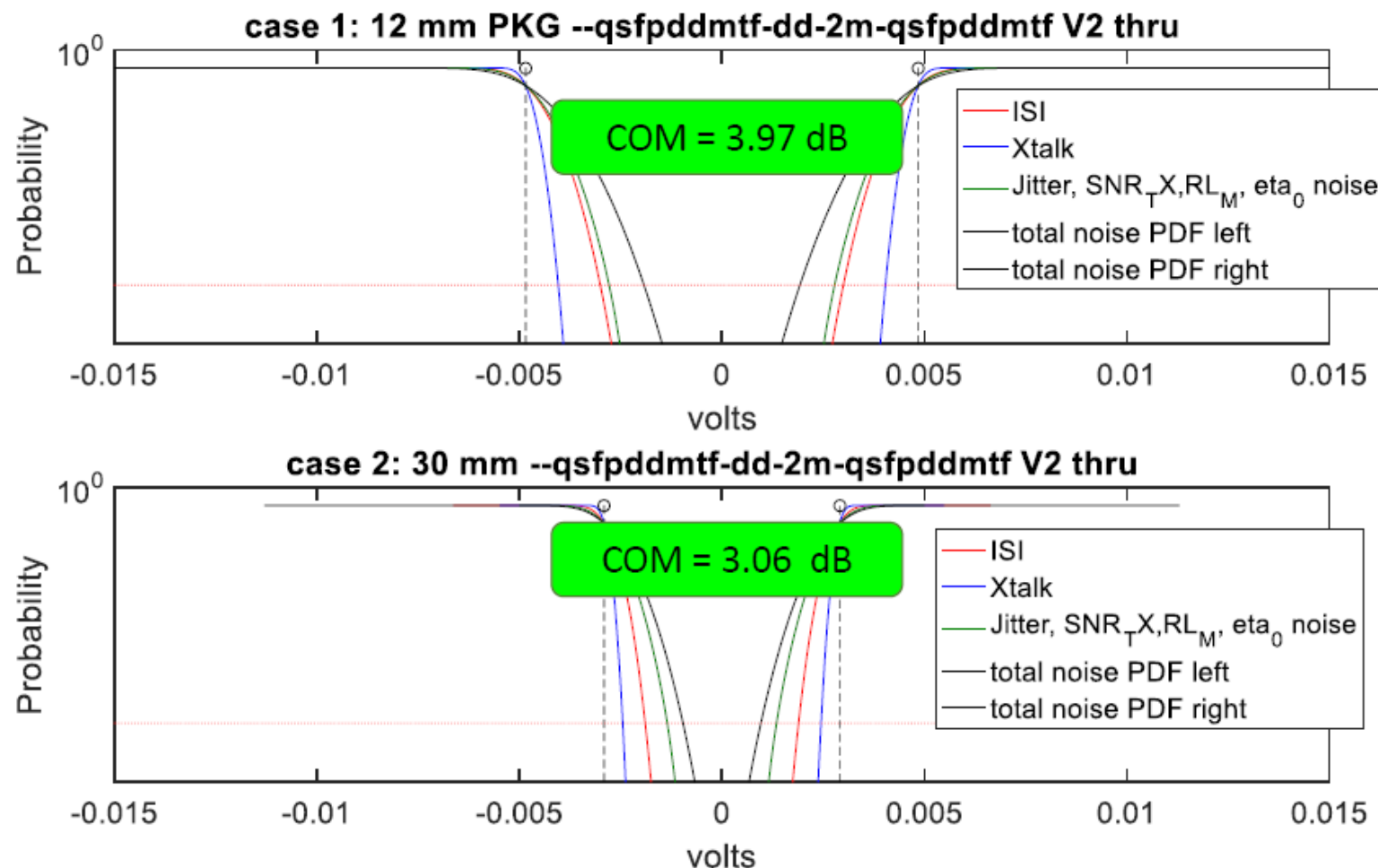
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	1000	
TDR_Butterworth	1	logical
beta_x	1.70E+09	
rho_x	0.25	
fixture delay time	0	enter sec
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0007901838 0.00050925]	
package_tl_tau	6.325E-03	ns/mm
package_z_c	[87.5 87.5 ; 92.5 92.5; 100 100 ; 100 100]	Ohm (tdr sel)

Table 92-12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_z_c	90	Ohm
z_bp (TX)	119	mm
z_bp (NEXT)	119	mm
z_bp (FEXT)	119	mm
z_bp (RX)	119	mm

COM Results – from Rich Mellitz



Insertion Loss – real cable



Summary

- Provided additional information in support of baseline proposal
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