

Server Backplane Channels

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IEEE 802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force.

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Summary

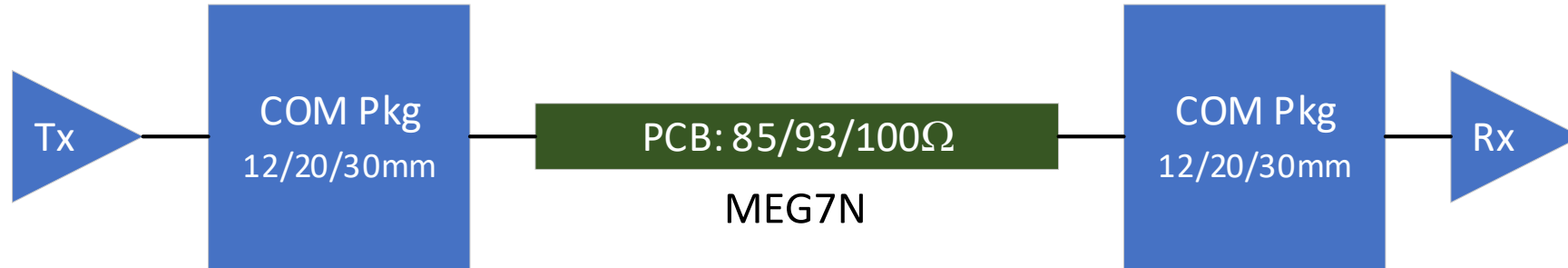
- Cabled backplane channel contribution:
 - Characteristics
 - 3FEXT, 4FEXT aggressors
 - 16dB to 28dB insertion loss
 - 0.575m & 0.995m cable length
 - 85 Ω -100 Ω PCB
 - We need channels like these to work for 100GKR.
- Getting them to work with 30mm package requires at least 20 taps in the Rx reference EQ.

Outline

- **Baseline**
 - Ideal Channel: Simple PCB Transmission Line
 - Ideal Channel with Impedance Mismatch
- **Realistic Channels (Cabled Backplane)**
 - Description
 - Frequency Response
 - COM results
- **Channel Contribution**

Ideal Channel

All analysis uses 802.3cd-based COM pkg model.



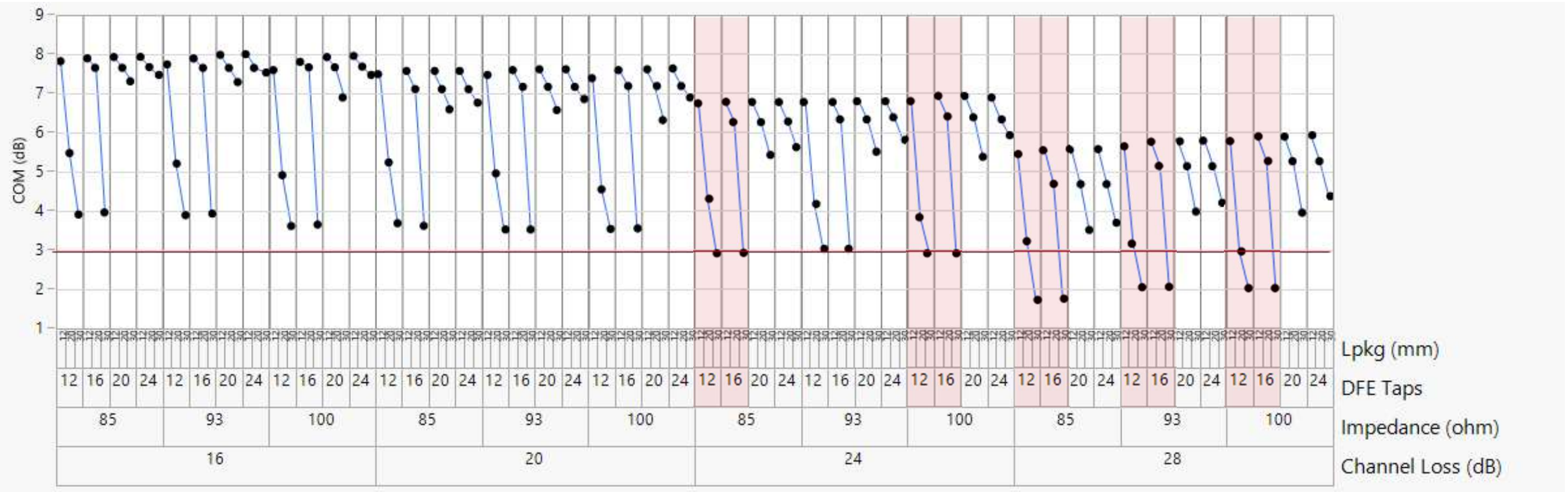
IL (dB)	Z _{diff} (Ω)	# DFE taps	Pkg (mm)
16	85	12	12
20	93	16	20
24	100	20	30
28		24	

(4x3x4x3)=144 cases total

COM Template Used (2.51)

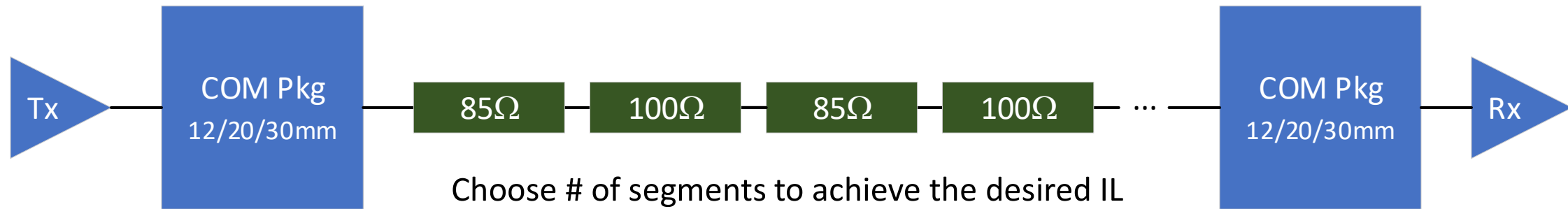
Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information				Parameter	Setting	Units
f_b	53.125	GBd		DIAGNOSTICS	0	logical	package_tl_gamma0_a1_a2	[0 1.734e-3 1.455e-4]	
f_min	0.05	GHz		DISPLAY_WINDOW	0	logical	package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz		CSV_REPORT	1	logical	package_Z_c	90	Ohm (Tx Rx)
C_d	[1.3e-4 1.3e-4]	nF	[TX RX]	RESULT_DIR	.\Test251_PKG_DFE24_{date}\		Table 92-12 parameters		
z_p select	[1 2 3]		[test cases to run]	SAVE_FIGURES	1	logical	board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
z_p (TX)	[12 20 30]	mm	[test cases]	Port Order	[1 3 2 4]		board_tl_tau	6.191E-03	ns/mm
z_p (NEXT)	[12 20 30]	mm	[test cases]	RUNTAG	DFE24_		board_Z_c	110	Ohm
z_p (FEXT)	[12 20 30]	mm	[test cases]	COM_CONTRIBUTION	0	logical	z_bp (TX)	151	mm
z_p (RX)	[12 20 30]	mm	[test cases]	Operational			z_bp (NEXT)	72	mm
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]	COM Pass threshold	3	dB	z_bp (FEXT)	72	mm
C_v	[0e-6 0e-6]	nF	[TX RX]	DER_0	1.00E-04		z_bp (RX)	151	mm
R_0	50	Ohm		Include PCB	0	Value			
R_d	[50 50]	Ohm	[TX RX]	T_r	6.16E-03	ns			
A_v	0.41	V		FORCE_TR	1	logical			
A_fe	0.41	V		TDR and ERL options					
A_ne	0.6	V		TDR	1	logical			
L	4			ERL	1	logical			
M	32			ERL_ONLY	0	logical			
filter and Eq				TR_TDR	0.01	ns			
f_r	0.75	*fb		N	1000				
c(0)	0.6		min	TDR_Butterworth	1	logical			
c(-1)	[-0.3:0.025:0]		[min:step:max]	beta_x	1.70E+09				
c(-2)	[0:.025:0.01]		[min:step:max]	rho_x	0.18				
c(-3)	0		[min:step:max]	fixture delay time	0				
c(-4)	0		[min:step:max]	Receiver testing					
c(1)	[-0.2:0.05:0]		[min:step:max]	RX_CALIBRATION	0	logical			
N_b	24	UI		Sigma BBN step	5.00E-03	V			
b_max(1)	0.7			Noise, jitter					
b_max(2..N_b)	0.2			sigma_RJ	0.01	UI			
g_DC	[-20:2:-10]	dB	[min:step:max]	A_DD	0.02	UI			
f_z	21.25	GHz		eta_0	8.20E-09	V^2/GHz			
f_p1	21.25	GHz		SNR_TX	32.5	dB			
f_p2	53.125	GHz		R_LM	0.95				
g_DC_HP	[-6:1:0]		[min:step:max]	BREAD_CRUMBS					
f_HP_PZ	0.6640625	GHz			1				
ffe_pre_tap_len	0	UI							
ffe_post_tap_len	0	UI							
ffe_tap_step_size	0								
ffe_main_cursor_min	0								
ffe_pre_tap1_max	0								
ffe_post_tap1_max	0								
ffe_tapn_max	0								

Ideal Channel COM Results



- Need ~20tap Rx EQ to meet 3dB COM for a 28dB channel made up of a PCB transmission line with 30mm packages.
- Channels with more reflections (vias, connectors, etc.) may need more taps.

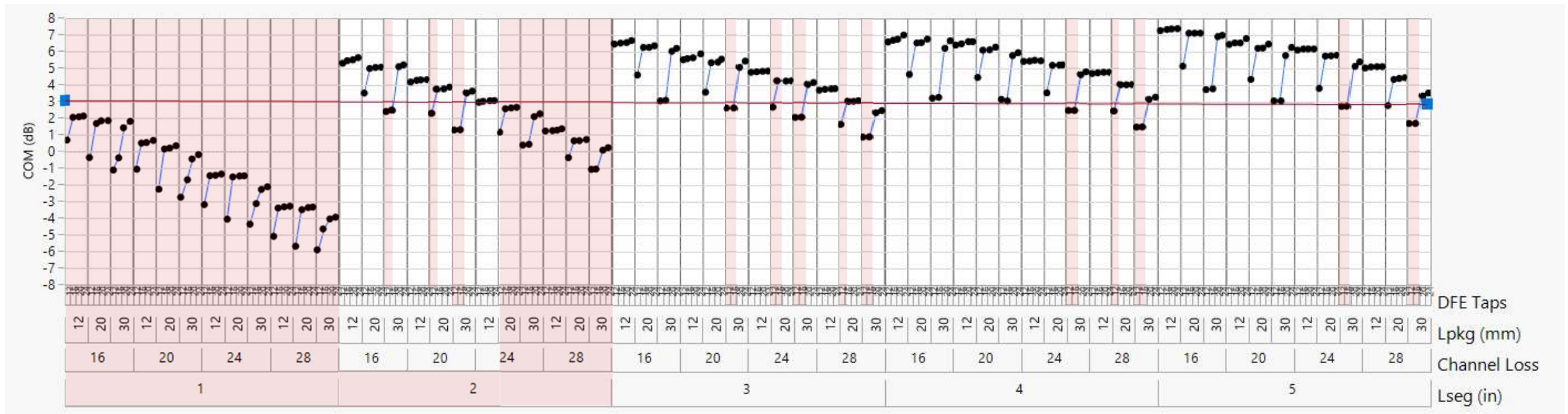
Ideal Channel w/ Reflections



IL (dB)	Segment Length (in)	# DFE taps	Pkg (mm)
16	1	12	12
20	2	16	20
24	3	20	30
28	4	24	
	5		

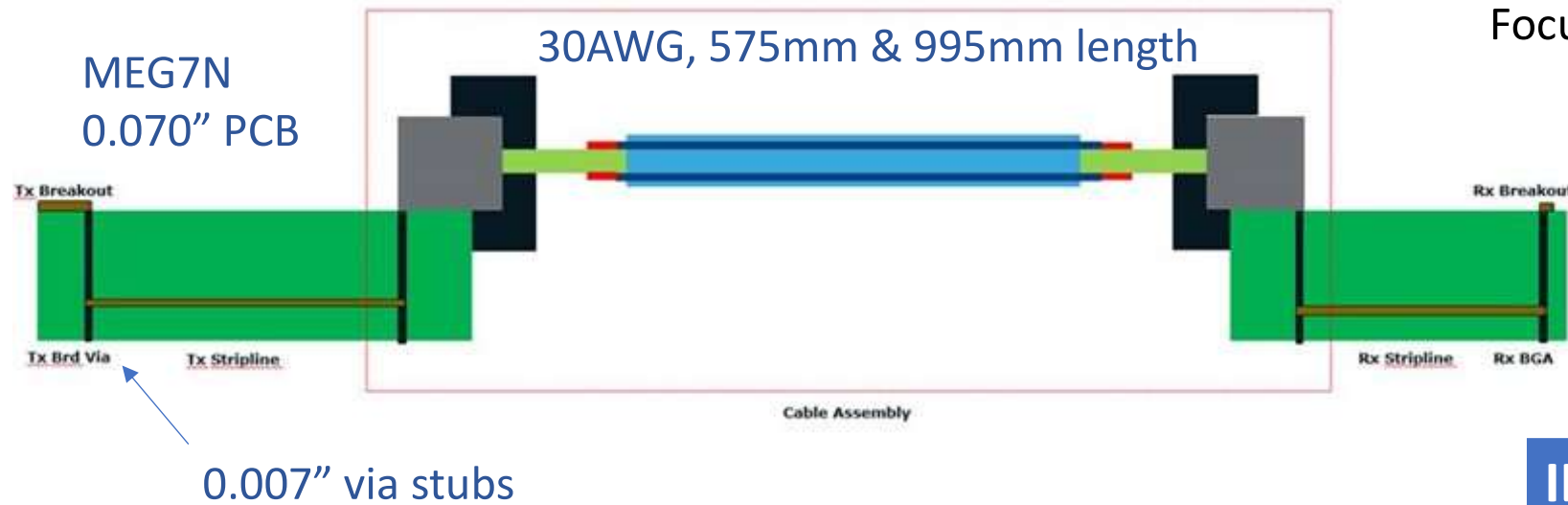
(4x5x4x3)=240 cases total

Ideal Channel w/ Reflections: COM Results



Added reflections likely push the Rx EQ need beyond 20 taps.

Realistic Channels



Focus on Cabled Backplanes

- TP0-TP4 (pkg ball-to-pkg ball)
- Symmetric Tx/Rx PCB trace lengths
- 3 FEXT, 4 NEXT aggressors: <2mV RMS
- No P/N skew
- "High ISI": half of PCB trace @ 85Ω, half @ 100Ω

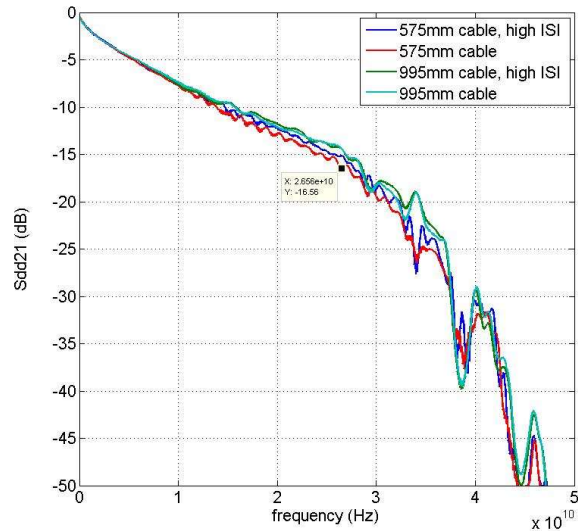
IL (dB)	Cable (m)	# DFE taps	Pkg (mm)	ISI
16	0.575	12	12	Low
20	0.995	16	20	High
24		20	30	
28		24		

(4x2x4x3x2)=192 cases

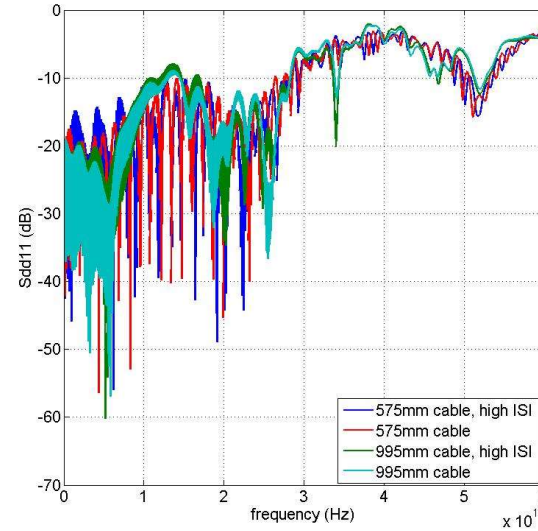
Insertion Loss & Return Loss

16dB

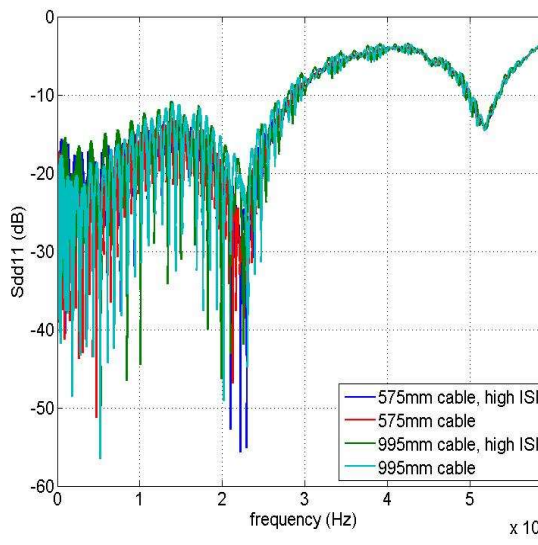
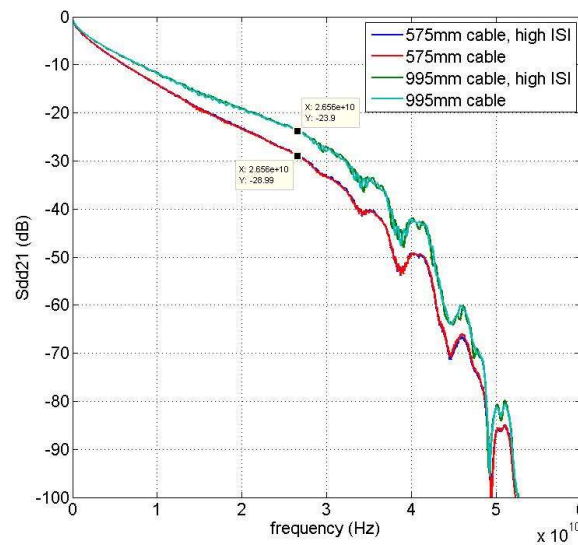
Insertion Loss



Return Loss



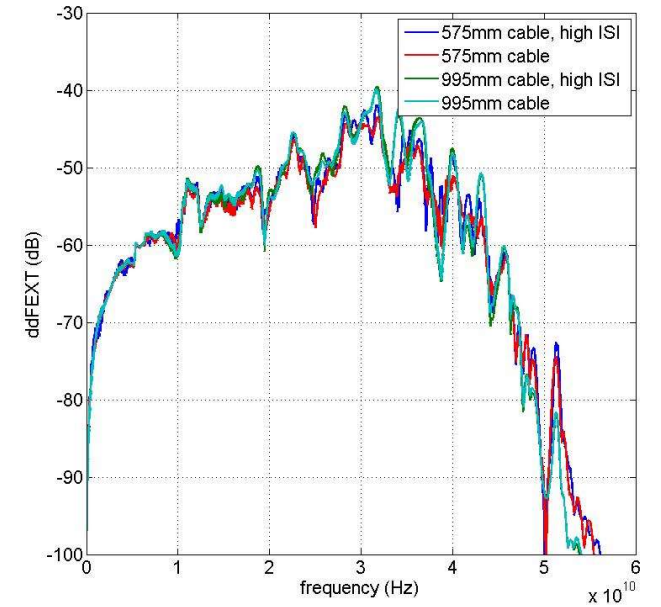
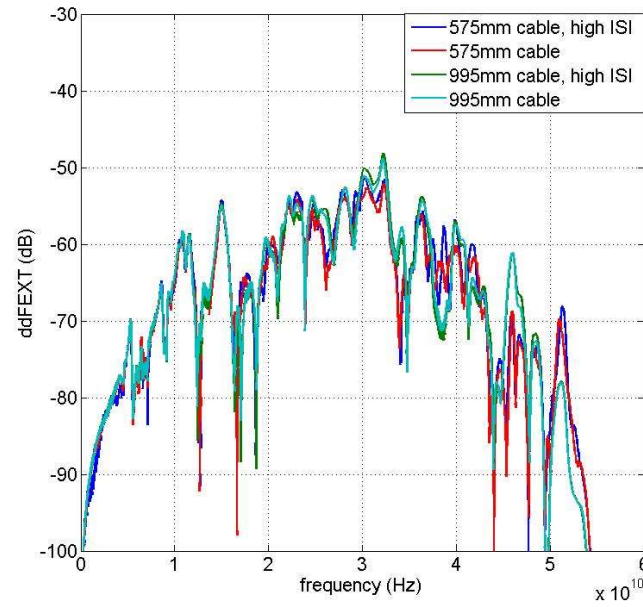
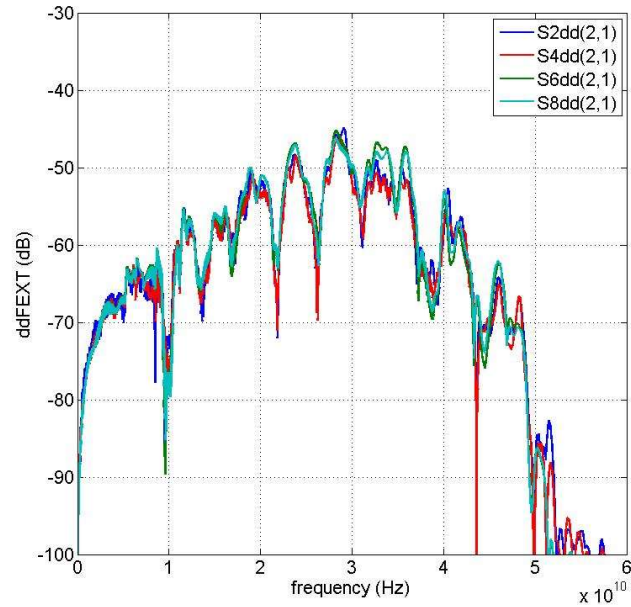
28dB



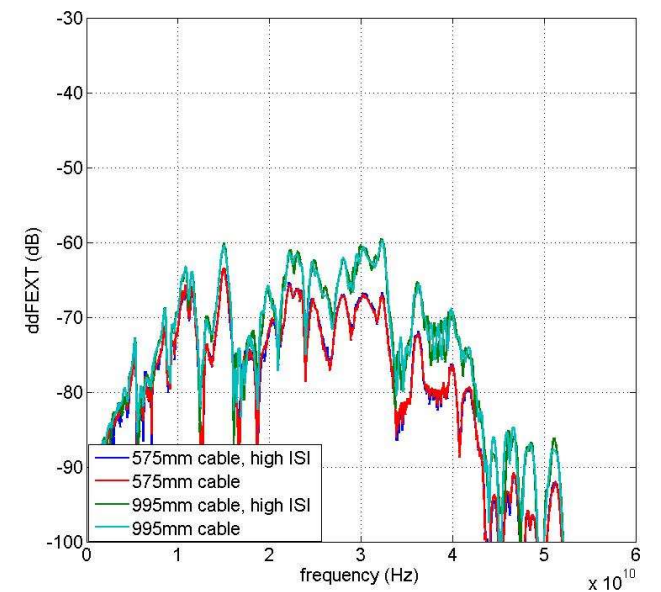
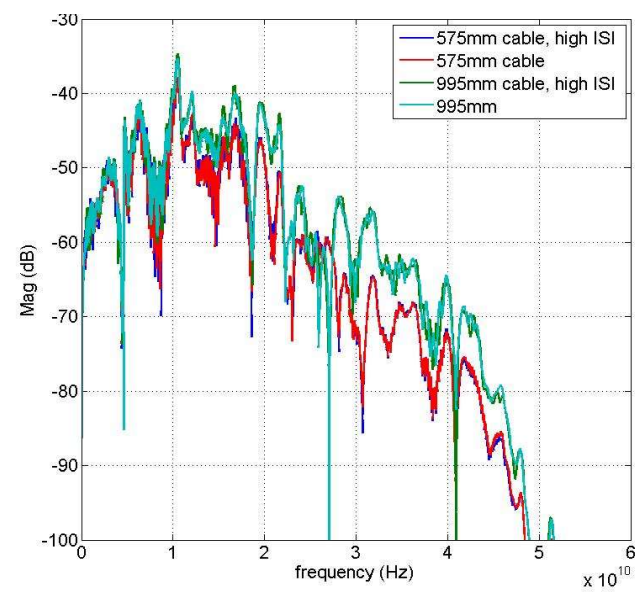
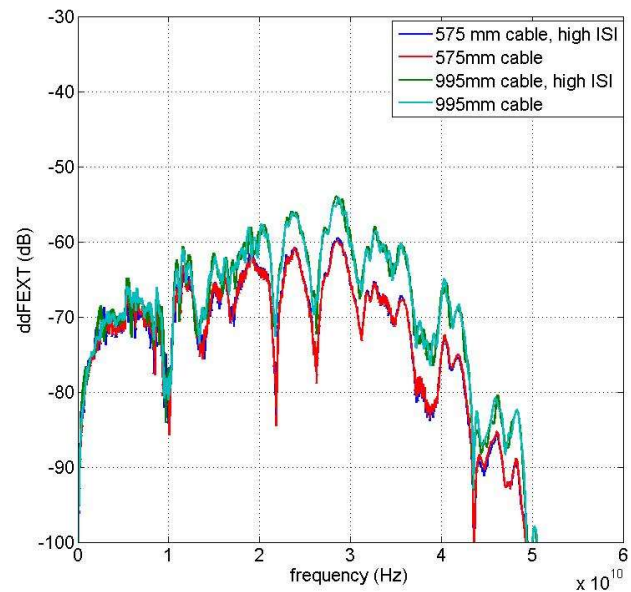
“High ISI” means impedance mismatch is included in the Tx & Rx PCBs.

FEXT

16dB

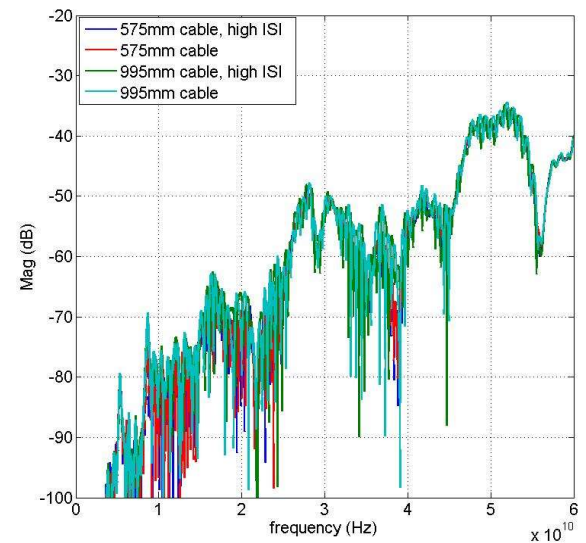
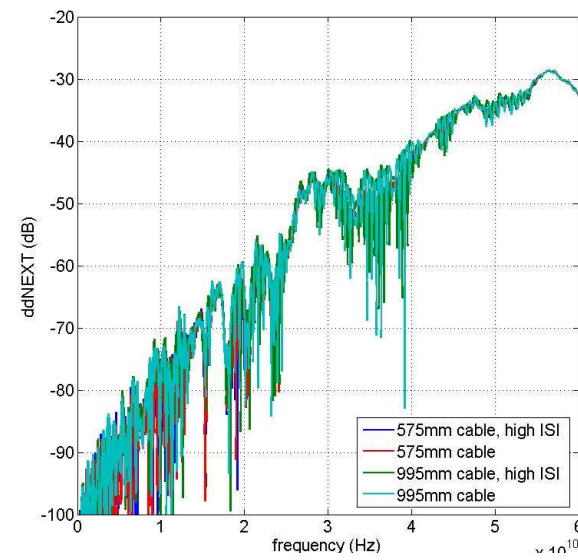
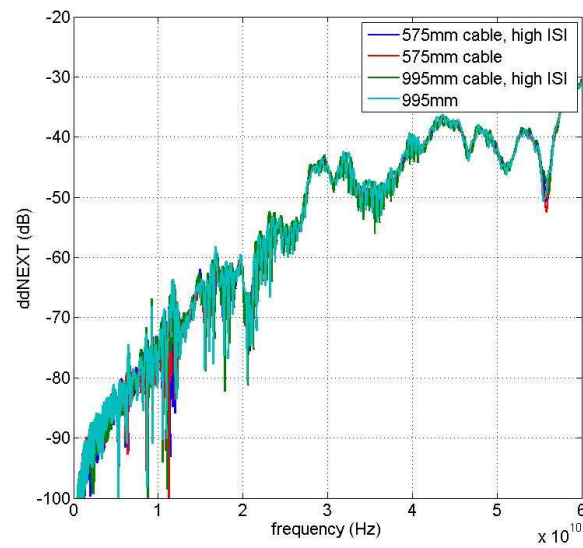
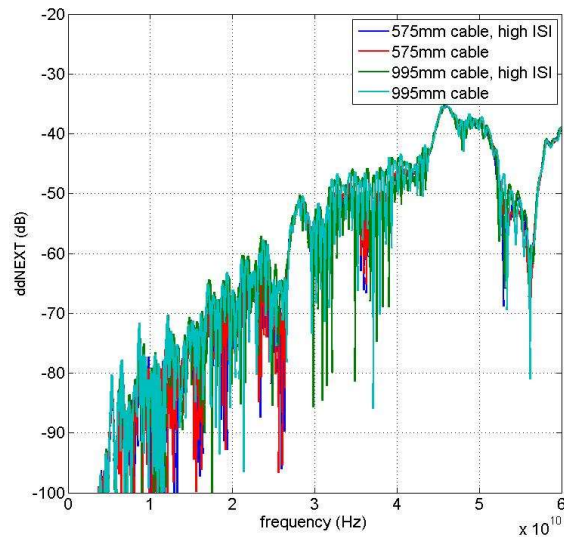


28dB

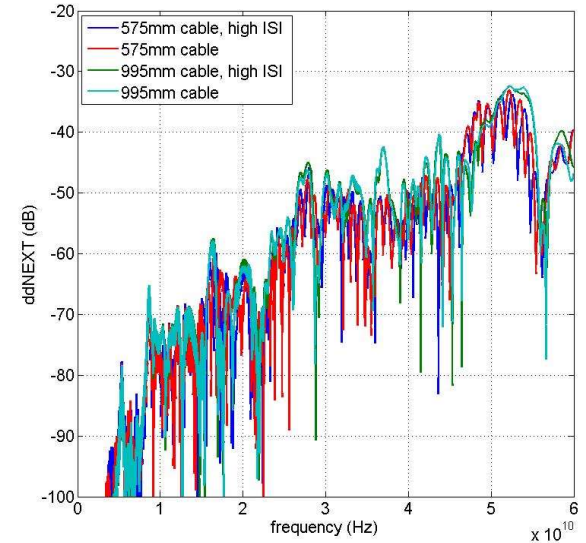
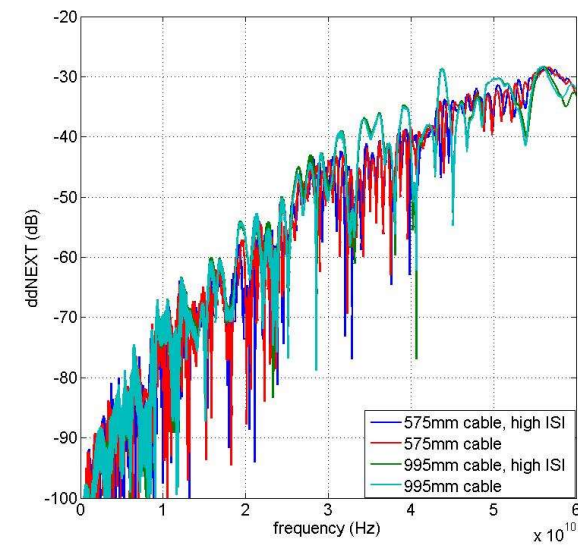
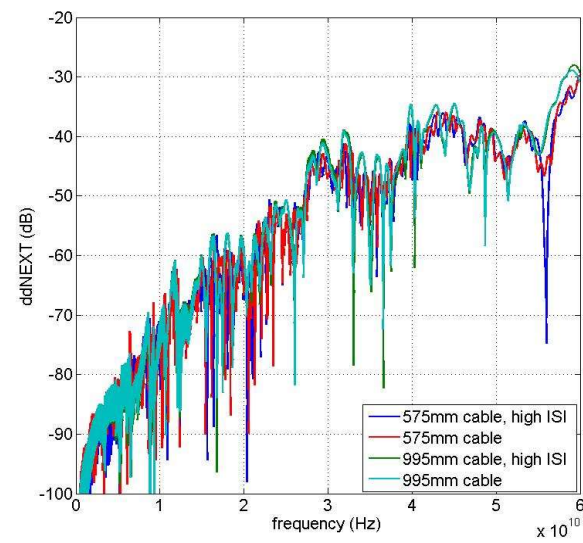
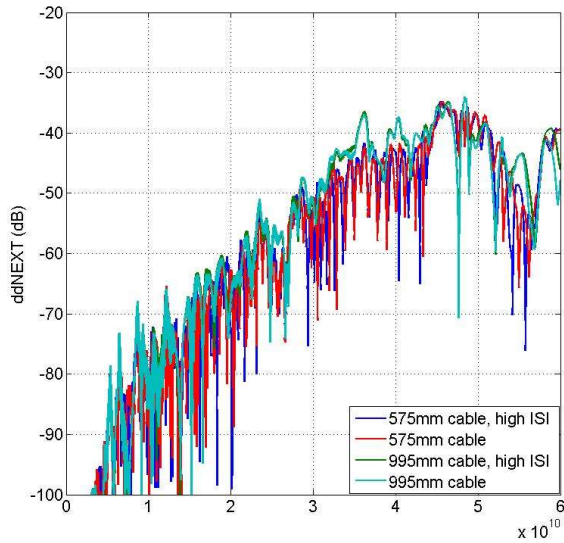


NEXT

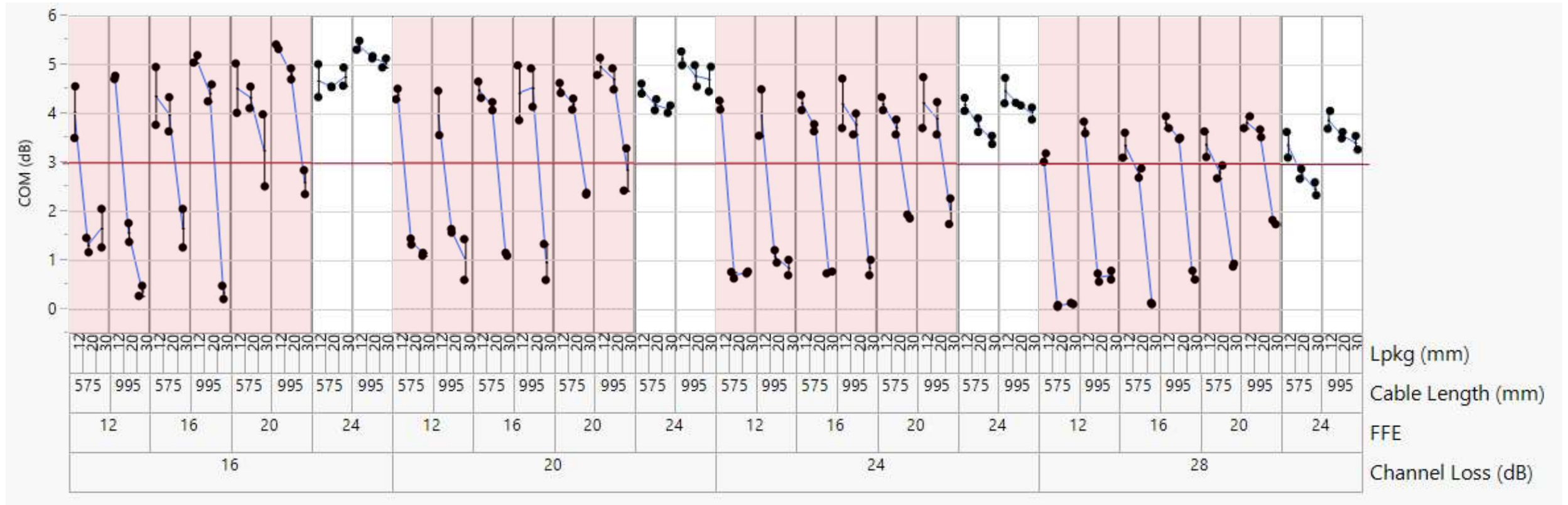
16dB



28dB



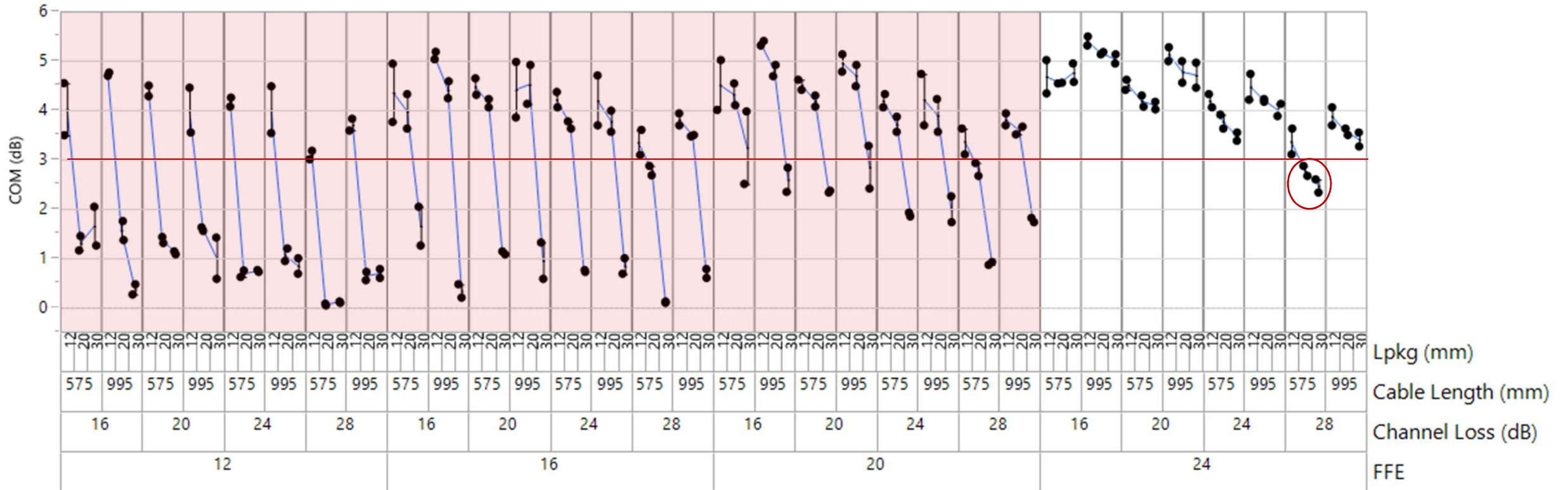
COM Results



Recommended focus channels:

- High loss: 28dB channel with 575mm cable & “high ISI”
- High reflection: 16dB channel with 575mm cable & “high ISI”

COM Results (Alternate View)



Contributed Cabled Backplane Channel

IL (dB)	Cable (mm)	Z _{PCB} mismatch	Zip folder	File
16	575	No	Cable_BKP_16dB.zip	Cable_BKP_16dB_0p575m.zip
		Yes		Cable_BKP_16dB_0p575m_more_isi.zip (L)
	995	No		Cable_BKP_16dB_0p995m.zip
		Yes		Cable_BKP_16dB_0p0p995m_more_isi.zip
20	575	No	Cable_BKP_20dB.zip	Cable_BKP_20dB_0p575m.zip
		Yes		Cable_BKP_20dB_0p575m_more_isi.zip
	995	No		Cable_BKP_20dB_0p995m.zip
		Yes		Cable_BKP_20dB_0p0p995m_more_isi.zip
24	575	No	Cable_BKP_24dB.zip	Cable_BKP_24dB_0p575m.zip
		Yes		Cable_BKP_24dB_0p575m_more_isi.zip
	995	No		Cable_BKP_24dB_0p995m.zip
		Yes		Cable_BKP_24dB_0p0p995m_more_isi.zip
28	575	No	Cable_BKP_28dB.zip	Cable_BKP_28dB_0p575m.zip
		Yes		Cable_BKP_28dB_0p575m_more_isi.zip (R)
	995	No		Cable_BKP_28dB_0p995m.zip
		Yes		Cable_BKP_28dB_0p0p995m_more_isi.zip

Notes:

- Each zip contains 8 S4P files.
 - thru: *_thru1
 - FEXT: *_xtalk1_Fext
*_xtalk2_Fext
*_xtalk3_Fext
 - NEXT: *_xtalk1_Next
*_xtalk2_Next
*_xtalk3_Next
*_xtalk3_Next
- Recommended boundary cases:
 - (L) Maximum loss
 - (R) Maximum reflection

Summary

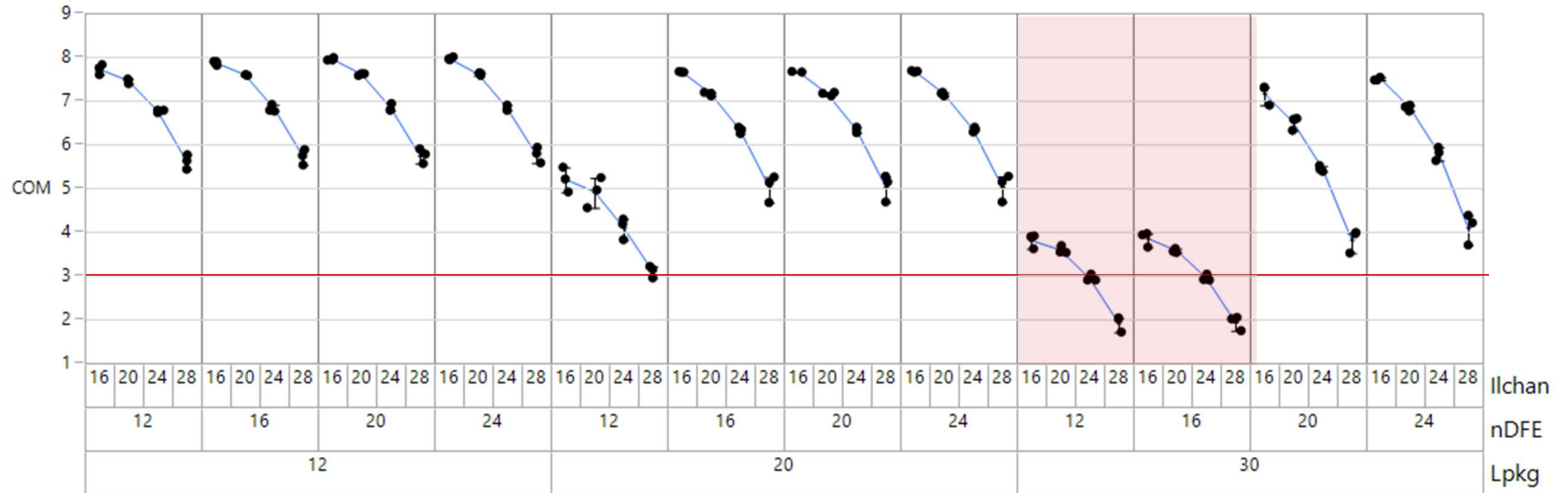
- Cabled backplane channel contribution:
 - Characteristics
 - 3FEXT, 4FEXT aggressors
 - 16dB to 28dB insertion loss
 - 0.575m & 0.995m cable length
 - 85 Ω -100 Ω PCB
 - We need channels like these to work for 100GKR.
- Getting them to work with 30mm package requires at least 20 taps in the Rx reference EQ.

Thank you!

COM Template - FFE

f_min	0.05	GHz		CSV_REPORT	1	logical	package_tl_tau	6.141E-03	ns/mm		
Delta_f	0.01	GHz		RESULT_DIR	\\Test251_PKG_RxFFE24_{date}		package_Z_c	90	Ohm (Tx Rx)		
C_d	[1.3e-4 1.3e-4]	nF	[TX RX]	SAVE_FIGURES	1	logical	Table 92-12 parameters				
z_p_select	[1 2 3]		[test cases to run]	Port Order	[1 3 2 4]		Parameter	Setting			
z_p (TX)	[12 20 30]	mm	[test cases]	RUNTAG	RxFFE24_		board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]			
z_p (NEXT)	[12 20 30]	mm	[test cases]	COM_CONTRIBUTION	0	logical	board_tl_tau	6.191E-03	ns/mm		
z_p (FEXT)	[12 20 30]	mm	[test cases]	Operational			board_Z_c	110	Ohm		
z_p (RX)	[12 20 30]	mm	[test cases]	COM Pass threshold	3	dB	z_bp (TX)	151	mm		
C_p	[1.1e-4 1.1e-4]	nF	[TX RX]	DER_0	1.00E-04		z_bp (NEXT)	72	mm		
C_v	[0e-6 0e-6]	nF	[TX RX]	Include PCB	0	Value	z_bp (FEXT)	72	mm		
R_0	50	Ohm		T_r	6.16E-03	ns	z_bp (RX)	151	mm		
R_d	[50 50]	Ohm	[TX RX]	FORCE_TR	1	logical					
A_v	0.41	V		TDR and ERL options							
A_fe	0.41	V		TDR	1	logical					
A_ne	0.6	V		ERL	1	logical					
L	4			ERL_ONLY	0	logical					
M	32			TR_TDR	0.01	ns					
filter and Eq				N	1000						
f_r	0.75	*fb		TDR Butterworth	1	logical					
c(0)	0.6		min	beta_x	1.70E+09						
c(-1)	[-0.3:0.025:0]		[min:step:max]	rho_x	0.18						
c(-2)	[0:.025:0.01]		[min:step:max]	fixture delay time	0						
c(-3)	0		[min:step:max]	Receiver testing							
c(-4)	0		[min:step:max]	RX_CALIBRATION	0	logical					
c(1)	[-0.2:0.05:0]		[min:step:max]	Sigma BBN step	5.00E-03	V					
N_b	1	UI		Noise, jitter							
b_max(1)	0.7			sigma_RJ	0.01	UI					
b_max(2..N_b)	0.2			A_DD	0.02	UI					
g_DC	[-20:2:-10]	dB	[min:step:max]	eta_0	8.20E-09	V^2/GHz					
f_z	21.25	GHz		SNR_TX	32.5	dB					
f_p1	21.25	GHz		R_LM	0.95						
f_p2	53.125	GHz		BREAD_CRUMBS							
g_DC_HP	[-6:1:0]		[min:step:max]		1						
f_HP_PZ	0.6640625	GHz									
ffe_pre_tap_len	3	UI									
ffe_post_tap_len	24	UI									
ffe_tap_step_size	0.01										
ffe_main_cursor_min	0.7										
ffe_pre_tap1_max	0.3										
ffe_post_tap1_max	0.3										
ffe_tapn_max	0.125										

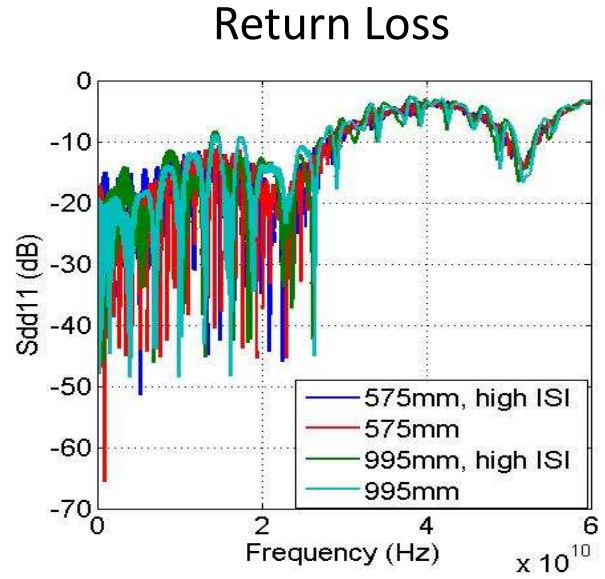
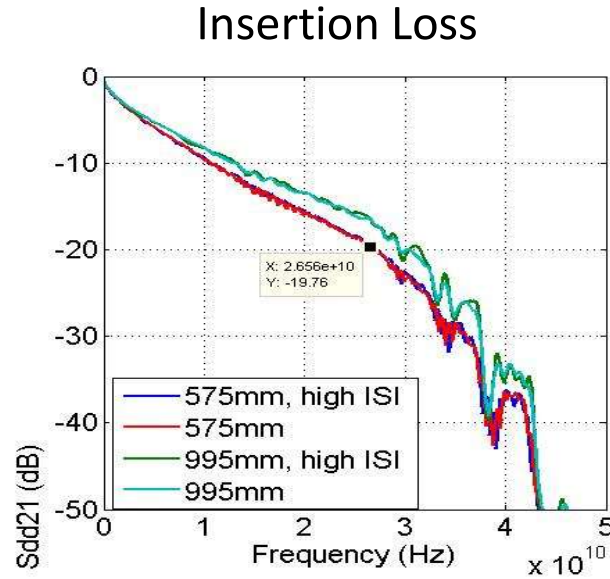
Ideal Channel COM Results



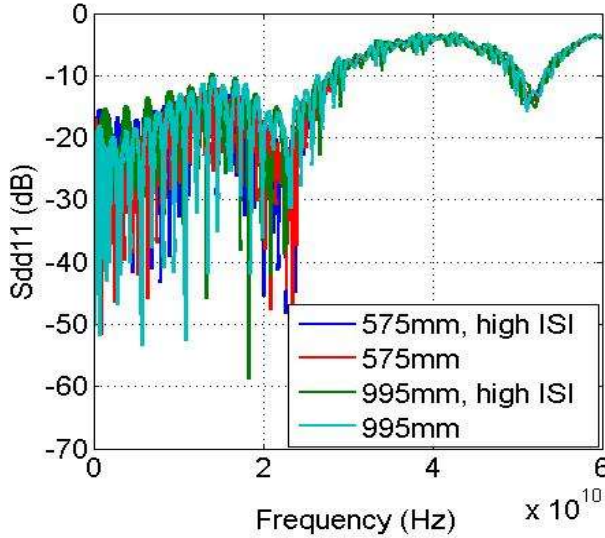
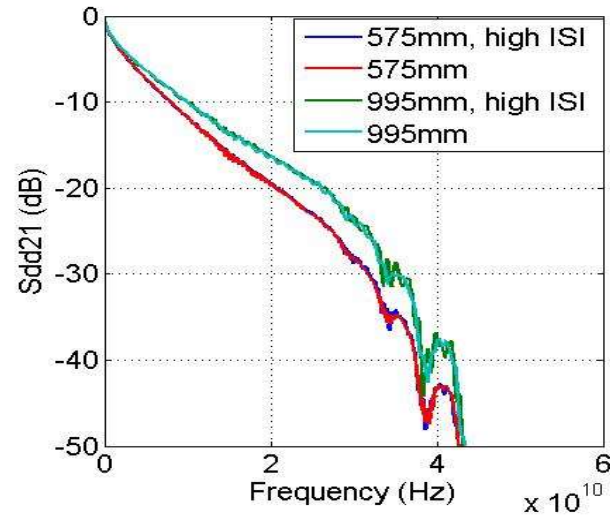
30mm package length drives 20+ taps

Insertion Loss & Return Loss

20dB



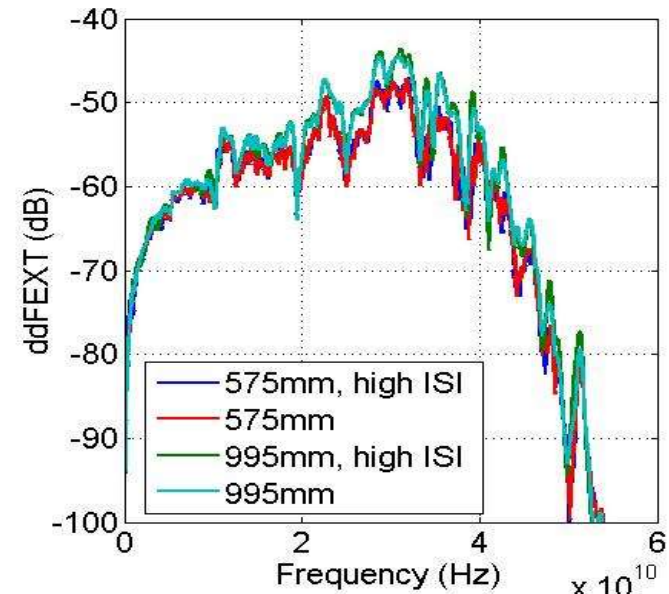
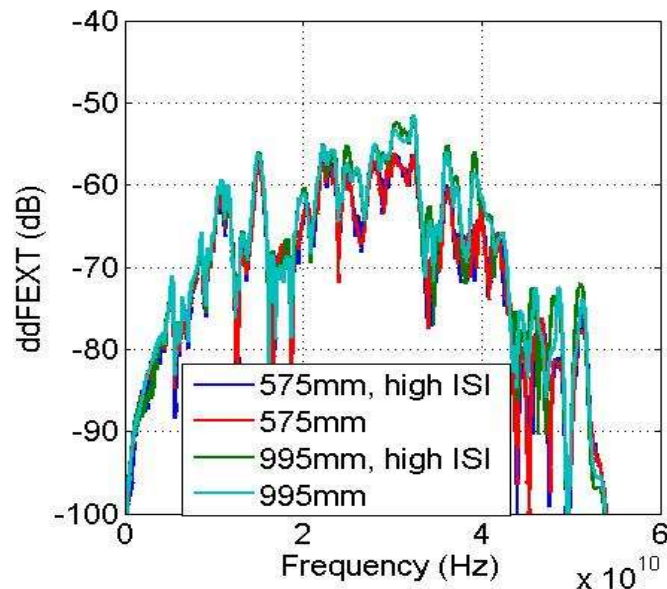
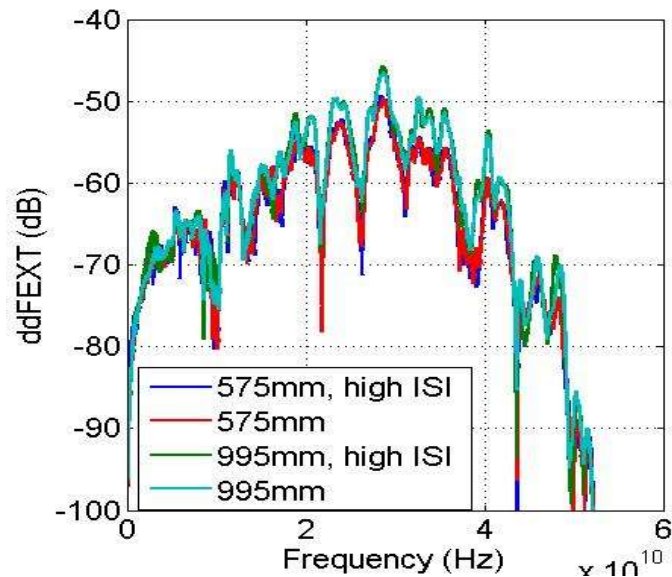
24dB



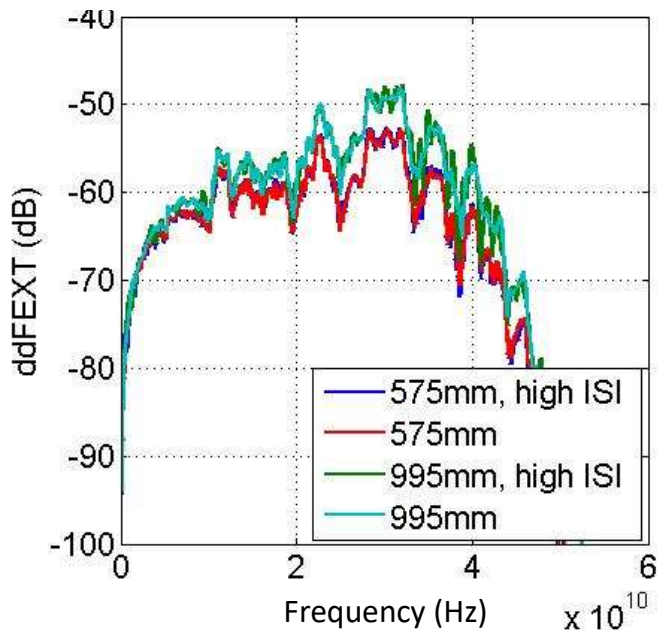
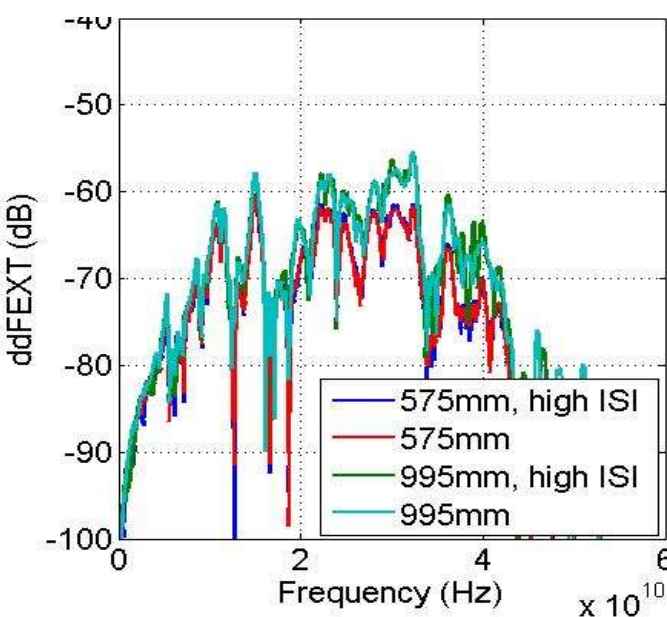
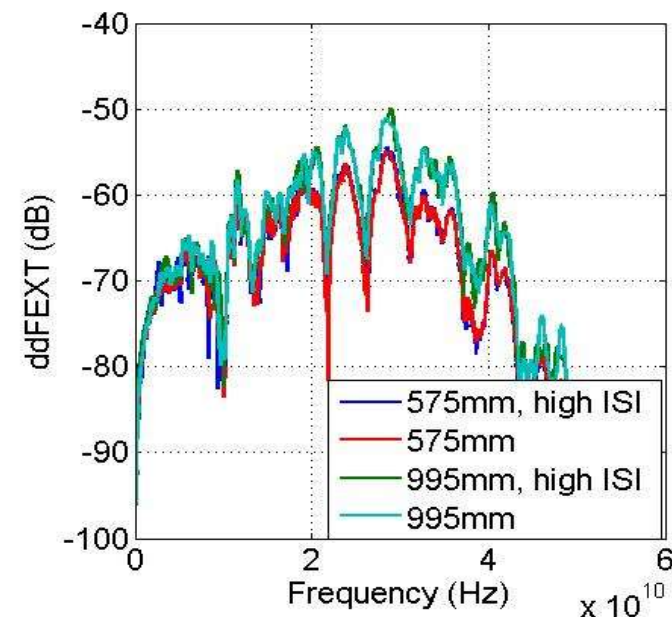
“high ISI” means PCB mismatch is included (both Tx & Rx PCBs).

FEXT Response

20dB

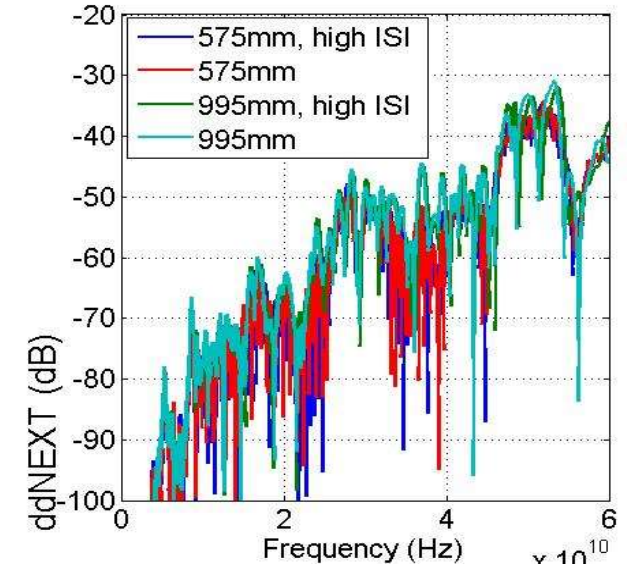
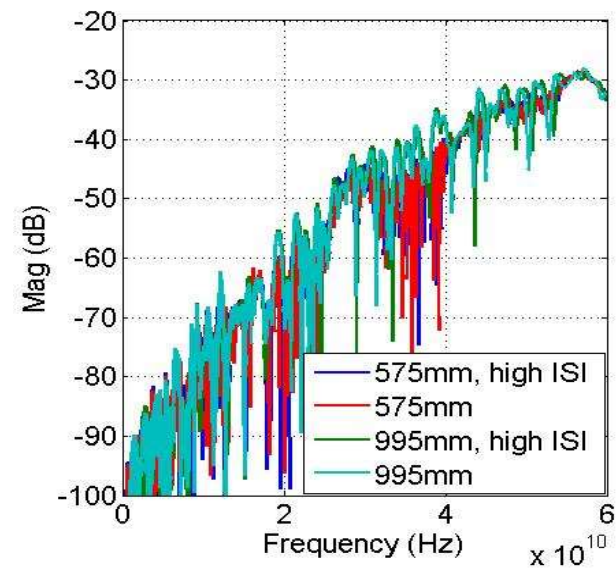
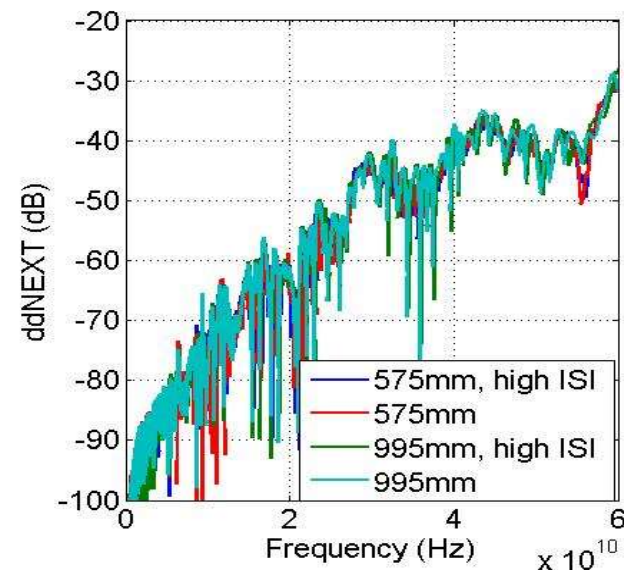
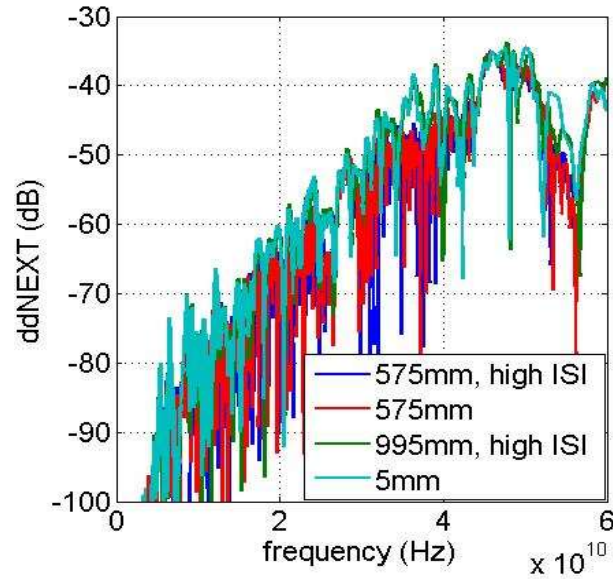


24dB

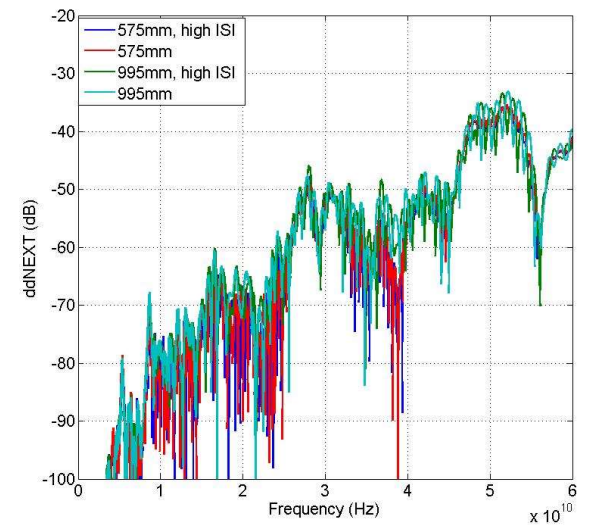
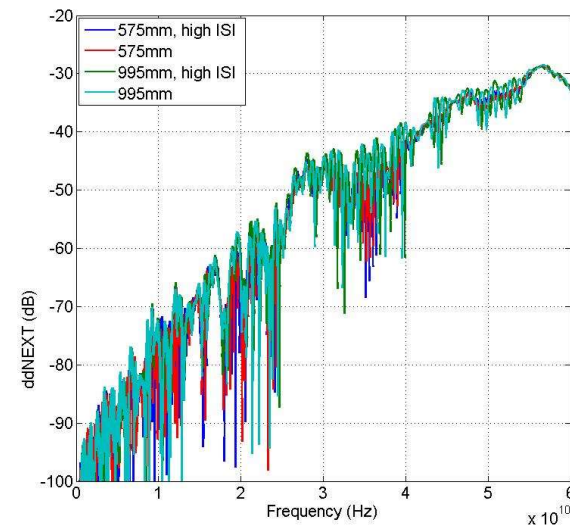
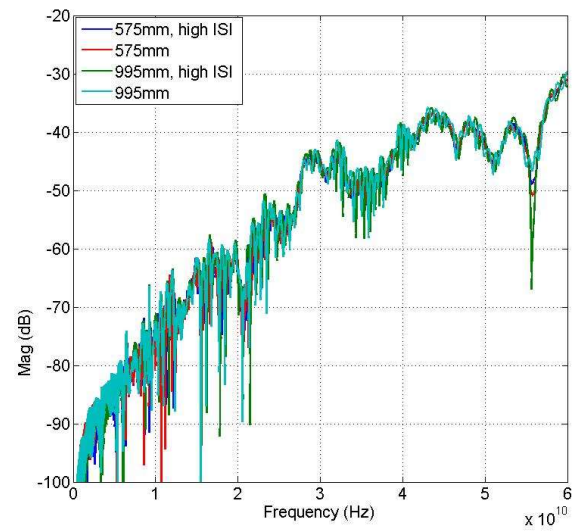
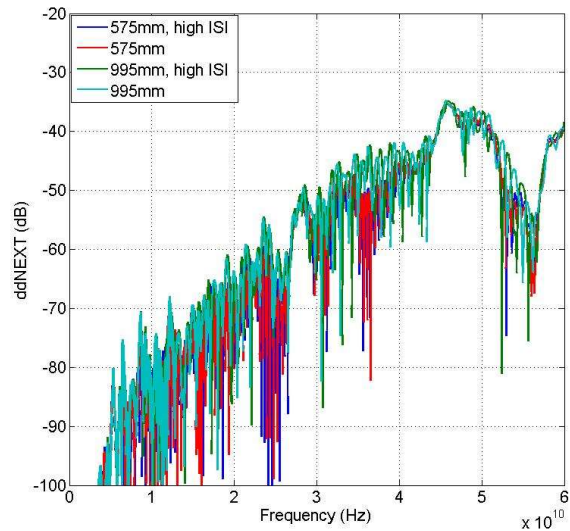


NEXT Response

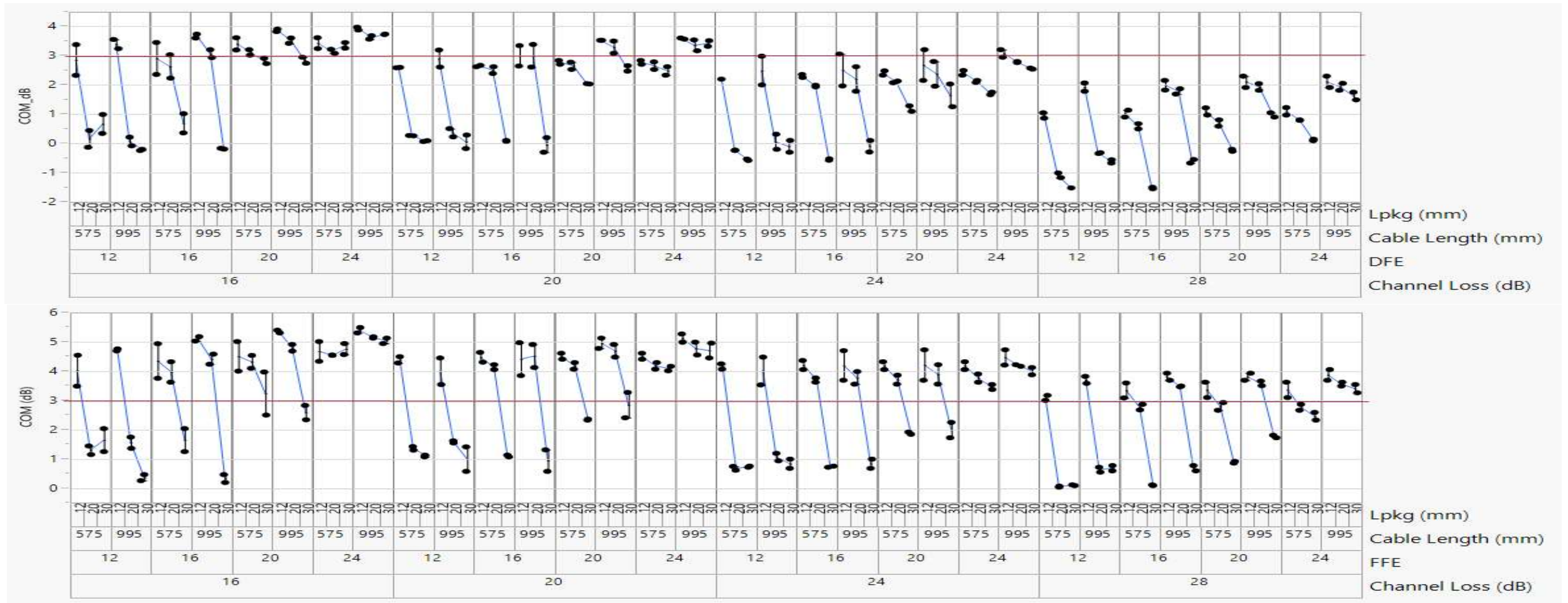
20dB



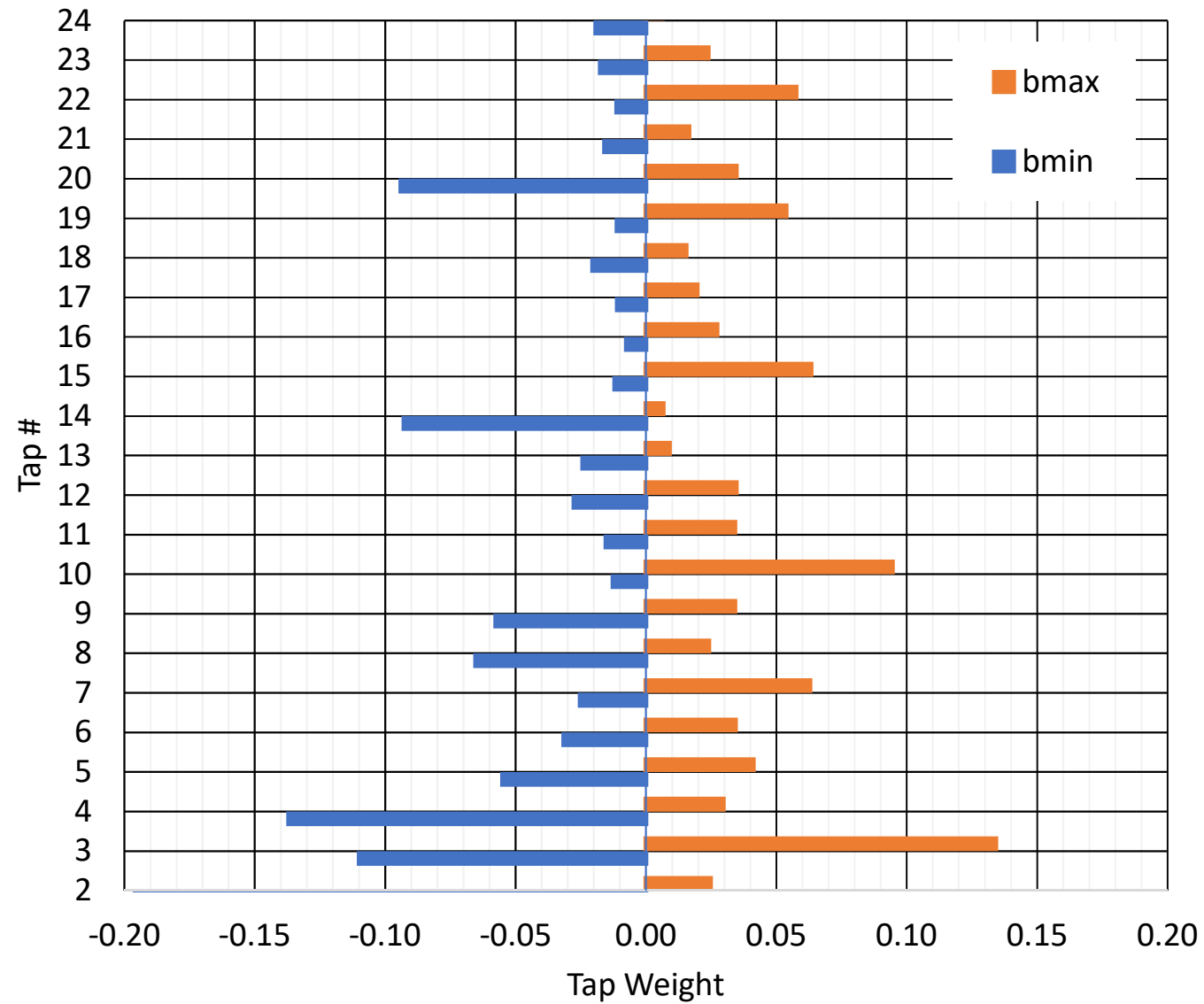
24dB



DFE/FFE Comparison



DFE Tap Weights



Tap 1: 0.66-0.7