IEEE P802.3ck
Channel Models for 100 Gb/s, 200Gb/s, 400 Gb/s C2C AUI

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May 2019, Salt Lake City, Utah

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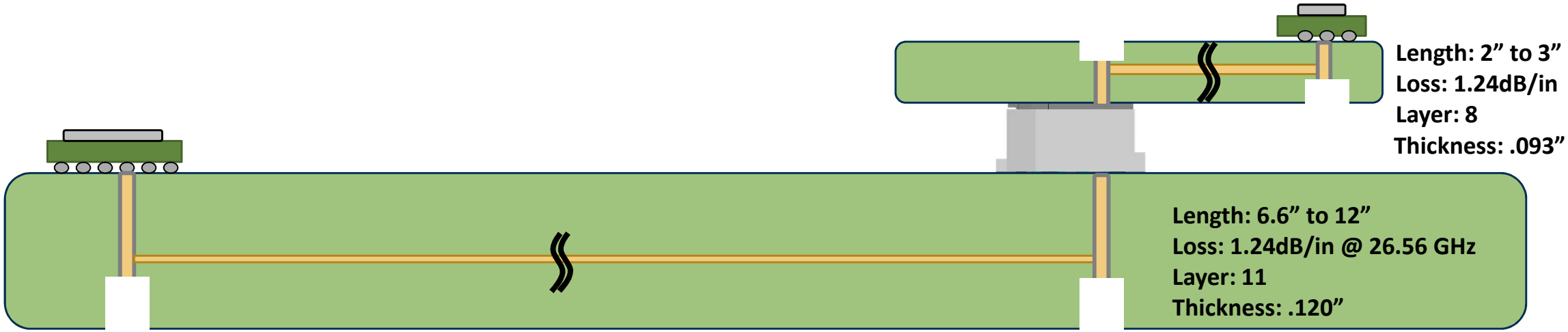
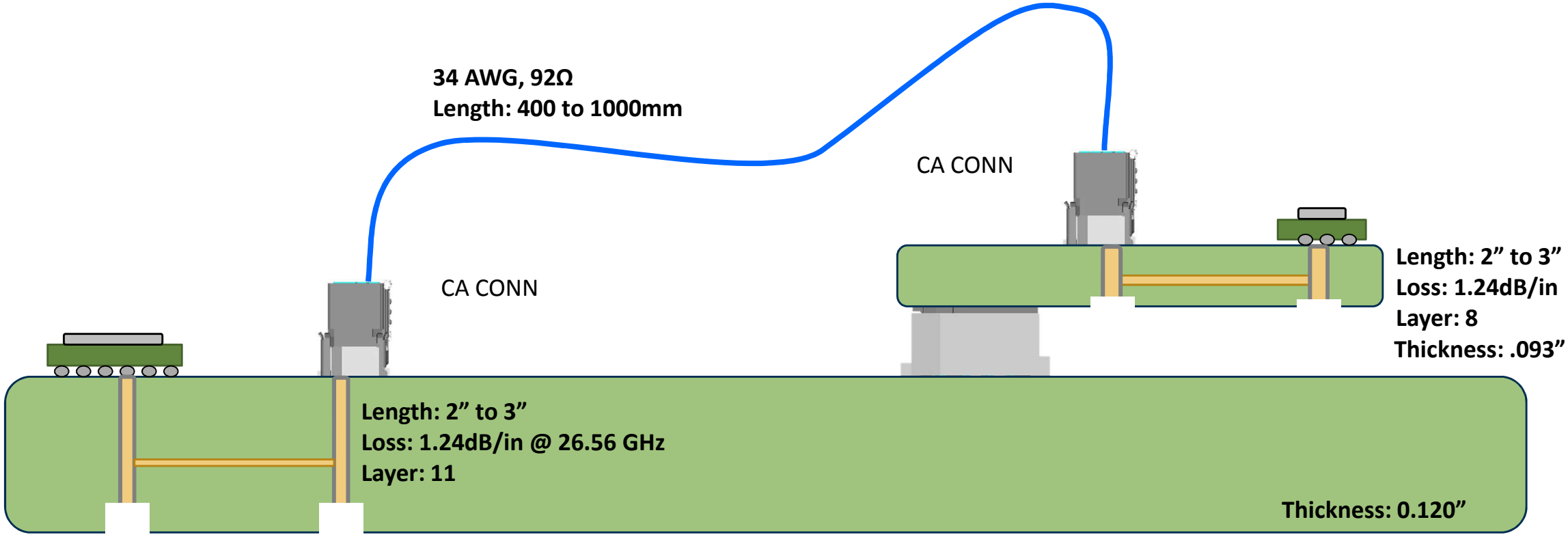
Channel Model Overview

- Both Cabled and PCB C2C Topologies
  - TP0 to TP5 loss targets: 20dB, 18dB, 16dB, 14dB, 12dB @ 26.56 GHz
- Synthesized models with pieces calibrated to measurements
- Nominal design. Manufacturing tolerance and DC blocking capacitor in future contribution.
- Includes BGA and Connector breakout footprint from system implementation
  - Routing on Layer 11 (host board) and Layer 8 (mezzanine)
- Via stub length is 8 mil nominal from back drill
- Transmission line loss of 1.24dB/in @ 26.56 GHz
  - Megtron6-like material with trace width of 6 mil and intra-pair pitch of 14 mil

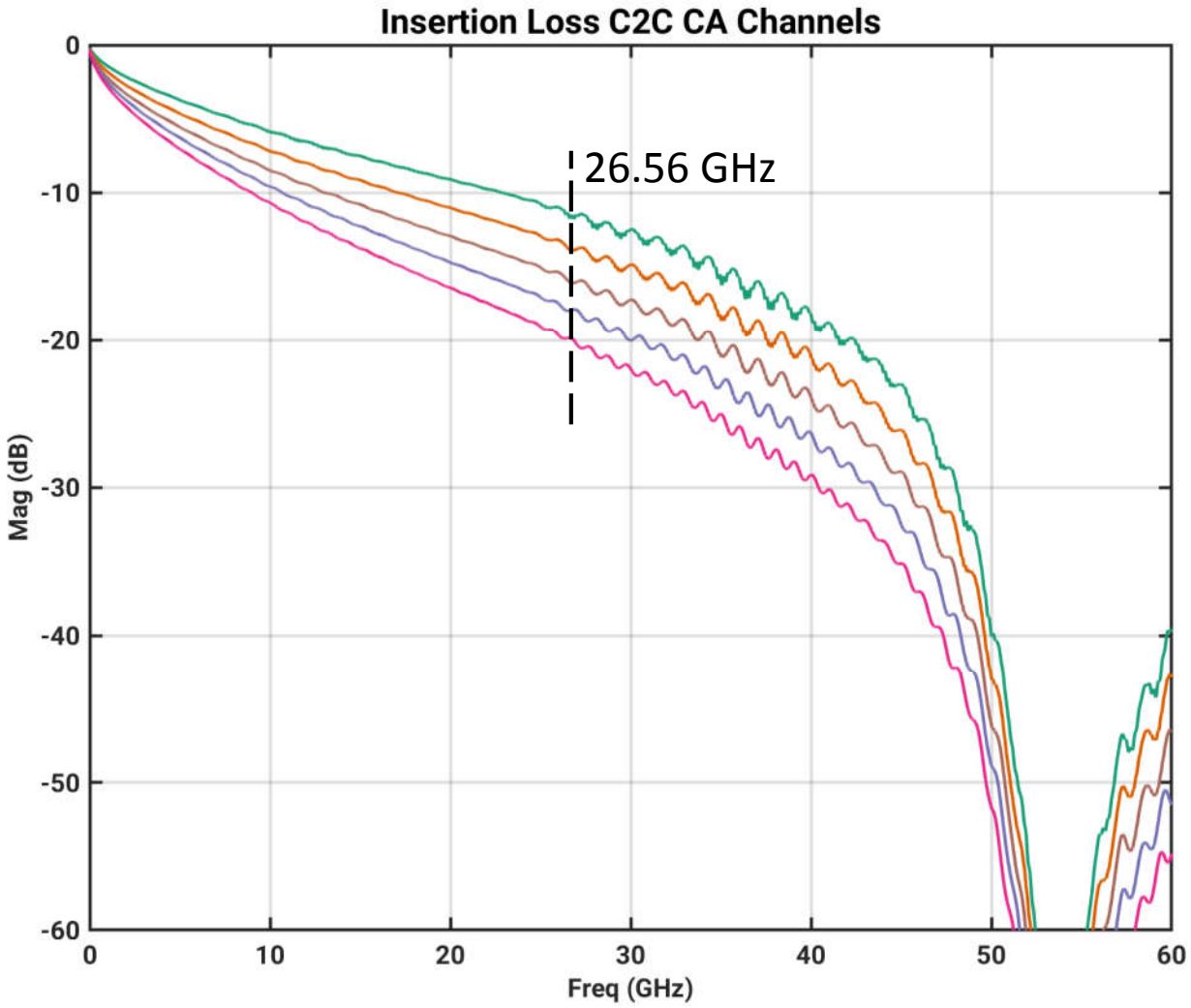
PCB C2C System

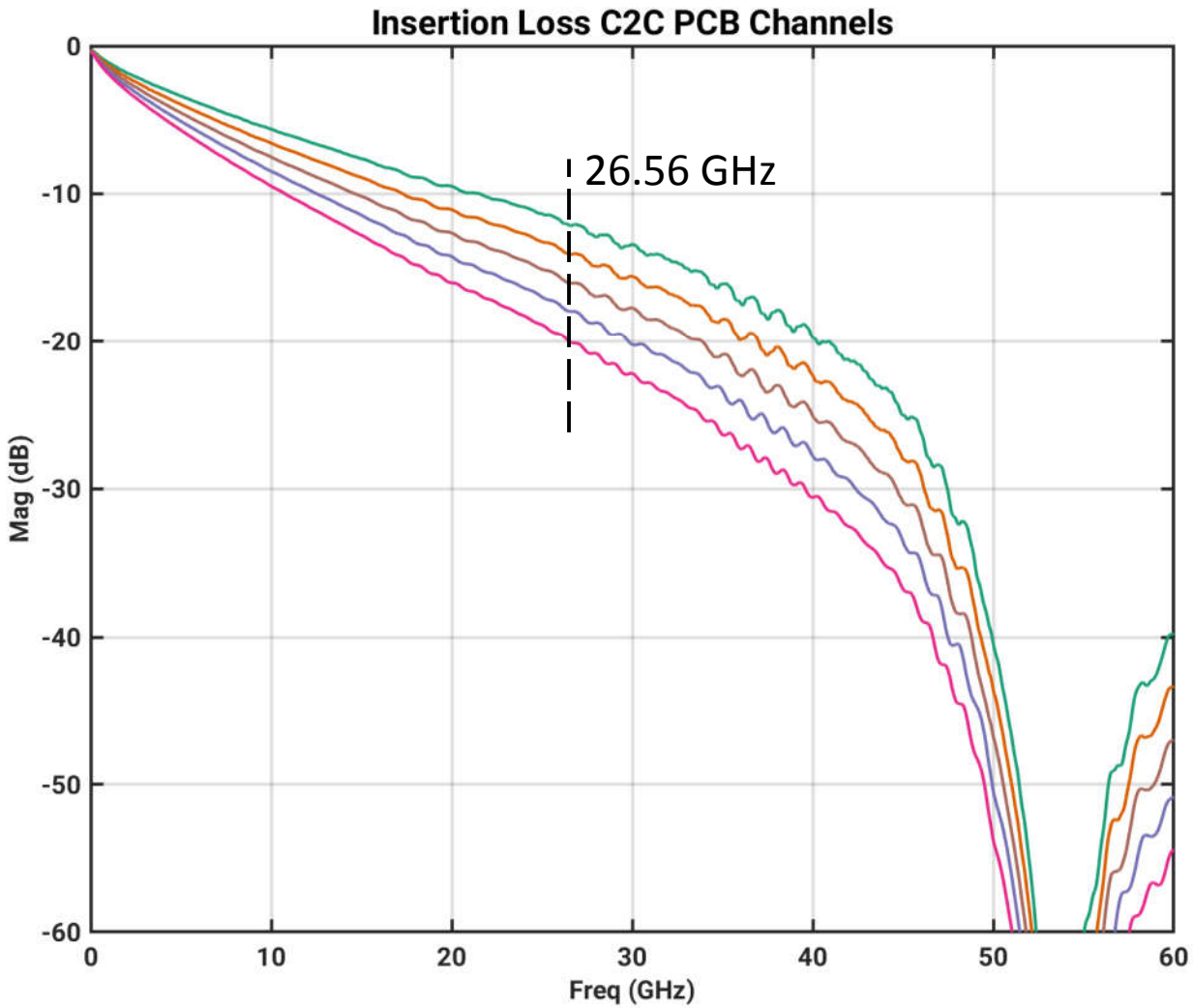


Cabled C2C System

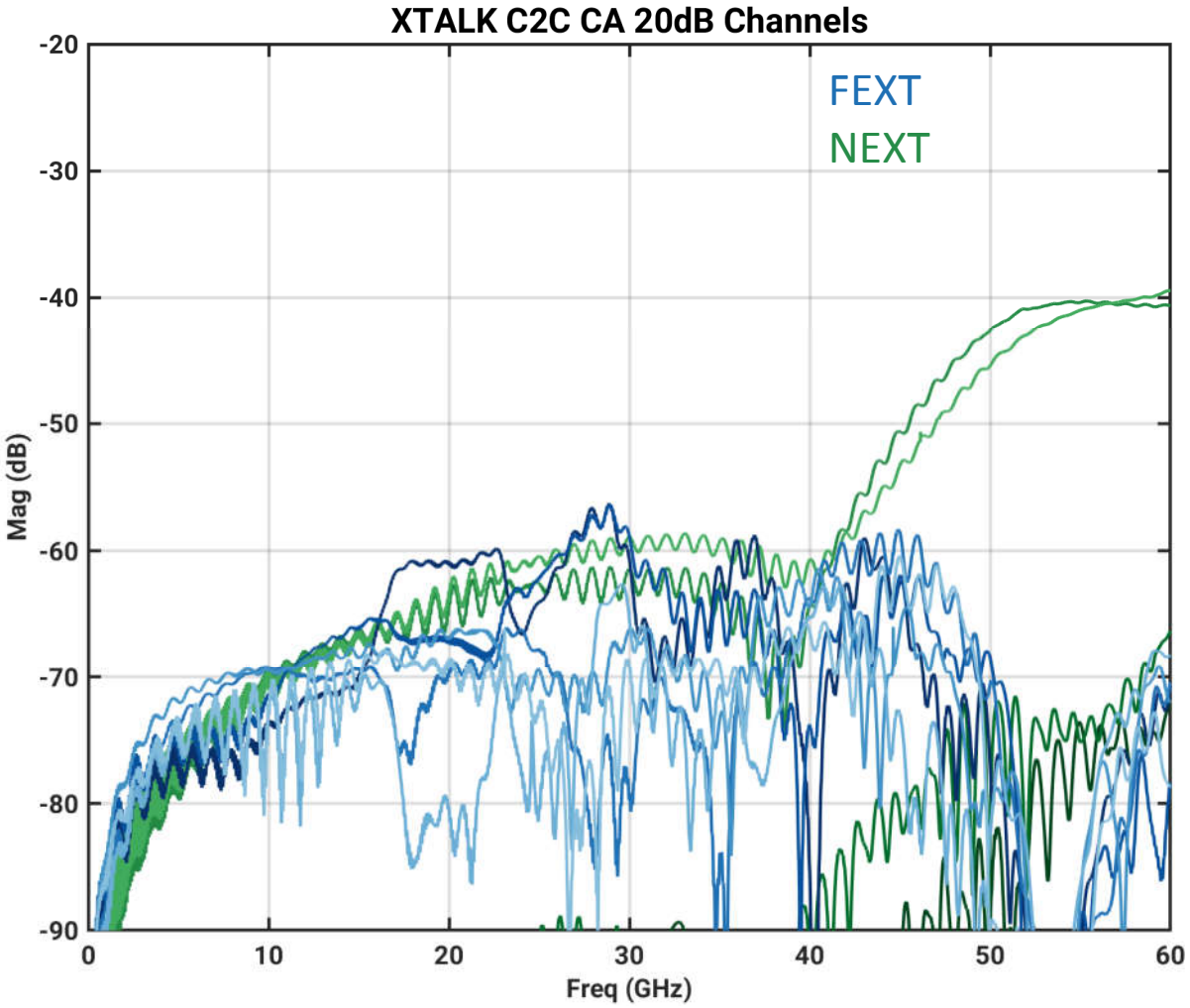


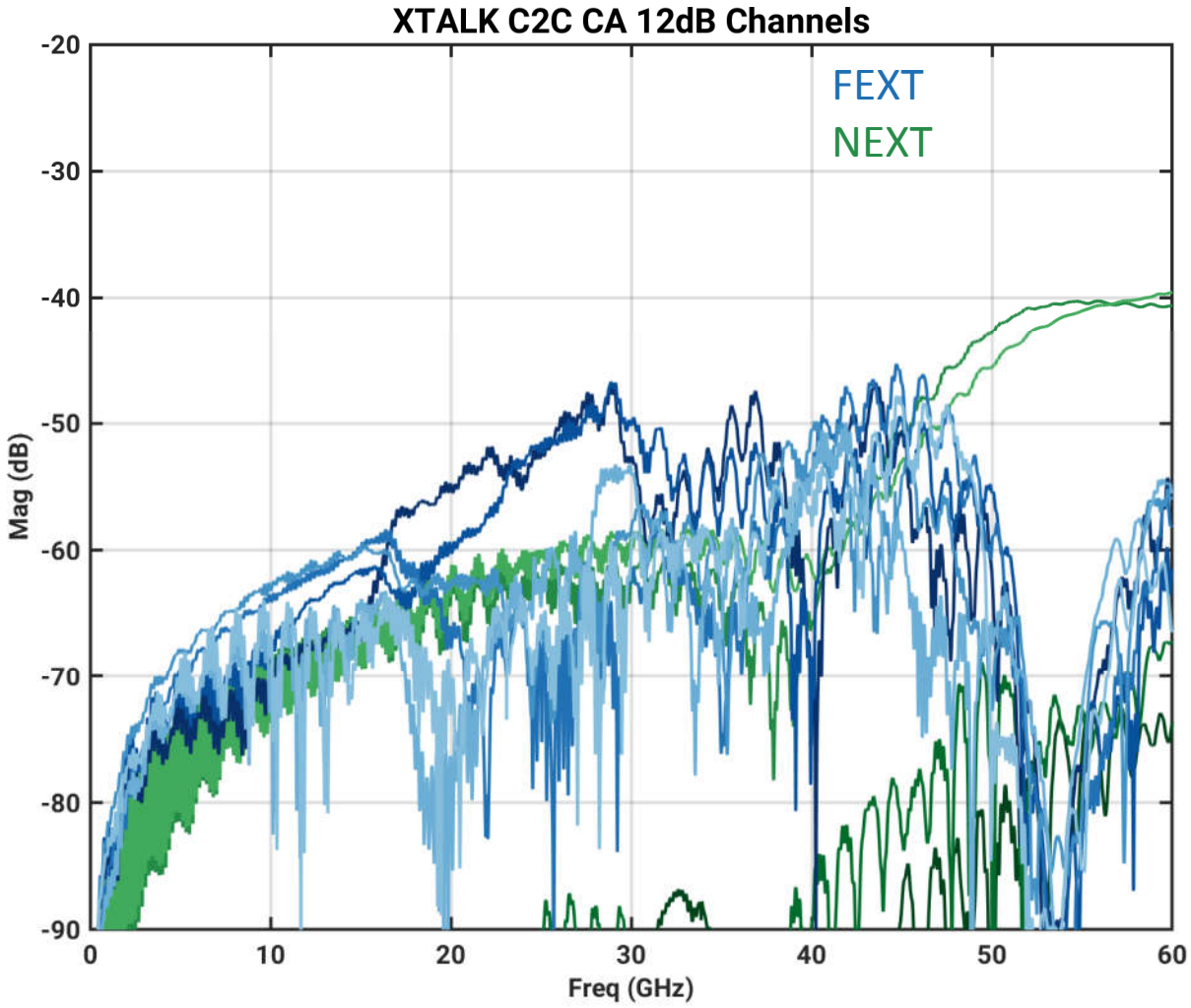
Differential IL Target 12dB to 20dB @ 26.56dB



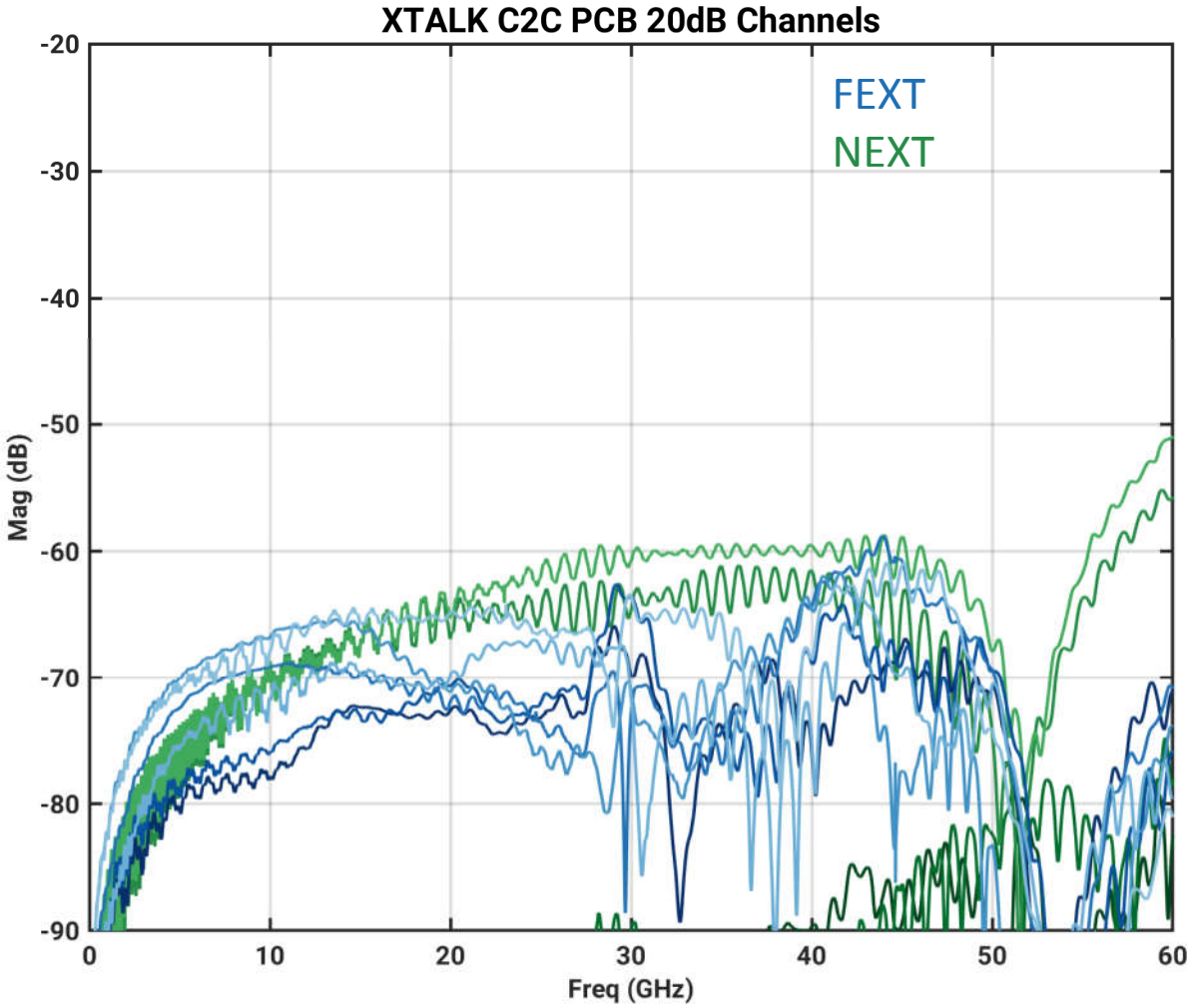


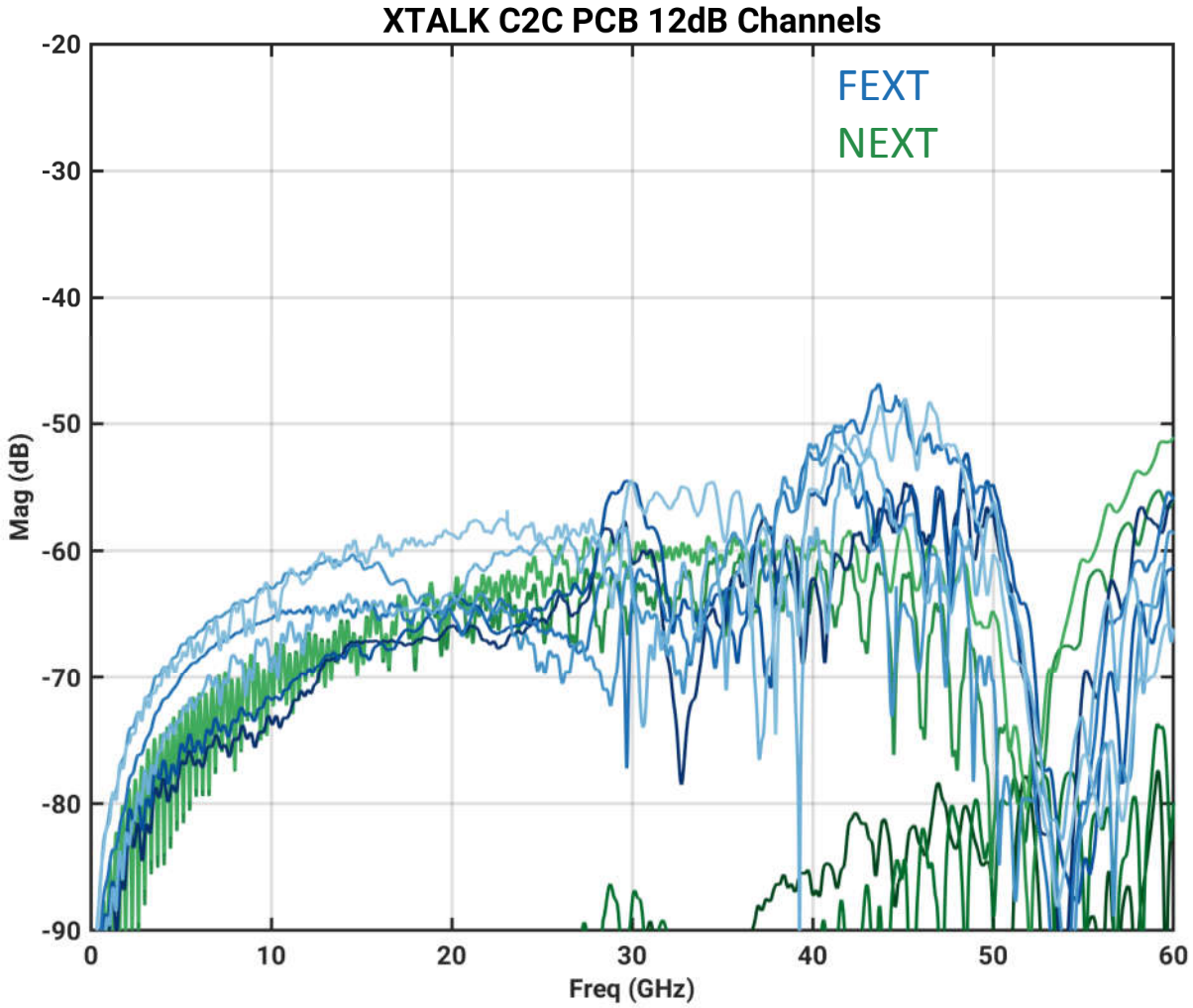
Far-End and Near-End Crosstalk (Cabled System)





Far-End and Near-End Crosstalk (PCB System)





Channel Analysis

Channel	COM(dB)**	IL (dB) Channel Only @ 26.56GHz	MDNEXT ICN (mV)	MDFEXT ICN (mV)	ICN (mV)	ERL (dB)
C2C_CA_CONN_20dB	3.43	19.85	0.42	0.35	0.546	18.50
C2C_CA_CONN_18dB	3.68	17.96	0.42	0.44	0.603	17.92
C2C_CA_CONN_16dB	3.76	15.94	0.42	0.54	0.685	17.36
C2C_CA_CONN_14dB	3.73	13.81	0.42	0.69	0.808	16.97
C2C_CA_CONN_12dB	3.90	11.58	0.42	0.87	0.966	16.45
C2C_PCB_CONN_20dB	3.78	20.08	0.38	0.29	0.477	18.65
C2C_PCB_CONN_18dB	4.04	17.95	0.38	0.34	0.513	17.97
C2C_PCB_CONN_16dB	4.21	16.03	0.38	0.41	0.559	17.50
C2C_PCB_CONN_14dB	4.32	14.09	0.38	0.49	0.620	17.44
C2C_PCB_CONN_12dB	4.31	12.17	0.39	0.59	0.702	17.37

**Results verified in COM 2.6

Summary

- 20dB C2C topologies are feasible with a subset of KR capability
- Both Cable and PCB based channels are provided for several loss targets
- These are nominal design targets. Manufacturing tolerance and DC blocking capacitor in a future contribution.

Backup

C2C COM parameters used as an example for analysis in this presentation

Table 93A-1 parameters		
Parameter	**Setting**	**Units**
f_b	53.125	GBd
f_min	0.05	GHz
Delta_f	0.01	GHz
C_d	[1.1e-4 1.1e-4]	nF
z_p select	[1 2]	
z_p (TX)	[12 32; 1.8 1.8]	mm
z_p (NEXT)	[12 32; 1.8 1.8]	mm
z_p (FEXT)	[12 32; 1.8 1.8]	mm
z_p (RX)	[12 32; 1.8 1.8]	mm
C_p	[0.87e-4 0.87e-4]	nF
R_0	50	Ohm
R_d	[50 50]	Ohm
A_v	0.413	V
A_fe	0.413	V
A_ne	0.608	V
L	4	
M	32	
filter and Eq		
f_r	0.75	*fb
c(0)	0.54	
c(-1)	[-0.34:0.02:0]	
c(-2)	[0:0.02:0.12]	
c(-3)	0	
c(1)	[-0.2:0.05:0]	
N_b	12	UI
b_max(1)	0.85	
b_max(2..N_b)	0.3	
g_DC	[-12:1:0]	dB
f_z	21.25	GHz
f_p1	21.25	GHz
f_p2	53.125	GHz
g_DC_HP	[-6:1:0]	
f_HP_PZ	0.6640625	GHz

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	32.5	dB
R_LM	0.95	

Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical