100G C2C-S Channel Estimate

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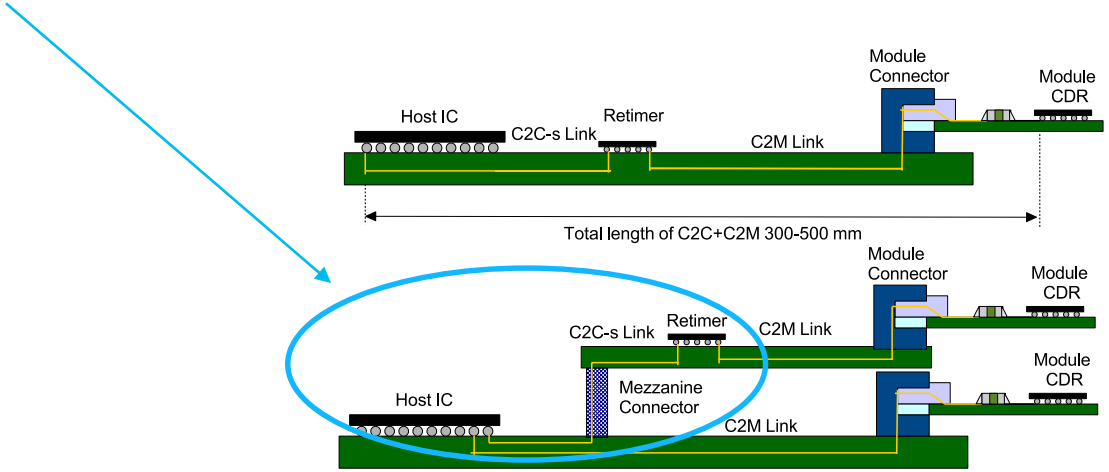
Scope

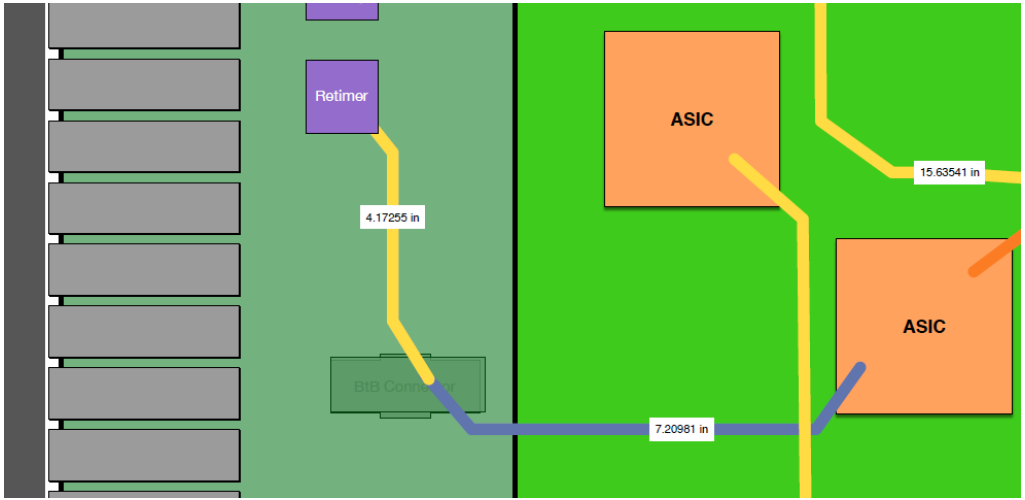
- Study front port channel C2C-S loss requirement & channel characteristics for next generation 100GEL optical and DAC links
  - Overall IL target should allow reasonable trace length from host ASIC sitting on the main board to the retimer on the daughter card



Picture source: http://www.ieee802.org/3/ck/public/19_05/ghiasi_3ck_02_0519.pdf

PCB Trace Length Estimate

- ASIC <-> Connector trace length, min= 3.3”, max=7.2”
- Connector <-> Retimer trace length, min=2.5”, max=4.2”
- Total PCB trace loss, 7.3dB – 14.4dB @ 26.56 GHz (Assume Meg7N material, 1.26dB/in)



Package & Connector Loss Estimate

- Retimer package:
  - FC-PBGA, 8-10 layer stackup, 400um core
  - Trace length, 4mm – 16mm, max. IL ~2dB @ 26.56 GHz
- ASIC package:
  - Follow KR/CR package baseline, max. IL ~4dB @ 26.56 GHz
- Mezzannie connector:
  - Connector + 2 sets of vias, max IL ~2.5dB @ 26.56 GHz

C2C-S Channel Loss Breakdown

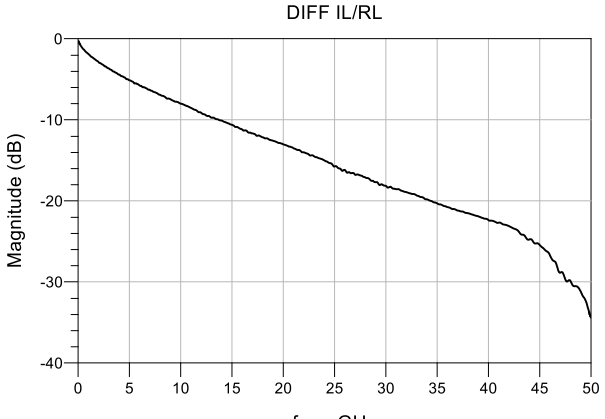
	Best case IL, dB @ 26.56 GHz	Worst case IL, dB @ 26.56 GHz
Host PCB	7.3	14.4
Connector + via	1.5	2.5
ASIC package	2.0	4.0
Retimer package	0.6	2.0
Ball-to-ball	8.8	16.9
Bump-to-bump	11.4	22.9

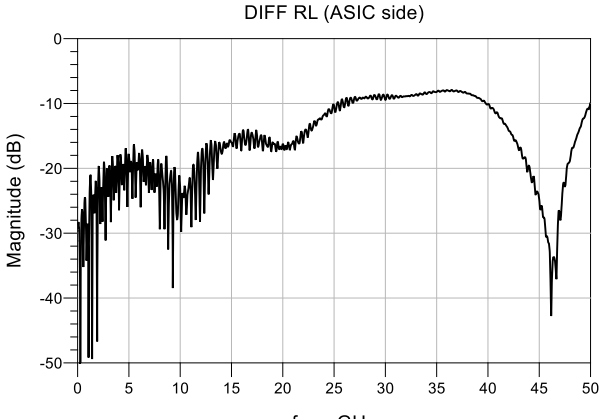
C2C-S Channels (Host ASIC to Retimer Direction)

- Total 4 channels were built with optimized host ASIC, retimer & mezzanine connector footprint (shallow via breakout). Both shallow and long via are considered at connector and retimer footprint.
  - Channel 1: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (shallow via breakout) + daughtercard trace 4” + Retimer footprint (shallow via) ; including 2 FEXT & 2 NEXT
  - Channel 2: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (shallow via breakout) + daughtercard trace 4” + Retimer footprint (long via); including 2 FEXT & 2 NEXT
  - Channel 3: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (long via breakout) + daughtercard trace 4” + Retimer footprint (shallow via) ; including 2 FEXT & 2 NEXT
  - Channel 4: ASIC BGA footprint (mid via – L17) TX + host trace 7” + Mezzanine footprint & connector (long via breakout) + daughtercard trace 4” + Retimer footprint (long via) ; including 2 FEXT & 2 NEXT

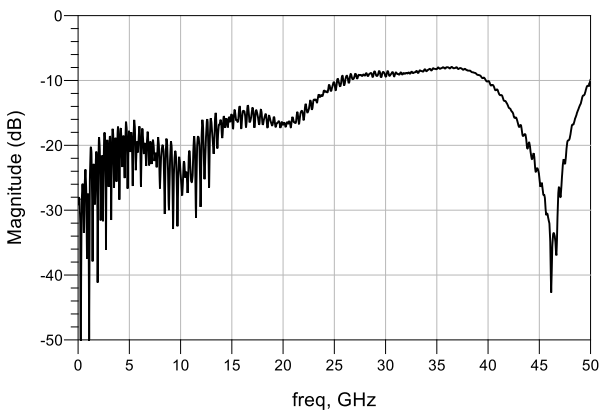
Channel 1/2: Insertion Loss, Return Loss

Channel 1



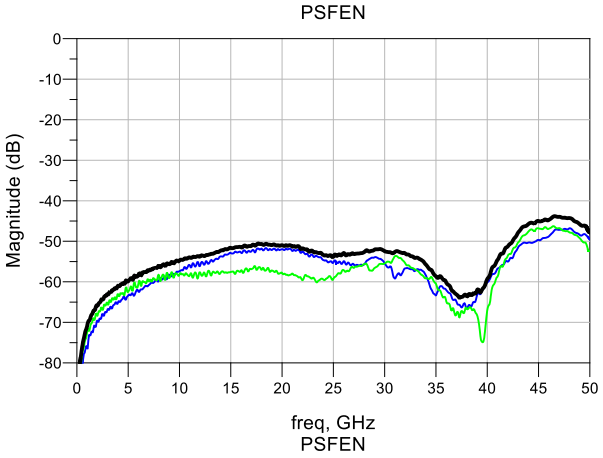


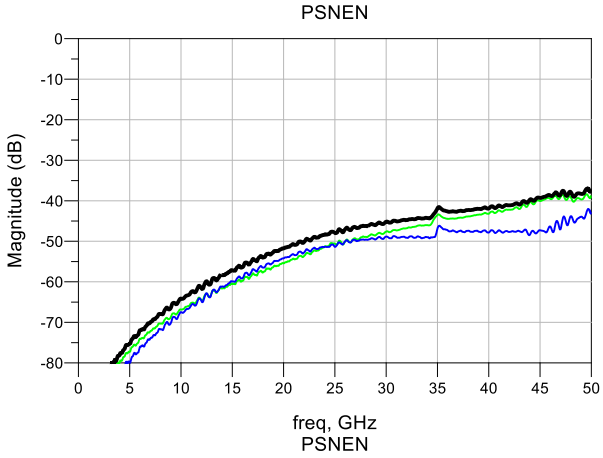
Channel 2



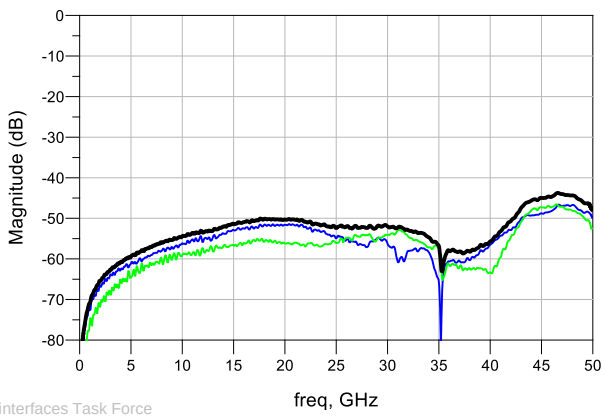
Channel 1/2: Far-end and Near-end Crosstalk

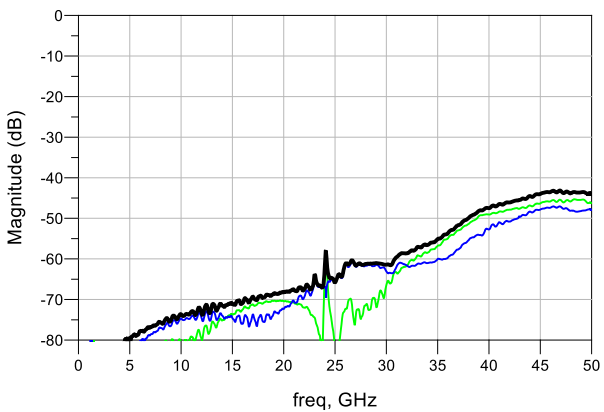
Channel 1





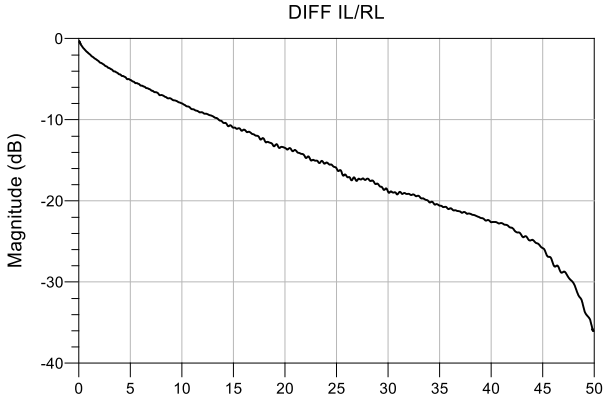
Channel 2

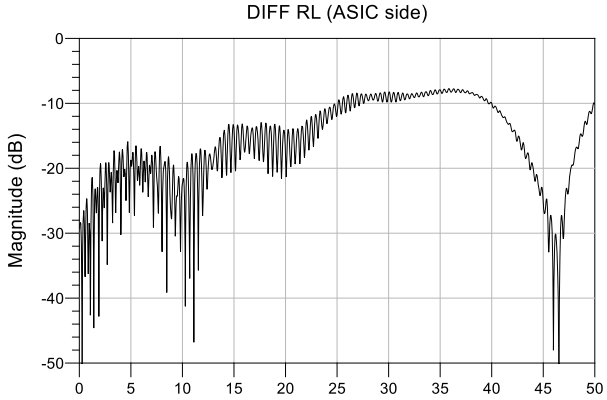




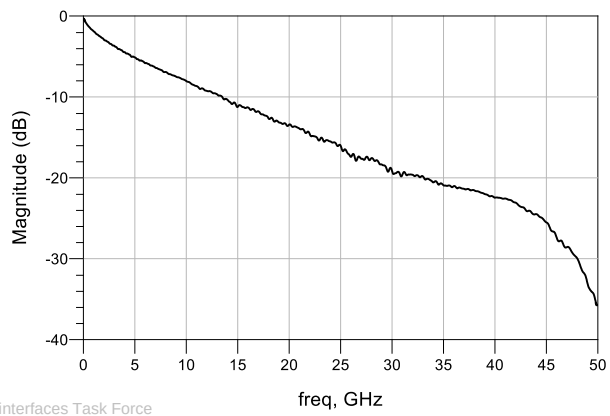
Channel 3/4: Insertion Loss, Return Loss

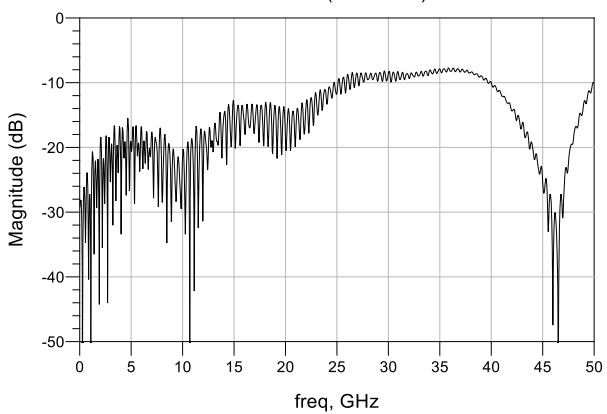
Channel 3





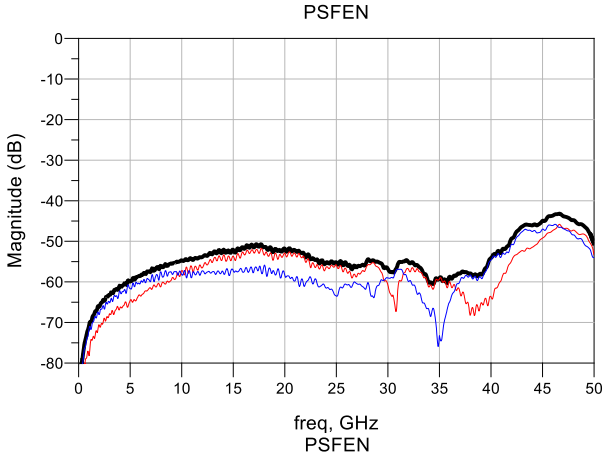
Channel 4

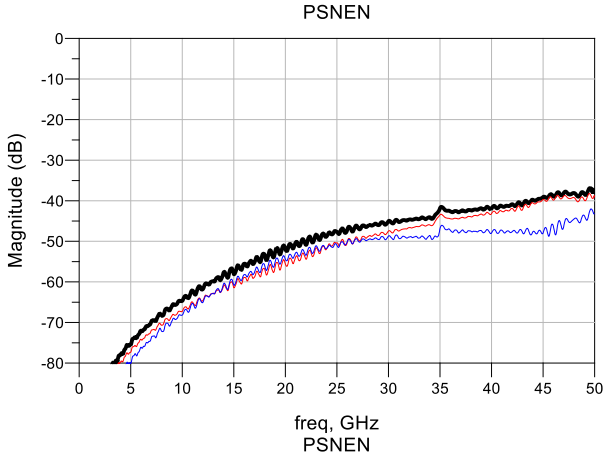




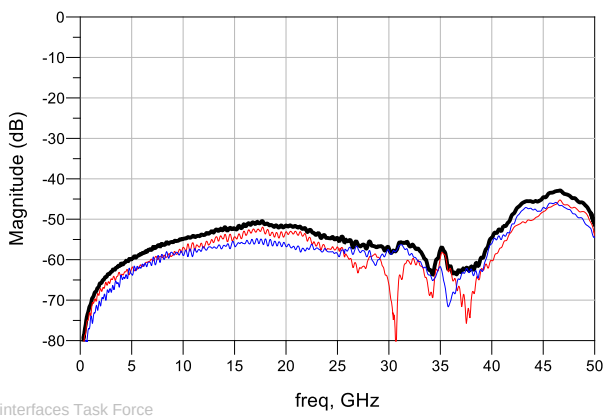
Channel 3/4: Far-end and Near-end Crosstalk

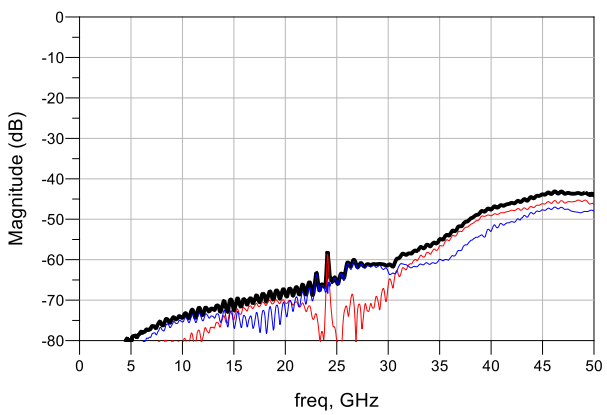
Channel 3





Channel 4





C2C-S COM Results, – 2 Ref. Rx (A & B)

DUT	COM TX15mm/RX4mm (dB)	COM TX30mm/RX16mm (dB)	ERL11 (dB)	ERL22 (dB)	ICN (mV)	FOM_{ILD} (dBrms)	IL@26G b2b (dB)
Channel 1 Ref Rec. A	4.29	3.21	20.79	18.27	1.58	0.07	16.5
Channel 1 Ref Rec. B	4.19	3.01	20.79	18.27	1.58	0.07	16.5
Channel 2 Ref Rec A	4.15	3.45	20.55	18.01	0.85	0.11	16.8
Channel 2 Ref Rec B	3.28	2.79	20.55	18.01	0.85	0.11	16.8
Channel 3 Ref Rec. A	3.40	2.81	18.96	15.79	1.56	0.11	17.3
Channel 3 Ref Rec. B	3.40	2.73	18.96	15.79	1.56	0.11	17.3
Channel 4 Ref Rec A	3.41	2.96	18.79	15.60	0.76	0.14	17.7
Channel 4 Ref Rec B	2.78	2.48	18.79	15.60	0.76	0.14	17.7

Ref Rec. A = with 4DFE; Ref Rec. B = with 5FFE + 1DFE, as listed in sun_3ck_01_0519
Use COM script 2.70

Summary

- End-to-end C2C-S channels are estimated to be around 16-18 dB at 26.56 GHz
- Worst case channels with long via at Mezzanine connector footprint can’t pass 3dB COM with the ref. receivers currently in consideration for C2M
- Channels with shallow via at Retimer footprint has worse ICN due to stronger Tx to Rx crosstalk

Next Steps

- Build the C2C-S channels at the reverse direction – Retimer to Host ASIC
- Analyze the channel in COM using stronger reference receivers with > 5 DFE taps

Backup slides

Reference Receiver A

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[15 30 ; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[4 16 ; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[15 30 ; 1.8 1.8]	mm	[test cases]
z_p (RX)	[4 16 ; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[-0.04:.02:0.0]		[min:step:max]
c(-3)	00:00.0		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	4	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-20:0.5:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	0	UI	
ffe_tap_step_size	0		
ffe_main_cursor_mir	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	**0.25**	
fixture delay time	0	s
TDR_W_TXPKG	1	
N_bx	24	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

Table 92–12 parameters 5.2dB at 26.56GHz		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 0.000599 0.0001022]*	1.286 dB/in or 0.0506 dB/mm at 100 ohms
board_tl_tau	*6.200E-03*	ns/mm
board_Z_c	90	Ohm
z_bp (TX)	*102.7*	mm
z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**0**	**0 1 2 or 3 groups**
N_bf	*0*	taps per group
N_f	20	UI span for floating taps
bmaxg	0.1	max DFE value for floating taps

yellow indicates WIP

Reference Receiver B

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[15 30 ; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[4 16 ; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[15 30 ; 1.8 1.8]	mm	[test cases]
z_p (RX)	[4 16 ; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.39	V	vp/vf=.694
A_fe	0.39	V	vp/vf=.694
A_ne	0.578	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.6		min
c(-1)	[-0.3:0.02:0]		[min:step:max]
c(-2)	[-0.04:.02:0.0]		[min:step:max]
c(-3)	00:00.0		[min:step:max]
c(1)	[-0.1:0.05:0]		[min:step:max]
N_b	1	UI	
b_max(1)	0.5		
b_max(2..N_b)	0.2		
g_DC	[-20:0.5:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	
ffe_pre_tap_len	0	UI	
ffe_post_tap_len	4	UI	
ffe_tap_step_size	0		
ffe_main_cursor_mir	0.7		
ffe_pre_tap1_max	0.3		
ffe_post_tap1_max	0.3		
ffe_tapn_max	0.125		
ffe_backoff	0		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_KR_{date}\	
SAVE_FIGURES	1	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-05	
T_r	6.16E-03	ns
FORCE_TR	1	logical
Include PCB	0	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.53E+09	
rho_x	**0.25**	
fixture delay time	0	s
TDR_W_TXPKG	1	
N_bx	24	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

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z_bp (NEXT)	*102.7*	mm
z_bp (FEXT)	*102.7*	mm
z_bp (RX)	*102.7*	mm

Floating Tap Control		
N_bg	**0**	**0 1 2 or 3 groups**
N_bf	*0*	taps per group
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