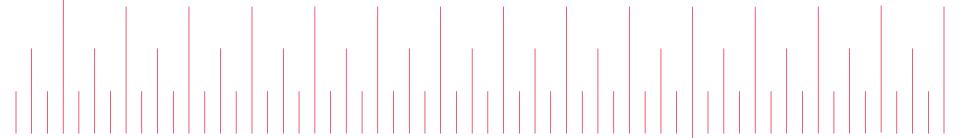
July 10th, 2019

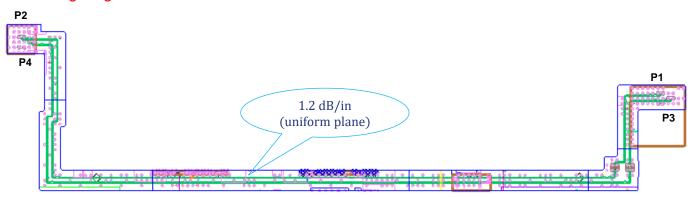


Rick Rabinovich



Example Channel with Impairments (Obstacles)

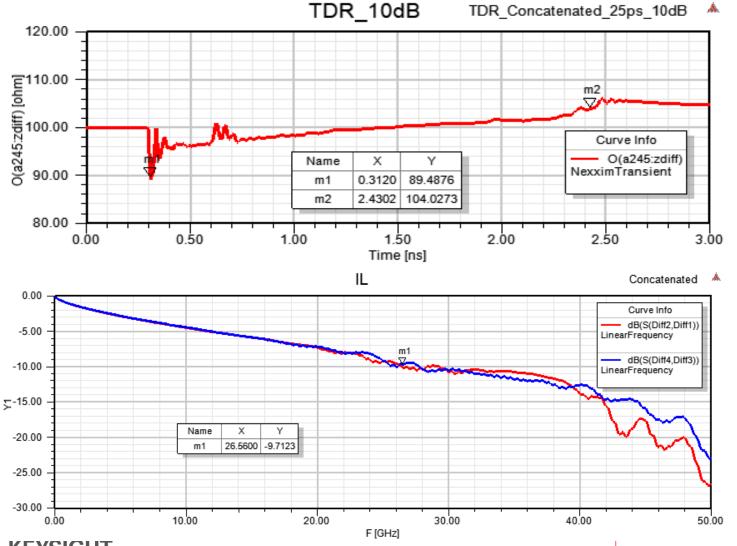
- 10 dB C2C channel
- Two-channel adaptation with AC coupling (~ connector)
- Dielectric similar to Megtron 7 (6.75" long)
- "Engineered" Channel
- Impairments:
 - Impedance tolerance
 - \sim Z_{nom} \sim 94 ohms
 - ASIC breakout
 - Long and short via stripline mix
 - 105 mils (0.5 dB/via)
 - 22 mils (0.4 dB/via)
 - Six 90° turns
 - Asymmetric via distribution along the route
 - · Routing on grid



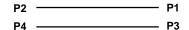


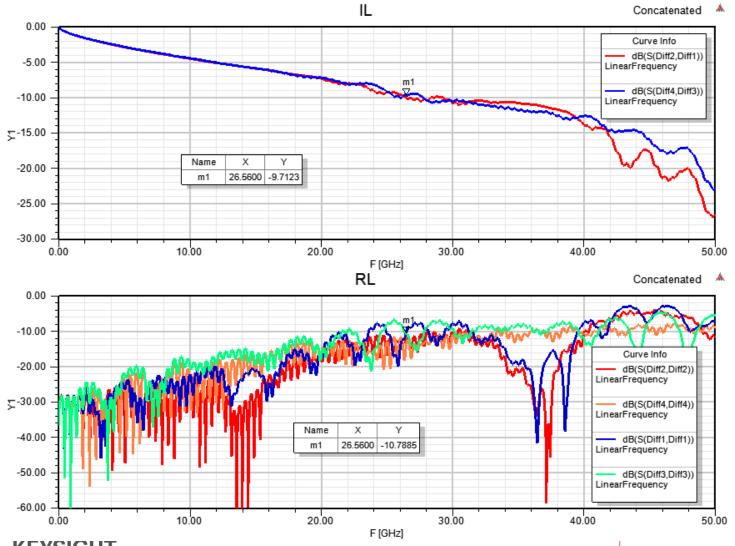
TDR – Engineered Channel



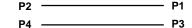


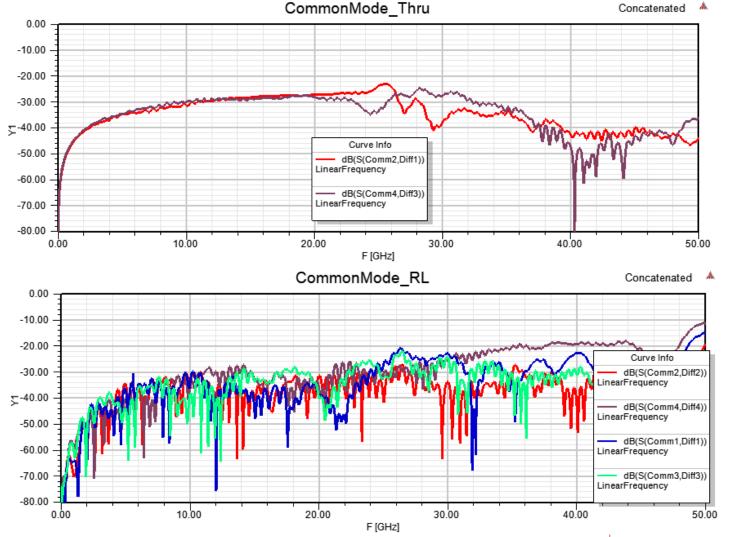






Common Mode Conversion

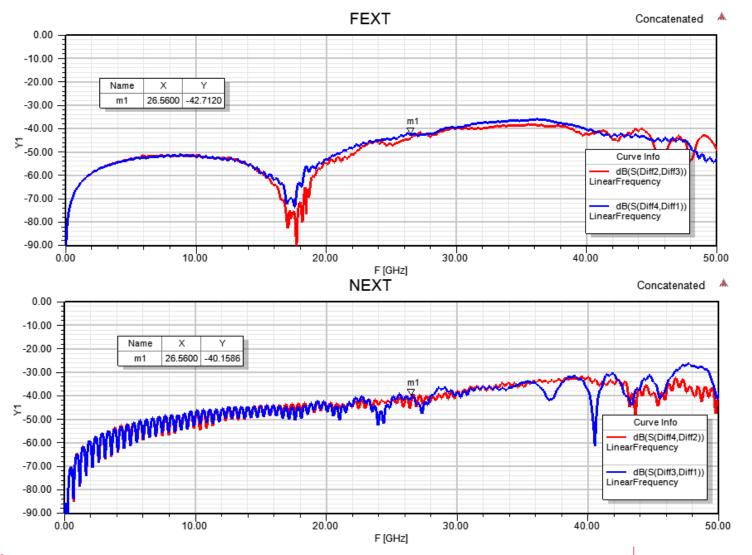






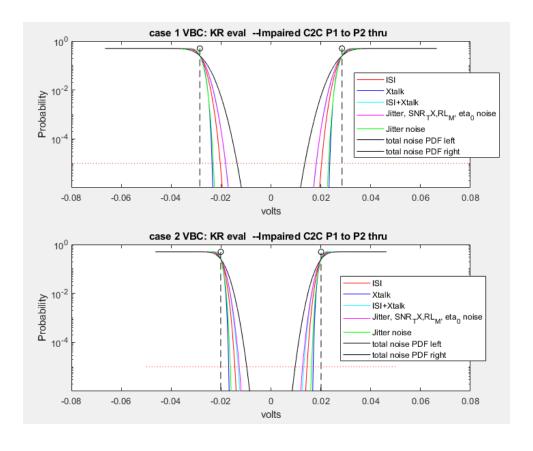








COM C2C rev. 2.7 Results

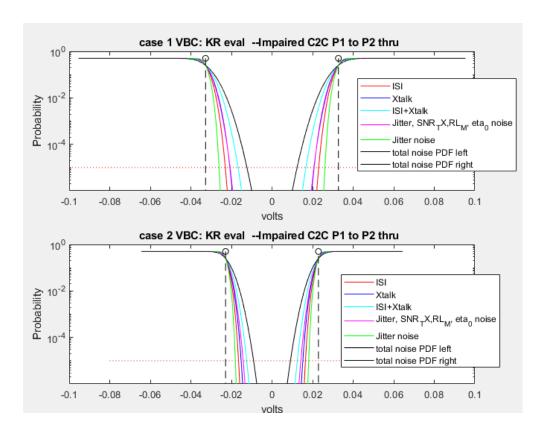


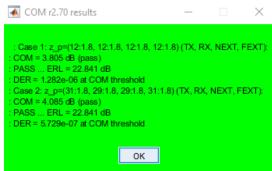


1 FEXT, 1 NEXT



COM C2C rev. 2.7 Results





3 FEXT, 4 NEXT



Q&A



C2C Channel With Impairments COM C2C Configuration Sheet

Table 93A-1 parameters				I/O control			Table 93A–3 parameters		
Parameter	Setting	Units	Information	DIAGNOSTICS	1	logical	Parameter	Setting	Units
f_b	53.125	GBd		DISPLAY_WINDOW	1	logical	package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
f_min	0.05	GHz		CSV_REPORT	1	logical	package_tl_tau	6.141E-03	ns/mm
Delta_f	0.01	GHz		RESULT_DIR	.\results\100GEL_	KR_{date}\	package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]	SAVE_FIGURES	1	logical			
L_s	[0.12, 0.12]	nH	[TX RX]	Port Order	[2143]		Table 92–12 parameters 5.2dB at 26.56GHz		
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]	RUNTAG	KR_eval_		Parameter	Setting	
z_p select	z_p select [12] [test cases to ru		[test cases to run]	COM_CONTRIBUTION	0	logical	board_tl_gamma0_a1_a2	[0 0.000599 0.0001022]	1.286 dB/in or 0.0506 dB/mm at 100 ohms
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]	Operational		board_tl_tau	6.200E-03	ns/mm	
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]	COM Pass threshold	3	dB	board_Z_c	90	Ohm
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	10	dB	z_bp (TX)	102.7	mm
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]	DER_0	1.00E-05		z_bp (NEXT)	102.7	mm
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]	T_r	6.16E-03	ns	z_bp (FEXT)	102.7	mm
R_0	50	Ohm		FORCE_TR	1	logical	z_bp (RX)	102.7	mm
R_d	[45 45]	Ohm	[TX RX]	Include PCB	0	logical			
A_v	0.39	V	vp/vf=.694		nd ERL options				
A_fe	0.39	V	vp/vf=.694	TDR	1	logical	Floating Tap Control		
A_ne	0.578	V		ERL	1	logical	N_bg	0	0 1 2 or 3 groups
L	4			ERL_ONLY	0	logical	N_bf	4	taps per group
M	32			TR_TDR	0.01	ns	N_f	40	UI span for floating taps
filter and Eq				N	3000		bmaxg	0.1	max DFE value for floating taps
f_r	0.75	*fb		beta_x	2.53E+09				
c(0)	0.5		min	rho_x	0.25				
c(-1)	[-0.3:0.02:0]		[min:step:max]	fixture delay time	0	5			
c(-2)	[0:0.02:0.12]		[min:step:max]	TDR_W_TXPKG	0				
c(-3)	[-0.06:0.02: 0]		[min:step:max]	N_bx	24	UI	yellow indicates WIP		
c(1)	[-0.2:0.05:0]		[min:step:max]	Recei	Receiver testing				
N_b	12	UI		RX_CALIBRATION	0	logical			
b_max(1)	0.85			Sigma BBN step	5.00E-03	V			
b_max(2N_b)	0.3			Noise, jitter					
g_DC	[-20:1:0]	dB	[min:step:max]	sigma_RJ	0.01	UI			
f_z	21.25	GHz		A_DD	0.02	UI			
f_p1	21.25	GHz		eta_0	8.20E-09	V^2/GHz			
f_p2	53.125	GHz		SNR_TX	33	dB			
g_DC_HP	[-6:1:0]		[min:step:max]	R_LM	0.95				
f HP PZ	0.6640625	GHz							

