“Inverse RS-FEC” vs. IFEC terminology, ref. comment I-8

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Clause 152 derives from Clause 91 and follows the same general pattern

- In the text of the clause 91, “RS-FEC” is generally used when referring to the sublayer, and “FEC” is used when referring to the service interface:
  - Example: FEC:IS_UNITDATA_*i*.request
  - Clause 153 SC-FEC uses essentially the same service interface as clause 91 RS-FEC. The service interface does not change based on the algorithm used within the sublayer to calculate the FEC parity
- Similarly in Clause 152 text, “Inverse RS-FEC” is generally used when referring to the sublayer, and “IFEC” is generally used when referring to the service interface.
  - Example: IFEC:IS_UNITDATA_*i*.request
- Propose not to change this convention within the text

Control and status registers and MDIO variable names

- The apparent intention in the register and variable naming in Tables 91-2 and 91-3 was to use “FEC” for any control or status register that arguably could apply to any FEC code (e.g., corrected/uncorrected codewords, lane lock, lane mapping), while using “RS-FEC” for a control or status register that would be specific to this FEC code. But if this was the intention, the rule has been unevenly applied, with two notable exceptions:
  - RS-FEC align status instead of FEC align status (note that the clause internal register is fec_align_status)
  - FEC optional states supported instead of RS-FEC optional states supported (given that this was a bug fix, presumably the original mistake would not be replicated
  - Some minor inconsistencies between PCS/PMA register names and MDIO variable names
- Clause 152 blindly used “Inverse RS-FEC” wherever clause 91 used “RS-FEC”, and blindly used “IFEC” wherever clause 91 used “FEC” in PCS/PMA and MDIO variable names

Current Clause 152 Variable Names

Follows the pattern of clause 91, retaining the same degree of inconsistency

Table 152-1			
IFEC bypass correction enable	Inverse RS-FEC control	1.2200.0	FEC_bypass_correction_enable
IFEC bypass indication enable	Inverse RS-FEC control	1.2200.1	FEC_bypass_indication_enable
Table 152-2			
IFEC bypass correction ability	Inverse RS-FEC status	1.2201.0	FEC_bypass_correction_ability
IFEC bypass indication ability	Inverse RS-FEC status	1.2201.1	FEC_bypass_indication_ability
Inverse RS-FEC high SER	Inverse RS-FEC status	1.2201.2	hi_ser
FEC AM lock x, x=0 to 3	Inverse RS-FEC status	1.2201.8:11	amps_lock<*x* >
Inverse RS-FEC align status	Inverse RS-FEC status	1.2201.14	fec_align_status
IFEC corrected codewords	Inverse RS-FEC corrected codewords counter	1.2202, 1.2203	IFEC_corrected_cw_counter
IFEC uncorrected codewords	Inverse RS-FEC uncorrected codewords counter	1.2204, 1.2205	IFEC_uncorrected_cw_counter
FEC lane x mapping	Inverse RS-FEC lane mapping	1.2206	FEC_lane_mapping<*x* >
FEC symbol errors, FEC lanes 0 to 3	Inverse RS-FEC symbol error counter, lane 0 to 3	1.2207 to 1.2217	FEC_symbol_error_counter_*i*

Option 1 to improve register and variable name consistency

Use IFEC for a variable that could be applicable to inverse of any FEC code (essentially all variables), and call out “Inverse RS-FEC” only for a variable that would be specifically for this FEC code (essentially no variables) – changes highlighted

Table 152-1			
IFEC bypass correction enable	**IFEC** control	1.2200.0	**I**FEC_bypass_correction_enable
IFEC bypass indication enable	**IFEC** control	1.2200.1	**I**FEC_bypass_indication_enable
Table 152-2			
IFEC bypass correction ability	**IFEC** status	1.2201.0	**I**FEC_bypass_correction_ability
IFEC bypass indication ability	**IFEC** status	1.2201.1	**I**FEC_bypass_indication_ability
IFEC high SER	**IFEC** status	1.2201.2	hi_ser
IFEC AM lock x, x=0 to 3	**IFEC** status	1.2201.8:11	amps_lock<*x* >
IFEC align status	**IFEC** status	1.2201.14	**IFEC**_align_status
IFEC corrected codewords	**IFEC** corrected codewords counter	1.2202, 1.2203	IFEC_corrected_cw_counter
IFEC uncorrected codewords	**IFEC** uncorrected codewords counter	1.2204, 1.2205	IFEC_uncorrected_cw_counter
IFEC lane x mapping	**IFEC** lane mapping	1.2206	**I**FEC_lane_mapping<*x* >
IFEC symbol errors, FEC lanes 0 to 3	**IFEC** symbol error counter, lane 0 to 3	1.2207 to 1.2217	**I**FEC_symbol_error_counter_*i*

Table 45-3 Register Name Changes (Option 1)

Register address	Register name	Subclause
1.2200	Inverse RS-FEC control	45.2.1.186aa
1.2201	Inverse RS-FEC status	45.2.1.186ab
1.2202, 1.2203	Inverse RS-FEC corrected codewords counter	45.2.1.186ac
1.2204, 1.2205	Inverse RS-FEC uncorrected codewords counter	45.2.1.186ad
1.2206	Inverse RS-FEC lane mapping	45.2.1.186ae
1.2207 through 1.2209	Reserved	
1.2210 through 1.2217	Inverse RS-FEC symbol error counter, lane 0 to 3	45.2.1.186af, 45.2.1.186ag

Existing

Register address	Register name	Subclause
1.2200	IFEC control	45.2.1.186aa
1.2201	IFEC status	45.2.1.186ab
1.2202, 1.2203	IFEC corrected codewords counter	45.2.1.186ac
1.2204, 1.2205	IFEC uncorrected codewords counter	45.2.1.186ad
1.2206	IFEC lane mapping	45.2.1.186ae
1.2207 through 1.2209	Reserved	
1.2210 through 1.2217	IFEC symbol error counter, lane 0 to 3	45.2.1.186af, 45.2.1.186ag

Updated

Table 45-150aa Register and Bit Name changes (Option 1)

Table 45-150aa-Inverse RS_FEC control register bit definitions

Bit(s)	Name	Description	R/W
1.2200.15:2	Reserved	Value always 0	RO
1.2200.1	IFEC bypass indications enable	1 = FEC decoder does not indicate errors to the remote PCS 0 = FEC decoder indicates errors to the remote PCS layer	R/W
1.2200.0	IFEC bypass correction enable	1 = FEC decoder performs error detection without error correction 0 = FEC decoder performs error detection and error correction	R/W

Existing

Table 45-150aa-IFEC control register bit definitions

Bit(s)	Name	Description	R/W
1.2200.15:2	Reserved	Value always 0	RO
1.2200.1	IFEC bypass indications enable	1 = IFEC decoder does not indicate errors ~~to the remote PCS~~ 0 = IFEC decoder indicates errors ~~to the remote PCS layer~~	R/W
1.2200.0	IFEC bypass correction enable	1 = IFEC decoder performs error detection without error correction 0 = IFEC decoder performs error detection and error correction	R/W

Updated

Copy/paste error from Clause 91-related registers. In the case of clause 152, errors are indicated to SC-FEC rather than the PCS.

Table 45-150ab Register and Bit Name changes (Option 1)

Table 45-150ab-Inverse RS-FEC status register bit definitions

Bit(s)	Name	Description	R/W
1.2201.15	PCS align status	1 = FEC decoder has locked and aligned all PCS lanes 0 = FEC decoder has not locked and aligned all PCS lanes	RO
1.2001.14	Inverse RS-FEC align status	1 = FEC receive lanes locked and aligned 0 = FEC receive lanes not locked and aligned	RO
1.2001.13:12	Reserved	Value always 0	RO
1.2001.11	FEC AM lock 3	1 = RS-FEC lane 3 locked and aligned 0 = RS-FEC lane 3 not locked and aligned	RO
1.2001.10	FEC AM lock 2	1 = RS-FEC lane 2 locked and aligned 0 = RS-FEC lane 2 not locked and aligned	RO
1.2001.9	FEC AM lock 1	1 = RS-FEC lane 1 locked and aligned 0 = RS-FEC lane 1 not locked and aligned	RO
1.2001.8	FEC AM lock 0	1 = RS-FEC lane 0 locked and aligned 0 = RS-FEC lane 0 not locked and aligned	RO
1.2001.7:3	Reserved	Value always 0	RO
1.2001.2	Inverse RS-FEC high SER	1 = FEC errors have exceeded threshold 0 = FEC errors have not exceeded threshold	RO/LH
1.2001.1	IFEC bypass indication ability	1 = FEC decoder has the ability to bypass error correction 0 = FEC decoder does not have the ability to bypass error correction	RO
1.2001.0	IFEC bypass correction ability	1 = FEC decoder performs error detection without error correction 0 = FEC decoder performs error detection and error correction	RO

Existing

Table 45-150ab Register and Bit Name changes (Option 1) - continued

Table 45-150ab-IFEC status register bit definitions

Bit(s)	Name	Description	R/W
1.2201.15	PCS align status	1 = IFEC decoder has locked and aligned all PCS lanes 0 = IFEC decoder has not locked and aligned all PCS lanes	RO
1.2001.14	IFEC align status	1 = IFEC receive lanes locked and aligned 0 = IFEC receive lanes not locked and aligned	RO
1.2001.13:12	Reserved	Value always 0	RO
1.2001.11	IFEC AM lock 3	1 = IFEC lane 3 locked and aligned 0 = IFEC lane 3 not locked and aligned	RO
1.2001.10	IFEC AM lock 2	1 = IFEC lane 2 locked and aligned 0 = IFEC lane 2 not locked and aligned	RO
1.2001.9	IFEC AM lock 1	1 = IFEC lane 1 locked and aligned 0 = IFEC lane 1 not locked and aligned	RO
1.2001.8	IFEC AM lock 0	1 = IFEC lane 0 locked and aligned 0 = IFEC lane 0 not locked and aligned	RO
1.2001.7:3	Reserved	Value always 0	RO
1.2001.2	IFEC high SER	1 = IFEC errors have exceeded threshold 0 = IFEC errors have not exceeded threshold	RO/LH
1.2001.1	IFEC bypass indication ability	1 = IFEC decoder has the ability to bypass error correction 0 = IFEC decoder does not have the ability to bypass error correction	RO
1.2001.0	IFEC bypass correction ability	1 = IFEC decoder performs error detection without error correction 0 = IFEC decoder performs error detection and error correction	RO

Updated

Table 45-150ac Register and Bit Name changes (Option 1)

Table 45-150ac-Inverse RS-FEC corrected codewords counter bit definitions

Bit(s)	Name	Description	R/W
1.2202.15:0	IFEC corrected codewords lower	IFEC_corrected_cw_counter[15:0]	RO, NR
1.2203.15:0	IFEC corrected codewords upper	IFEC_corrected_cw_counter[31:16]	RO, NR

Existing

Table 45-150ac-IFEC corrected codewords counter bit definitions

Bit(s)	Name	Description	R/W
1.2202.15:0	IFEC corrected codewords lower	IFEC_corrected_cw_counter[15:0]	RO, NR
1.2203.15:0	IFEC corrected codewords upper	IFEC_corrected_cw_counter[31:16]	RO, NR

Updated

Table 45-150ad
Register and Bit Name changes (Option 1)

Table 45–150ad—Inverse RS-FEC uncorrected codewords counter bit definitions

Bit(s)	Name	Description	R/W
1.2204.15:0	IFEC corrected codewords lower	IFEC_uncorrected_cw_counter[15:0]	RO, NR
1.2205.15:0	IFEC corrected codewords upper	IFEC_uncorrected_cw_counter[31:16]	RO, NR

Existing

Table 45–150ad—IFEC uncorrected codewords counter bit definitions

Bit(s)	Name	Description	R/W
1.2204.15:0	IFEC corrected codewords lower	IFEC_uncorrected_cw_counter[15:0]	RO, NR
1.2205.15:0	IFEC corrected codewords upper	IFEC_uncorrected_cw_counter[31:16]	RO, NR

Updated

Table 45-150ae
Register and Bit Name changes (Option 1)

Existing

Table 45–150ae—Inverse RS-FEC lane mapping register			
Bit(s)	Name	Description	R/W
1.2206.15:8	Reserved	Value always 0	RO
1.2206.7:6	RS-FEC lane 3 mapping	RS-FEC lane mapped to IFEC lane 3	RO
1.2206.5:4	RS-FEC lane 2 mapping	RS-FEC lane mapped to IFEC lane 2	RO
1.2206.3:2	RS-FEC lane 1 mapping	RS-FEC lane mapped to IFEC lane 1	RO
1.2206.1:0	RS-FEC lane 0 mapping	RS-FEC lane mapped to IFEC lane 0	RO

Updated

Table 45–150ae—IFEC lane mapping register			
Bit(s)	Name	Description	R/W
1.2206.15:8	Reserved	Value always 0	RO
1.2206.7:6	RS-FEC lane 3 mapping	RS-FEC lane mapped to IFEC lane 3	RO
1.2206.5:4	RS-FEC lane 2 mapping	RS-FEC lane mapped to IFEC lane 2	RO
1.2206.3:2	RS-FEC lane 1 mapping	RS-FEC lane mapped to IFEC lane 1	RO
1.2206.1:0	RS-FEC lane 0 mapping	RS-FEC lane mapped to IFEC lane 0	RO

Table 45-150af
Register and Bit Name changes (Option 1)

Existing

Table 45–150af—Inverse RS-FEC symbol error counter bit definitions			
Bit(s)	Name	Description	R/W
1.2210.15:0	FEC symbol errors, lane 0 lower	FEC_symbol_error_counter_0[15:0]	RO/NR
1.2211.15:0	FEC symbol errors, lane 0 upper	FEC_symbol_error_counter_0[31:16]	RO/NR

Clause 91 called these FEC symbol errors (rather than RS-FEC symbol errors) for an unknown reason. Could be updated to RS-FEC for accuracy, or left alone for consistency with Clause 91

Updated

Table 45–150af—IFEC symbol error counter bit definitions			
Bit(s)	Name	Description	R/W
1.2210.15:0	FEC symbol errors, lane 0 lower	FEC_symbol_error_counter_0[15:0]	RO/NR
1.2211.15:0	FEC symbol errors, lane 0 upper	FEC_symbol_error_counter_0[31:16]	RO/NR

Corresponding text changes to be made to clause 45.2.1.186ag for symbol errors on lanes 1, 2, 3 even though there is no register/bit table for these lanes

Option 2 to improve register and variable name consistency

Follow conventions as in the text: use IFEC for a variable that is related to the service interface, and use “Inverse RS-FEC” for a variable related to a sublayer internal function – changes highlighted

Table 152-1			
Inverse RS-FEC bypass correction enable	Inverse RS-FEC control	1.2200.0	**inverse_RS-**FEC_bypass_correction_enable
Inverse RS-FEC bypass indication enable	Inverse RS-FEC control	1.2200.1	**inverse_RS-**FEC_bypass_indication_enable
Table 152-2			
Inverse RS-FEC bypass correction ability	Inverse RS-FEC status	1.2201.0	**inverse_RS-**FEC_bypass_correction_ability
Inverse RS-FEC bypass indication ability	Inverse RS-FEC status	1.2201.1	**inverse_RS-**FEC_bypass_indication_ability
Inverse RS-FEC high SER	Inverse RS-FEC status	1.2201.2	hi_ser
IFEC AM lock x, x=0 to 3	Inverse RS-FEC status	1.2201.8:11	amps_lock<*x* >
IFEC align status	Inverse RS-FEC status	1.2201.14	**IFEC**_align_status
Inverse RS-FEC corrected codewords	Inverse RS-FEC corrected codewords counter	1.2202, 1.2203	**inverse_RS-FEC**_corrected_cw_counter
Inverse RS-FEC uncorrected codewords	Inverse RS-FEC uncorrected codewords counter	1.2204, 1.2205	**inverse_RS-FEC**_uncorrected_cw_counter
IFEC lane x mapping	Inverse RS-FEC lane mapping	1.2206	**I**FEC_lane_mapping<*x* >
Inverse RS-FEC symbol errors, FEC lanes 0 to 3	Inverse RS-FEC symbol error counter, lane 0 to 3	1.2207 to 1.2217	**inverse_RS-**FEC_symbol_error_counter_*i*

Proposal

- Adopt Option 1 (slides 5-13) to improve register and variable name consistency. Supporting text and clause 45 section headings are updated to reflect updated register and/or bit-field names.
  - While Option 2 also adds consistency, it has the drawbacks of creating possible confusion by both changing some IFEC to Inverse RS-FEC and changing other Inverse RS-FEC to IFEC. It is also wordier and less compact in variable naming. (Would need to work through Clause 45 details for Option 2 if that option were to be preferred)
- Would also be an option to leave this unchanged, as the situation is no worse (and following the same pattern) as register and variable naming for Clause 91, along with its Clause 45 register definitions