Towards a baseline specification for 400GBASE-ZR transmitter clock phase jitter

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Outline

- Chief editor’s summary on optical parameters
- IEEE 802.3 reference jitter specs
- OIF 400ZR reference jitter spec
- Analysis of 400GBASE-ZR Tx clock phase jitter
- Proposal

From P802.3cw Chief Editor

- Key Open Topics (issenhuth_3cw_01_200716)
  - Impacts of 75GHz spacing
  - **Optical Parameters**
  - EVM test methodology

- Optical Parameters Baseline Proposal Status (issenhuth_3cw_01_200611)
  - FFS (for further studies) items proposed in slide 17 of Sluyski-02-200507
  - **Tx clock phase noise** is one of the FFS items in transmitter spec section

Reference 802.3-2018 400G jitter specifications

- Section 8 - Annex 120D (normative): 400GAUI-8 C2C interface
  - Specifies TX jitter with J_{RMS}, J4u and EOJ
- Section 8 - Annex 120E (normative) : 400GAUI-8 C2M interface
  - Uses an eye width specification, jitter specification is implied
- Clause 124: 400GBASE-DR4 PMD optical interface
  - Specifies Tx quality metric (TDECQ), jitter specification is implied
    - Refers Clause 121 which describes the setup to measure TDECQ on the optical output

Ref 1: IEEE 802.3-2018 Annex 120D C2C

Output jitter			
J_{RMS} (max)	120D.3.1.8	0.023	UI
J4u (max)	120D.3.1.8	0.118	UI
Even-odd jitter (max)	120D.3.1.8	0.019	UI

The jitter is measured with a clock recovery unit (CRU) with a corner frequency of 4 MHz and a slope of 20 dB/decade. Jitter measurements are performed with transmitters on all lanes enabled and using identical transmitter equalizer settings. Transmitters on lanes not under test transmit PRBS31Q, or a valid 200GBASE-R or 400GBASE-R signal. PRBS31Q is described in 120.5.11.2.2.

IEEE 802.3-2018 section 8, pg375

Ref 2: IEEE 802.3-2018 Annex 120E C2M

ESMW (Eye symmetry mask width)	120E.4.2	0.22	UI
Eye height, differential (min)	120E.4.2	32	mV

120E.4.2 Eye width and eye height measurement method

Eye diagrams in 200GAUI-4 and 400GAUI-8 chip-to-module are measured using a reference receiver. The reference receiver includes a fourth-order Bessel-Thomson low-pass filter response with 33 GHz 3 dB bandwidth, and a selectable continuous time linear equalizer (CTLE) to measure eye height and width. The pattern used for output eye diagram measurements is PRBS13Q. Unless specified otherwise the probabilities are relative to the number of PAM4 symbols measured. The following procedure should be used to obtain the eye height and eye width parameters, as illustrated by Figure 120E–13:

1) Capture the PRBS13Q using a clock recovery unit with a corner frequency of 4 MHz and slope of 20 dB/decade. The capture includes a minimum of 3 samples per symbol, or equivalent. Collect sufficient samples equivalent to at least 1.2 million PAM4 symbols to allow for construction of a normalized cumulative distribution function (CDF) to a probability of 10^{-5} without extrapolation.

IEEE 802.3-2018 section 8, pg401

Ref 3: IEEE 802.3-2018 Clause 124 DR4

Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	3.4	dB

The test pattern (specified in Table 121–10) is transmitted repetitively by the optical lane under test and the oscilloscope is set up to capture the complete pattern for TDECQ analysis as described in 121.8.5.3. The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology.

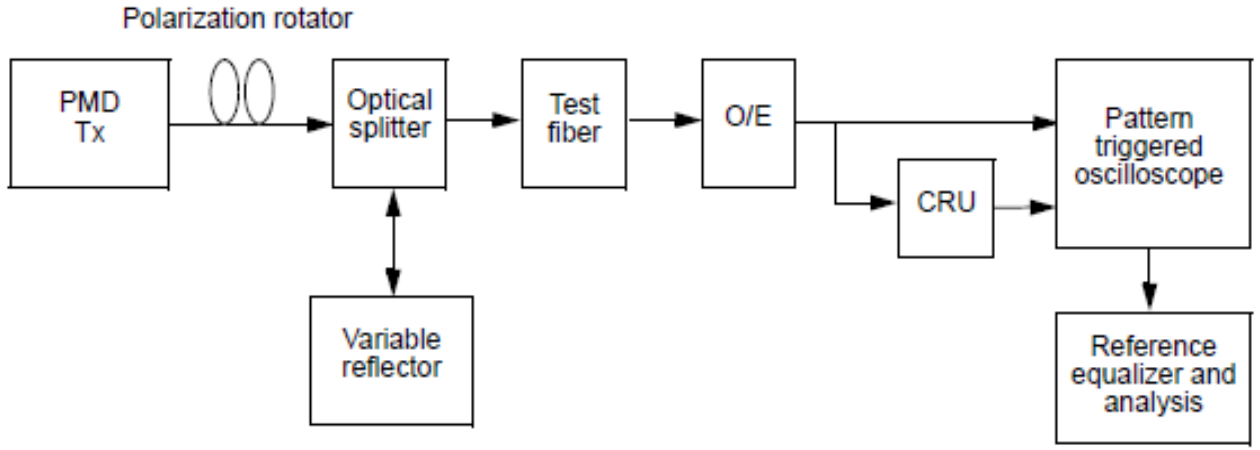

Figure 121–4—TDECQ conformance test block diagram

IEEE 802.3-2018 section 8, pg132

OIF 400ZR reference jitter spec

Tx clock phase noise (PN): Maximum PN mask for low frequency PN

https://www.oiforum.com/wp-content/uploads/OIF-400ZR-01.0_reduced2.pdf#page=61

Tx clock phase noise (PN): Maximum total integrated RMS phase jitter between 10KHz and 10MHz

https://www.oiforum.com/wp-content/uploads/OIF-400ZR-01.0_reduced2.pdf#page=62

Tx clock phase noise (PN): Maximum total integrated RMS phase jitter between 1MHz and 200MHz

https://www.oiforum.com/wp-content/uploads/OIF-400ZR-01.0_reduced2.pdf#page=63

Integrated jitter does not include a clock recovery transfer function

A high pass filter is essential

- Integrated jitter without a high-pass filter is unbounded
  - For example, here is an example of the integrated jitter of the phase noise mask over different frequency ranges
    - 10kHz-10MHz: 507fs
    - 1kHz-10MHz: 1.6ps
    - 100Hz-10MHz: 4.9ps
- From a system perspective, we care about the **jitter relative to the recovered clock at the receiver.** This is modelled in prior specifications by applying a first-order high-pass filter to the phase noise (and spurs) prior to integration. The high-pass filter models the behavior of timing recovery in a reference receiver and is specified by the standard
  - For example, here is the integrated jitter with a high-pass filter with 3dB cutoff at 1MHz
    - 10kHz-10MHz: 154fs
    - 1kHz-10MHz: 154fs
    - 100Hz-10MHz: 154fs

Direct measurement on the Tx output

- TX signal test point has highest bandwidth and cleanest jitter from system perspective
  - Specifications on TX clock assume an auxiliary path where a (possibly divided) version of the TX clock is brought out of the chip with high quality specifically for jitter measurements.
  - This is unnecessary because test equipment (high-speed digital scopes) are widely available and commonly used for these type of measurements. The measurement is done directly on the TX output using PRBS sequences to capture all the effects of normal operation.
  - Some effects such as odd-even jitter due to poor power supply rejection etc. can only be seen on the broadband TX output signal
- Measurements on a divided TX clock do not capture all the important parameters necessary for interoperability.

Further Thoughts

- IEEE 802.3-2018 Annex 120D specifies a jitter high pass filter with 3dB of 4MHz. A lower 3dB frequency of ~2MHz is more appropriate for a DSP intensive design such as a coherent receiver.
- Various clauses in IEEE standards tend to take different approaches to split the jitter into unbounded (or random) components and the bounded (or deterministic) components
- Any linear inter-symbol-interference (ISI) effects should not be treated as jitter because the coherent receiver is expected to equalize and compensate for ISI. Digital scope typically has the ability to extract and calculate this component automatically.
- Even-odd jitter (EOJ) should be specified explicitly because it is common to implement high-speed designs as slower parallel paths and even-odd mismatches can degrade performance severely.

Analysis of standardized jitter spec methodology

- **IEEE and OIF have converged on transmit jitter specifications for PAM4 and have defined procedures for measurement**
  - IEEE 802.3-2018 Annex 120D
  - OIF-CEI-56G-MR-PAM4: Clause 17
  - OIF-CEI-56G-LR-PAM4: Clause 21
- **Jitter is specified using the following**
  - Uncorrelated jitter interval with probability 1e-4: J4u < 0.118 UI
  - Uncorrelated jitter rms: J_{RMS} < 0.023UI
  - Even-odd jitter < 0.019UI
- **This methodology allows more flexibility and avoids some of the difficulties in jitter measurement**
  - Measurement using a specified PRBS13Q test pattern which is built into scopes
  - Measurement procedure excludes ISI/data-dependent components

Calculation of RJ and BUJ for 400GBASE-ZR

$$A_{DD} = \left(\left(\frac{J4u}{2}\right) + Q4\sqrt{\left((Q4^2+1)\times J_{RMS}{}^2 - \left(\frac{J4u}{2}\right)^2\right)}\right)/(Q4^2+1) \qquad (120D\text{–}10)$$

$$\sigma_{RJ} = \left(\frac{J4u}{2} - A_{DD}\right)/(Q4) \qquad (120D\text{–}11)$$

Where $Q4$ is 3.8906.

IEEE 802.3-2018 section 8, pg377

- **A_{DD} is the peak of dual-dirac jitter model and represents the peak of bounded uncorrelated jitter**
- **σ_{RJ} is the RMS of the random jitter (i.e. unbounded uncorrelated jitter)**
- **J4u and J_{RMS} specifications from Annex 120D translate into**
  - σ_{RJ} <0.01UIrms and A_{DD} < 0.02UIpeak
  - Limits σ_{RJ} <0.015UIrms if there is negligible bounded jitter/spurs

For P802.3cw 400GBASE-ZR

- σ_{RJ} <166fs rms with up to 650fs peak-to-peak of bounded jitter, or
- σ_{RJ} <250fs rms with negligible bounded jitter
- These numbers are consistent with a 2MHz CRU applied to the current phase noise mask [dBc/Hz over Frequency] defined in 400ZR in OIF
- Limits single spurs to under 650fs peak-to-peak or ~230fs rms

Proposal for 400GBASE-ZR Tx clock phase jitter spec

- Option A: Adopt traditional IEEE 802.3 Tx jitter specifications (J4u, J_{RMS}, even-odd jitter) with values specified in previous slide, and measurement methodology from Annex 120D with a proposed CRU bandwidth of 2MHz.
  - This option also allows relatively easy addition of 100GBASE-ZR (P802.3ct) Tx clock jitter specs in case we choose to do so

- Option B: Leverage IEEE 802.3-2018 Clause 124 400GBASE-DR4 Tx quality metric for coherent Tx output. Tx EVM could be one such candidate to incorporate Tx clock jitter. However, designing, agreeing on, and verifying require considerable efforts.

- Option C: Adopt existing OIF 400ZR IA Tx clock phase noise mask and jitter specs with the understanding that it deviates from IEEE jitter specification methodologies