IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

**Comment #10**

**Comment Type:** E  
**Comment Status:** A

Brown, Matt  
Huawei

"400GBASE-Z" should be "400GBASE-ZR".

**Suggested Remedy:**  
Change "400GBASE-Z" to "400GBASE-ZR".

**Response:**  
Response Status: C  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment #12**

**Comment Type:** E  
**Comment Status:** A

Lewis, Jon  
Dell Technologies

Text and arrow intersect.

**Suggested Remedy:**  
Remove intersection of text and arrow to make the figure more legible.

**Response:**  
Response Status: C  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment #13**

**Comment Type:** T  
**Comment Status:** A

Bruckman, Leon  
Huawei

Clause 155.3.3.3.1 defines FAW as a 22 symbols sequence, "bits" are not mentioned there

**Suggested Remedy:**  
For consistency replace: "The sequence is considered to be valid if at least 36 bits match the 44 known bits of the FAW pattern described in 155.3.3.3.1.,” with: "The sequence is considered to be valid if at least 18 symbols match the 22 known symbols of the FAW pattern described in 155.3.3.3.1."

**Response:**  
Response Status: C  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment #14**

**Comment Type:** E  
**Comment Status:** A

Bruckman, Leon  
Huawei

Text on FAW synchronization seems to imply that there is a FAW synchronization process for each lane, for a total of 4 independent FAW synchronization processes. Actually there are 2 FAW synchronization processes, one per polarization (see figure 115.10 and clause 155.3.7)

**Suggested Remedy:**  
Replace: "The synchronization process operates independently on each lane" with: "The synchronization process operates independently on each polarization"

**Response:**  
Response Status: C  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment #15**

**Comment Type:** E  
**Comment Status:** A

Bruckman, Leon  
Huawei

Empty box without any function

**Suggested Remedy:**  
Remove empty fbox from figure 155-10

**Response:**  
Response Status: C  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment #16**

**Comment Type:** ER  
**Comment Status:** A

Gorshe, Steve  
Microchip Technology

The current text refers to "the +/- 100ppm 257-bit blocks" Blocks don't have a frequency or ppm offset in and of themselves. Rather it is the block stream that has a rate with associate frequency tolerance.

**Suggested Remedy:**  
In this paragraph and any other occurrances, references to the frequency or frequency offset of "blocks" should be changed to "block stream"

**Response**  
Response Status: W  
ACCEPT IN PRINCIPLE.

See response to comment #346.
Response #17
Cl 155 SC 155.2.4.5.3 P 40 L 24 # 17
Gorsh, Steve Microchip Technology

Comment Type E Comment Status A rewrite bucket

It seems worthwhile to provide some basic context regarding the meaning of Cm(t) and SCn(t). Although G.709 provides the details, it may be worthwhile expanding this statement somewhat.

Suggested Remedy
I suggest adding the following sentences to the end of this paragraph: "Note that Cm(t) indicates the number of 1028-bit GMP data words that will be transmitted during the next multi-frame, with SCnD(t) nominally indicating the running remainder. Averaging the Cm(t) plus SCnD(t) values across multiple multi-frames, the average represent the incoming serial stream rate as the number of information bytes arriving at the GMP encoder per multi-frame."

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Response #18
Cl 155 SC 155.2.5.8 P 48 L 36 # 18
Gorsh, Steve Microchip Technology

Comment Type ER Comment Status A rewrite bucket

The sentence incorrectly confuses the location and coverage of the GMP CRC fields. Specifically, it says that the CRC8 is found in JC1-3 and the CRC4 is found in JC4-6. The CRC8 is located in JC3 and the CRC4 is located in JC6.

Suggested Remedy
Change the last sentence of the paragraph to read: "The CRC8 value in JC3 provides error detection coverage for the information in JC1-JC3 and the CRC4 value in JC4 provides error detection coverage for the associated information fields in JC4-6."

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Response #19
Cl 155 SC 155.2.5.8 P 48 L 36 # 19
Gorsh, Steve Microchip Technology

Comment Type E Comment Status A rewrite bucket

This sentence appears to incorrectly imply that the CRC8 is the sole protection against errors in JC1-3. Although G.709 provides the details, it may be worthwhile expanding this statement somewhat.

Suggested Remedy
In conjunction with the change proposed in the previous comment, add the following sentence to the end of the paragraph: "The JC1-2 field information is also protected by limits on how the JC1-2 fields can change in successive multi-frames and the coding technique for indicating these changes, which combine with the CRC8 in JC3 to provide error correction capability for bit and burst errors impacting JC1-3."

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Response #20
Cl 155 SC 155.2.1 P 36 L 22 # 20
Gustlin, Mark Cisco

Comment Type TR Comment Status A rewrite bucket

The use of inner and outer FEC codes seems to be backwards when compared to industry standards. Two industry books on FEC are Error Control Coding (Shu Lin/Daniel Costello) and Error Control Coding (Peter Sweeney), both refer to the first code in a concatenation as the outer, and the 2nd code in a concatenation as the inner. This makes sense when you look at a diagram of the FEC codes, though it does not make sense when looking at the location of the codes in the concatenation.

Suggested Remedy
Reverse the usage to: "an outer SC-FEC code" and "an inner Hamming code SD-FEC."

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.
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Cl 155 SC 155.2.1 P 36 L 35 # 28
Marris, Arthur Cadence Design Systems

Comment Type T Comment Status A rewrite bucket
Should this be "128 bit"?

SuggestedRemedy
Consider changing "128-symbol" to "128 bit symbol". Similar issue with "119-symbol" on line 37.

Response
Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.2.1 P 36 L 41 # 29
Marris, Arthur Cadence Design Systems

Comment Type T Comment Status A rewrite bucket
Is "frame" the correct word to use here?

SuggestedRemedy
Consider changing "each 400GBASE-ZR frame" to "each 400GBASE-ZR PCS lane" or define what "frame" means in this context. Perhaps add a link to Figure 155-3.

Response
Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.2.4.9 P 43 L 14 # 31
Marris, Arthur Cadence Design Systems

Comment Type T Comment Status A rewrite bucket
Is resetting the scrambler a functional requirement?

SuggestedRemedy
Consider changing "resets" to "shall be reset"

Response
Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.5.1 P 67 L 9 # 33
Marris, Arthur Cadence Design Systems

Comment Type E Comment Status A rewrite bucket
Insert correct cross reference

SuggestedRemedy
Replace 45 with a subclause number or a cross reference to Clause 45

Response
Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.1.4 P 34 L 2 # 42
Ran, Adee Cisco

Comment Type T Comment Status A rewrite bucket
The "rate" of the PCS output has been defined as per-lane transfer rate in previous PCS clauses, not as the aggregate bit rate as defined here. Consistency is preferable.

SuggestedRemedy
Change to the per-lane rate (59.84375 ? 28/29 Gb/s on each of 8 PCS lanes).

Response
Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.2.1 P 36 L 6 # 43
Ran, Adee Cisco

Comment Type E Comment Status A rewrite bucket
The sentence "The PCS.. can operate in normal mode or in test-pattern mode" is out of place in the first paragraph. These modes are only discussed in the third paragraph.

SuggestedRemedy
Move the last sentence of the first paragraph to a separate paragraph before the current third paragraph.

Response
Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

**Comment #44**

**Comment Type:** E  
**Comment Status:** A  
**Rewrite Bucket:** 

Line 5 says "PCS Transmit and PCS Receive processes", but then in lines 7, 17, and 27 it is "transmit channel", and line 35 "receive channel".
"channel" is an overloaded term, it is not defined in this clause and its other meanings are quite different.

**Suggested Remedy:**
Change "transmit channel" to "Transmit process", 3 times. Change "receive channel" to "Receive function".

**Response:** ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment #46**

**Comment Type:** T  
**Comment Status:** A  
**Rewrite Bucket:** 

The scrambled idle pattern defined in 119.2.4.9 cannot be used here as is, because the PCS processes are different.

**Suggested Remedy:**
Add a new subclause based on 119.2.4.9 but specific to this clause, and refer to it instead.

**Response:** ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment #48**

**Comment Type:** E  
**Comment Status:** A  
**Rewrite Bucket:** 

"257B blocks" is inconsistent with "257-bit blocks" used earlier. "B" is not used to denote bits elsewhere (except as abbreviations in coding scheme names).

Similarly "66b", "120b", and other instances in this draft.

**Suggested Remedy:**
Change "257B" to "257-bit" across the draft except where it is part of "256B/257B".

Similarly, change "66b" to "66-bit" in 155.2.2, "120b" to "120-bit" in 155.2.4.3, and similar instances as necessary.

**Response:** ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment #49**

**Comment Type:** E  
**Comment Status:** A  
**Rewrite Bucket:** 

"The frame is illustrated as a structure with 256 rows of 10 280 bits with a logical transmission order of left to right, top to bottom. This frame contains 5140 bits of overhead and 10 220 257B blocks of payload. This frame is illustrated in Figure 155-3"  

The order should be clearly defined in the text, not just "illustrated" in a figure.

The text can be made shorter and clearer.

**Suggested Remedy:**
Change the quoted text to:
"The frame is a structure that contains 5140 bits of overhead followed by 10 220 257-bit blocks of payload. This frame is illustrated in Figure 155-3, with transmission order from top row to bottom row and from left to right within each row".

**Response:** ACCEPT IN PRINCIPLE.

See response to comment #346.
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<table>
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<tr>
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<th>Comment Status</th>
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<tr>
<td>155</td>
<td>155.2.4.3</td>
<td>38</td>
<td>5</td>
<td>50</td>
<td>T</td>
<td>A</td>
<td>rewrite bucket</td>
</tr>
</tbody>
</table>
|     | Ran, Adee | Cisco | *starting at column 5141 of row 0 and ending at column 10 280 of row 255, using GMP*
"column" has not been mentioned in preceding text. I assume a column is a bit, so there's no need to use another term (and possibly create confusion, since in the related Clause 155 the columns denote octets).
The payload area ends simply at the end of the frame, so rows are not necessary either.
Suggested Remedy
Change the quoted text to "from bit 5141 to the end of the frame, using GMP"
Change "column" to "bit" across this description.
Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

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<tr>
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<th>Comment Status</th>
<th>Suggested Remedy</th>
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<td>38</td>
<td>30</td>
<td>52</td>
<td>T</td>
<td>A</td>
<td>rewrite bucket</td>
</tr>
</tbody>
</table>
|     | Ran, Adee | Cisco | It seems that the GMP word numbers start from 1 while the bits and rows start from 0. If the starting index is inconsistent, it should at least be explicit.
Suggested Remedy
Add "(starting from 1)" after "GMP word numbers".
Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

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<tr>
<th>Cl</th>
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<tr>
<td>155</td>
<td>155.2.4.3</td>
<td>38</td>
<td>30</td>
<td>53</td>
<td>E</td>
<td>A</td>
<td>rewrite bucket</td>
</tr>
</tbody>
</table>
|     | Ran, Adee | Cisco | The "(row, column)" column seems redundant with the GMP word numbers. Also, "rows" is only used for illustration and "column" is not defined.
Suggested Remedy
Consider deleting the third column. Otherwise, change "column" to "bit #".
Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

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<tr>
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<td>155.2.4.3</td>
<td>39</td>
<td>6</td>
<td>54</td>
<td>E</td>
<td>A</td>
<td>rewrite bucket</td>
</tr>
</tbody>
</table>
|     | Ran, Adee | Cisco | "10 970 bit row aligned" - the number is part of a compound noun so a hyphen should be used. The separator is not helpful in this case.
Suggested Remedy
Change to "10970-bit row aligned".
Response
ACCEPT IN PRINCIPLE.
See response to comment #346.
Comment ID 55

**Comment Type** E  **Comment Status** A  **rewrite bucket**

"The AM field, containing am_mapped<1919:0> is transmitted LSB first, i.e. am_mapped<0> first, and am_mapped<1919> last"

This phrasing is awkward (am_mapped has already been defined in the first paragraph) and redundant.

**SuggestedRemedy**

Change to "The transmission order of am_mapped is from am_mapped<0> to am_mapped<1919>".

**Response**

Response Status C

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Comment ID 56

**Comment Type** E  **Comment Status** A  **rewrite bucket**

"The 400GBASE-ZR overhead is a 40-byte frame structure that uses a four-frame multi-frame, as shown in Figure 155-4"

There are 3 occurrences of "frame" in this sentence, it's unclear what they mean (especially with "400GBASE-ZR frame" also being defined; "frame" is an overly overloaded term).

Also, "byte" is not strictly defined in 802.3 and we typically use the more specific "octet" instead.

**SuggestedRemedy**

Change to "The 400GBASE-ZR overhead is a 160-octet block that is divided into four 40-octet frames, as shown in Figure 155-4".

Change "byte" to "octet" globally.

In 151.2.4.5.1, change "a 256-frame multi-frame sequence" to "a 256-frame sequence".

In 155.2.4.5.3 change "four-frame multi-frame" to "OH".

Change elsewhere as appropriate.

Implement with editorial license.

**Response**

Response Status C

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Comment ID 57

**Comment Type** T  **Comment Status** A  **rewrite bucket**

C_m(t) and CnD(t) are used but not defined.

I assume they are defined in an external reference, but it is unclear. If all control bytes are defined externally then there is no need for this text.

**SuggestedRemedy**

Preferably add the detailed definitions from the referenced document.

Otherwise, delete the entire last paragraph.

**Response**

Response Status C

ACCEPT IN PRINCIPLE.

See response to comment #346.
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**Comment Type:** T  **Comment Status:** A  **rewrite bucket**

I assume the MFAS is an 8-bit counter, but figure 155-4 shows only 2 bits. This can confuse readers.

**Suggested Remedy:**
Change "It is a wrapping counter that is incremented each frame" to "It is an auto-wrapping 8-bit counter that is incremented on each 40-octet frame within the OH block."

**Response:**
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment ID:** 60

**Comment Type:** E  **Comment Status:** A  **rewrite bucket**

What do "downstream", "host interface signal" and "MDI signal" mean? Perhaps "downstream" should be "link partner"?

For signals, are these the signals received by the 400GAUI C2M (which is optional) and the MDI?

**Suggested Remedy:**
Please rephrase to clarify.

**Response:**
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment ID:** 61

**Comment Type:** E  **Comment Status:** A  **rewrite bucket**

"mapped to 5 successive SC-FEC blocks"

isolated numbers less than 10 in general text should be spelled out.

**Suggested Remedy:**
Change "5" to "five".

Implement similar changes, and write numbers greater than 9 in digits, across the document as necessary.

**Response:**
ACCEPT IN PRINCIPLE.

See response to comment #346.
<table>
<thead>
<tr>
<th>Cl/SC</th>
<th>P/L</th>
<th>Comment ID</th>
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<tr>
<td>155</td>
<td>40</td>
<td>64</td>
<td>E</td>
<td>A</td>
<td>C</td>
<td>&quot;The 32 bits of the CRC value are placed with the x31 term as the left-most...&quot;</td>
<td></td>
<td>delete quoted sentence.</td>
<td>accept in principle.</td>
<td></td>
<td></td>
<td>rewrite bucket</td>
<td></td>
<td></td>
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<tr>
<td>65</td>
<td>43</td>
<td>64</td>
<td>T</td>
<td>A</td>
<td>C</td>
<td>&quot;a frame-synchronous scrambler of sequence 65 535&quot;</td>
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<td>rewrite as appropriate.</td>
<td>accept in principle.</td>
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<td></td>
<td>rewrite bucket</td>
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<tr>
<td>66</td>
<td>43</td>
<td>67</td>
<td>T</td>
<td>A</td>
<td>C</td>
<td>ITU-T G.709.3 seems to be a normative reference.</td>
<td></td>
<td>rewrite bucket</td>
<td>accept in principle.</td>
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<td></td>
<td>rewrite bucket</td>
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</table>

**Comment ID 67**

**Type:** TR/technical required

**Comment Status:** D/dispatched

**Response Status:** C/closed

**Sort Order:** Comment ID
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Comment ID 68
Ran, AdeeCisco

Comment Type T
Comment Status A
Suggested Remedy

"The convolutional interleaver is described in ITU-T G.709.3 subclause 15.4.3" The text in this subclause and figure 155-7 are insufficient to understand/implement the interleaver function. If it isn't fully defined (defined only in an external document) then there is no need for this text and figure.

Suggested Remedy
Preferably add the detailed definitions from the referenced document. Otherwise, delete the whole subclause except for the quoted sentence.

Response C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 69
Ran, AdeeCisco

Comment Type T
Comment Status A
Suggested Remedy

"The generic operation of the Hamming SD-FEC scheme is specified in ITU-T G.709.3 Annex D" The text in this subclause is insufficient to understand/implement the SD-FEC encoder function. If it isn't fully defined (defined only in an external document) then there is no need for the details in the second paragraph.

Suggested Remedy
Preferably add the detailed definitions from the referenced document. Otherwise, delete the second paragraph.

Response C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 70
Ran, AdeeCisco

Comment Type T
Comment Status A
Suggested Remedy

"The SC-FEC decoder function is described in ITU-T G.709.2 Annex A" The text in this subclause is insufficient to understand/implement the SD-FEC decoder function. If it isn't fully defined (defined only in an external document) then there is no need for the details in the first paragraph.

Suggested Remedy
Preferably add the detailed definitions from the referenced document. Otherwise, delete the first two paragraphs, retaining the quoted sentence.

Response C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 71
Ran, AdeeCisco

Comment Type E
Comment Status A
Suggested Remedy

The third paragraph "The 400GBASE-ZR PCS provides detection and signaling of link degrade for use by network equipment..." is repeated verbatim in 155.2.5.7.2. No need to write it twice.

Suggested Remedy
Delete the third paragraph.

Response C
ACCEPT IN PRINCIPLE.

See response to comment #346.
Comment ID: 72
Ran, Adee
Cisco

Comment Type: E
Comment Status: A
"will" is deprecated.

SuggestedRemedy
Change "will have" to "has".
Change other instances as necessary.

Response
Response Status: C
ACCEPT IN PRINCIPLE.
See response to comment #346.

---

Comment ID: 73
Ran, Adee
Cisco

Comment Type: E
Comment Status: A
There are multiple state machines (diagrams) in 155.4.
I assume Figure 155-16 is the one.

SuggestedRemedy
Change "follows the state machine in 155.4" to "is depicted by the state diagram in Figure 155-16".

Response
Response Status: C
ACCEPT IN PRINCIPLE.
See response to comment #346.

---

Comment ID: 74
Ran, Adee
Cisco

Comment Type: T
Comment Status: A
"LF ordered sets" are not defined in this draft.
I assume it is the "Local Fault" RS ordered set.

SuggestedRemedy
Change to "Local Fault ordered sets (see 81.3.4)".
(or another ordered set if so intended)

Response
Response Status: C
ACCEPT IN PRINCIPLE.
See response to comment #346.

---

Comment ID: 75
Ran, Adee
Cisco

Comment Type: T
Comment Status: A
The term "symbol" seems to be overloaded in the PMA subclause, sometimes meaning bit, other times an element of the set {-3, -1, +1, +3}, and other times a pair of such elements (DP-16QAM symbol).
This is confusing.

SuggestedRemedy
Define a clear terminology (e.g. bits, quaternary symbols, DP-16QAM symbols) and apply it across 155.3.

Response
Response Status: C
ACCEPT IN PRINCIPLE.
See response to comment #346.
"The primitives are defined for \( i = 0 \) to 7, and for \( j = 0 \) to \( m-1 \), where \( m \) is the number of bits of resolution of the received digitized DP-16QAM symbols."

The next paragraph says the nominal signaling rate is approximately 57.78 Gb/s in the transmit side and 57.78 GBd in the receive side.

Each DP-16QAM symbol corresponds to 4 bits, so with this definition, the rate of the receive direction DP-16QAM symbols should be a quarter of the transmit direction bit rate.

Alternatively \( m \) should be the number of bits of resolution per bit of information.

The meaning of \( tx\_symbol \) and \( rx\_symbol \) is unclear in this subclause, and may be changed e.g. if the \( tx\_symbols \) are defined as Gray-coded PAM4 symbols or SD-FEC encoder codewords (suggested by another comments).

**Suggested Remedy**

Rewrite this subclause as necessary such that the meaning of \( tx\_symbol \) and \( rx\_symbol \) is clear, and the rates match the meaning.

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Signal health should not be "based on receipt of the PMD:IS\_SIGNAL\_indication from the 400GBASE-ZR PMD sublayer" because this indication is always OK.

**Suggested Remedy**

Delete "receipt of the PMD:IS\_SIGNAL\_indication from the 400GBASE-ZR PMD sublayer," and the comma after "functions".

In Figure 155-10 delete PMD:IS\_SIGNAL\_indication as input to the SIL.

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.
Each 128-bit code word from the SD-FEC encoder \( c = [c_0, c_1, \ldots, c_{127}] \), is mapped to sixteen DP-16QAM symbols. Does the PMA have to be aligned with the SD-FEC encoder codewords?

If so, the alignment function is not defined; it may be more appropriate to define the service interface in the Tx direction in terms of 128-bit codewords instead of bits on 8 lanes, such that the alignment is inherent.

If not, please clarify that the 128-bit blocks start point within the SD-FEC codeword is arbitrary.

A similar question holds for the Rx direction (based on the text in 155.3.3.8) - is the alignment of SD-FEC defined as a PMA function or a PCS function?

The title says "Symbol mapping to physical lanes", but in the text it is "coherent signal to physical lane mappings". The conversion of symbols to signals is done in the PMD.

Change "Four coherent signals" to "Four continuous signals". In 155.3.3.4.1 and in Table 155-7 change "coherent signal" to "symbol".

The signals IX/QX/IY/QX are just signals (per 155.3.3.4 and 156.1), and are not "coherent" by themselves. The coherency is part of the PMD.

The signals IX/QX/IY/QX are just signals (per 155.3.3.4 and 156.1), and are not "coherent" by themselves. The coherency is part of the PMD.
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**Comment ID: 85**

Ran, Adee  
Cisco  

**Comment Type:** T  
**Comment Status:** A  
rewritten by Ran, Adee, Cisco

"The encoding of 16QAM symbols is based on Table 155-2"  

This table does not define any encoding of input symbols - it defines mapping of bit tuples to output symbols.

"but with a higher resolution than 4 bits"

Resolution is for the digital representation of each analog value. The resolution here should be more than two bits (per dimension). The resolution seems to be left open to implementation.

This should be written more clearly. The suggested remedy is my attempt, but other text may be used.

**Suggested Remedy**

Change from
"The encoding of 16QAM symbols is based on Table 155-2 but with a higher resolution than 4 bits to enable the SD-FEC decoder to correct symbol errors"

to "The 16QAM symbols should be sampled with more than two bits per dimension, in order to enable the SD-FEC decoder to correct errors and recover the bits from the symbols based on the mapping in Table 155-2."

**Response**

**Response Status:** C  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment ID: 87**

Ran, Adee  
Cisco  

**Comment Type:** T  
**Comment Status:** A  
rewritten by Ran, Adee, Cisco

"comprising sixteen symbols encoded as shown in Table 155-2 but at a higher resolution than 8 bits"

SD-FEC codewords are by definition 128 bits; and table 155-2 shows mapping of bit tuples into output symbols.

Also, according to the next paragraph, the output of the process is a single stream of samples, not codewords.

This text seems to specify that the input to the decoder should be four streams of samples (combinations of X/Y and I/Q) with more than two bits per sample.

**Suggested Remedy**

Rewrite to clarify.

**Response**

**Response Status:** C  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment ID: 88**

Ran, Adee  
Cisco  

**Comment Type:** E  
**Comment Status:** A  
rewritten by Ran, Adee, Cisco

The subclause hierarchy below "State variables" is unnecessary, and includes subclauses that are not about state variables (155.4.2.2 through 155.4.2.4)

**Suggested Remedy**

Delete 155.4.2 and move its subclauses upper in the hierarchy (to become 55.4.2 through 155.4.5).

**Response**

**Response Status:** C  
ACCEPT IN PRINCIPLE.

See response to comment #346.
<table>
<thead>
<tr>
<th>Comment Type</th>
<th>Comment Status</th>
<th>Suggested Remedy</th>
<th>Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>A</td>
<td>The state diagram has several blocks in which text of assignment statements wraps to the next line. There is enough room to prevent that.</td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>The service interface of this PMD is not consistent with 116.3 because as it is written, the inputs and outputs are analog signals, not streams of discrete symbols.</td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>A</td>
<td>As described here the PMA sends digital symbols (discrete and sampled) from a set of 4 levels, not &quot;analog streams&quot; (which is an undefined term).</td>
<td></td>
</tr>
</tbody>
</table>

**Response**

- Resize blocks (changing layout if required) to prevent wrapping lines.
- Rewrite the text without referring to 116.3 (or make it "similar to 116.3 but...")
- Change "the PMA continuously sends four analog streams to the PMD" to "the PMA continuously sends four streams of quaternary symbols to the PMD".
- Change "the PMD then converts these four analog streams" to "the PMD then converts these streams of symbols".
- Rewrite "the PMD sends analog signals (continuous, to be sampled and digitized in the PMA)." to "the PMD continuously sends four analog signals to the PMA, corresponding to the optical signal received from the MDI".
- Change "the PMD continuously sends four analog streams to the PMA, corresponding to the signals received from the MDI" to "the PMD continuously sends four analog signals to the PMA, corresponding to the optical signal received from the MDI".

**Response**

- ACCEPT IN PRINCIPLE.
- ACCEPT IN PRINCIPLE.
Comment Type: T  Comment Status: A  rewrite bucket

I suspect that skew variation cannot exist at SP2 (PMD service interface), because the PCS and PMA are defined as operating in one clock domain, not as multiple lanes with separate logic. This may be worth mentioning (as done in other cases where skew variation can't exist, e.g. 140.3.2).

Is skew variation (as opposed to static skew) relevant on a single-lane, but coherent, PMD output?

If there is no skew variation between SP2 and SP3 then skew variation need not be specified at all.

Suggested Remedy
Add a statement that there is no skew variation at TP2.

If skew variation between the PMDs isn't relevant, change also the text about skew variation at SP3 and SP4, as in 140.3.2.

Response  Response Status: C
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment Type: T  Comment Status: A  rewrite bucket

Figure 80-8 applies to 100GBASE-R PHYs. The diagram for skew points for 400GBASE-R PHYs is in Figure 116–5.

Also, there SP0 and SP7 are not defined for 400GBASE-R PHYs.

Suggested Remedy
Change "at the points SP0 to SP7 shown in Figure 80-8" to "at the points SP1 to SP6 shown in Figure 116–5".

Response  Response Status: C
ACCEPT IN PRINCIPLE.

See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

Cl 155 SC 155.1.1 P 32 L 3 # 126
Nicholl, Gary Cisco Systems

Comment Type TR Comment Status A rewrite bucket
This is a single clause that covers both the PCS and PMA sublayers. Section 155.1 includes a summary of the PCS functions (in section 155.1.3). For consistency with previous standards I think this section should also include a summary of the PMA functions.

SuggestedRemedy
Add a new sub-section after 155.1.3 and before 155.1.4, to include a summary of the PMA functions.

Response Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.1.3 P 33 L 42 # 128
Nicholl, Gary Cisco Systems

Comment Type ER Comment Status A rewrite bucket
Item e) and f) mention SC-FEC, but there is no definition of "SC-FEC" in the definitions section (1.4).

SuggestedRemedy
Add a definition for "SC-FEC" into section 1.4 (unless it was added by a previous project).

Response Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.1.4 P 33 L 49 # 129
Nicholl, Gary Cisco Systems

Comment Type ER Comment Status A rewrite bucket
This section is under "overview" and is titled "Inter-sublayer interfaces". However it only mentions the inter-sublayer interfaces above and below the PCS. Shouldn't this section also cover the PMA inter-sublayer interfaces?

SuggestedRemedy
Add a description of the PMA inter-sublayer interfaces to this section.

Response Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.
It is not clear to me from reading the descriptions as to how the 400GBASE-ZR base frame (Figure 155-3), 400GBASE-ZR OH frame (Figure 155-4) and the SC-FEC frame (Figure 155-5) are related and aligned?

Suggested Remedy
Add a description or diagram to indicate how the various frame structures described in the comment are related and aligned (if indeed they are aligned).

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

The format of the text in Figure 155-8 is all over the place. I know in 802.3df we are using a constant font for all text in figures.

Suggested Remedy
Update Figure 155-8 to use a constant font for all text.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Why is the approximate sign used in the term "(512/511) x (5485/5140) x (5488/5485) x (128/119) x ~50.212875 Gb/s^20 ppm"? Isn't the nominal signaling rate known exactly?

I don't remember seeing the "approximate" sign used in other IEEE standards when referring to the nominal signaling rate?

Suggested Remedy
This is more of a question of clarification?

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.
The sentence states "Each super-frame is made up of 49 sub-frames ..: This is unusual terminology as a super-frame (or multi-frame) is usually made of n frames (and not sub-frames). This also begs the question as to why "super-frame" is used instead of the more usual "multi-frame".

Suggested Remedy
Propose changing "super-frame" to "multi-frame" and "sub-frame" to "frame" throughout this section. An alternative would be to use "frame" and "sub-frame".

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

The first sentence states "On each polarization, the stream of symbols is converted to four analog signals per symbol: IX, QX, IY, and QY......". This makes it sound like that they are four analog signals per symbol per polarization (making 8 in total).

I thought IX and QX formed one 16QAM symbol on one polarization (the X polarization) and IY and QY formed one 16QAM symbol for the other polarization (the Y polarization).

Suggested Remedy
Rewrite the text to make it clear that there are not four analog signals (IX, QX, IY, QY) for each polarization (which would mean 8 analog signals in total), but instead there are two analog signals (IX, QX) per symbol for the X polarization and two analog signals (IY, QY) per symbol for the Y polarization.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.
<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Page</th>
<th>Comment</th>
<th>Comment Type</th>
<th>Response</th>
<th>Response Status</th>
<th>Comment Status</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>141</td>
<td>61</td>
<td>CL 155</td>
<td>TR</td>
<td></td>
<td></td>
<td>A</td>
<td>Definition of variable &quot;faws_lock&lt;x&gt;&quot;. A number of issues here. Firstly the text states that &quot;...receiver has detected the location of the FAW for a given lane on the PMA service interface.&quot;. There is no &quot;FAW&quot; on the &quot;PMA service interface&quot; (i.e. the interface above the PMA sublayer) as the FAW is inserted/removed by the PMA sublayer itself. I think what is meant here is the &quot;PMD service interface&quot; and not the &quot;PMA service interface&quot;? Secondly the description states &quot;...where x=0-3&quot;. This suggests that there are four separate FAWs being located to, whereas according to section 155.3.3.3 and Figure 155-10 there is only a single FAWs inserted per polarization, so one FAW for X polarization and one FAW for Y polarization. Suggested Remedy: Correct the reference to the PMD service interface (if the assumption in the comment is correct) and explain why there are 4 &quot;faws_lock&lt;x&gt;&quot; boolean variables when according to section 155.3.3.3 there are only two FAWs (one for X polarization and one for Y polarization). Response</td>
</tr>
<tr>
<td>142</td>
<td>61</td>
<td>CL 155</td>
<td>ER</td>
<td></td>
<td></td>
<td>A</td>
<td>Definition of &quot;faw_valid&quot;. The references to &quot;Table 155-3&quot; and section &quot;155.3.3.1&quot; are not active cross-references. Suggested Remedy: Correct cross-references. Response</td>
</tr>
<tr>
<td>143</td>
<td>67</td>
<td>CL 155</td>
<td>TR</td>
<td></td>
<td></td>
<td>A</td>
<td>In Table 155-8 there are several MDIO control variables associated with &quot;FEC degraded SER&quot; processing, but I can find no description of FEC degraded SER processing in the draft? For 400GBASE-R the FEC degrade SER processing is associated with the RS544 FEC and based on monitoring for RS symbol errors within a given time interval (as described in section 119.2.5.3). If we want to do something similar for 400GBASE-ZR then the &quot;FEC degrade&quot; monitoring should be based on monitoring a combination of the SD-FEC and SC-FEC. Suggested Remedy: Define a FEC degrade monitoring scheme for 400GBASE-ZR (similar to what was done in section 119.2.5.3 for 400GBASE-R). Response</td>
</tr>
</tbody>
</table>
Table 155-9 provides FEC corrected and uncorrected codeword counts for the SC-FEC. Should there be similar monitoring for the SD-FEC? This is missing in the current draft.

Suggested Remedy
Define FEC monitoring for the SD-FEC.

ACCEPT IN PRINCIPLE.

See response to comment #346.

Table 155-9 has a MDIO variable called "SC-FEC AM lock," which refers to a PCS/PMS variable "amps_locked." However, when I look in section 155.4.2 (state variables), "amps_lock" is based on locking onto the alignment marker (AM). But then in Figure 155-2 it appears that the "AM detect" block should be the "SC-FEC decoding" block, so how can "amps_lock" be used to lock onto the SC-FEC frame? Are the AM frames and the SC-FEC frames aligned, and is the AM used by the SC-FEC decoding block to lock onto the SC-FEC frame?

Suggested Remedy
This is simply a question for clarification. Depending on the answer, changes may or may not be required in the draft.

ACCEPT IN PRINCIPLE.

See response to comment #346.
As a first time reader of this section, the term "stuff" and its use in this sub-clause is difficult to follow. It took me a while to understand what "stuff" was. In this case, I interpret "stuff" to mean non-data blocks or stuffing blocks. The last two paragraphs of the sub-clause could use wording improvements to make it clearer to the reader.

In the second to last paragraph, change:
"Each 1028-bit GMP word is either filled with data (the logically serialized 257B encoded stream produced according to 155.2.4.2) or stuff, which is transmitted as zero and ignored on receipt." to
"Each 1028-bit GMP word is either filled with data bits (the logically serialized 257B encoded stream produced according to 155.2.4.2) or stuffing blocks, which is transmitted as zero and ignored on receipt."

In the last paragraph, change:
"While the GMP mechanism is generic, the particular clock rates and tolerances for this application result in only five cases, allowing the positions of data and stuff to be pre-computed." to
"While the GMP mechanism is generic, the particular clock rates and tolerances for this application result in only five cases, allowing the positions of data blocks and stuffing blocks to be pre-computed."

Update title of Table 155-1 to:
"GMP stuffing block locations in 400GBASE-ZR frame"

In Table 155-1, change column header from:
"GMP word numbers of stuff locations"
to
"GMP word numbers of stuffing block locations"

In Table 155-1, change column header from:
"(row, column) of stuff location starting bits"
to
"(row, column) of stuffing block starting location"

When using an Extender, the PCS is connecting to the 400GMII in theory. This sentence does not express this - Optionally the upper interface may connect to a 400GMII Extender, defined in Clause 118, which then connects to the Reconciliation Sublayer.

Delete noted sentence.
The inclusion of the word FEC in this sentence implies that the only encoding is FEC -
The PMA Service Interface supports the exchange of FEC encoded data between the PCS
and PMA sublayer.
There is also the 64B/66B encoding.

Suggested Remedy
delete the word FEC.

Response
Response Status W
ACCEPT IN PRINCIPLE.
See response to comment #346.

The following is stated -
When communicating with the PMA in the transmit direction, the 400GBASE-ZR PCS
provides eight digital lanes, which the PMA encodes into two streams of 16QAM symbols.

What are eight digital lanes? Isn't this just the PMA Service Interface?

Suggested Remedy
Reword
Transmit data-units are sent to the PMA service interface via the
PMA-IS_UNITDATA_i.request primitive. The PMA then encodes the data into two streams
of 16QAM symbols.

Response
Response Status C
ACCEPT IN PRINCIPLE.
See response to comment #346.

MFAS is not listed in abbreviations

Suggested Remedy
Add to 1.5

MFAS Multi-frame alignment signal

Response
Response Status C
ACCEPT IN PRINCIPLE.
See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

Cl 155  SC 155.2.1  P 36  L 22  # 190
D'Ambrosia, John  Futuurewei, US Subsidiary of Huawei
Comment Type  TR  Comment Status  A  rewrite bucket
This line has inner and outer FEC codes reversed -
The transmit data is encoded with a concatenated forward error correction (CFEC) code consisting of an inner SC-FEC code and an outer Hamming code SD-FEC.

SuggestedRemedy
Modify noted sentence -
The transmit data is encoded with a concatenated forward error correction (CFEC) code consisting of an outer SC-FEC code and an inner Hamming code SD-FEC.

Response  Response Status  W  ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 156  SC 156.3.2  P 75  L 44  # 193
D'Ambrosia, John  Futuurewei, US Subsidiary of Huawei
Comment Type  TR  Comment Status  A  rewrite bucket
It is unclear if the skew constraints need to be revisited in light that the part is not part of 400GBASE-R family, but current pointer is to 80-8, which is for 100G

SuggestedRemedy
Revisit skew constraints as needed.
The diagram reference should be 116-4.

Response  Response Status  C  ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 155  SC 155.3.3.4.1  P 58  L 39  # 191
D'Ambrosia, John  Futuurewei, US Subsidiary of Huawei
Comment Type  E  Comment Status  A  rewrite bucket
This sentence appears to include unnecessary information -
Note that interleaving of signals by polarization is not allowed since this would add a non-essential level of complexity to the Rx digital processing.

SuggestedRemedy
modify sentence to
Note that interleaving of signals by polarization is not allowed.

Response  Response Status  C  ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 155  SC 155.5.1  P 68  L 30  # 194
D'Ambrosia, John  Futuurewei, US Subsidiary of Huawei
Comment Type  TR  Comment Status  A  rewrite bucket
Why is there a reference to a PCS lane alignment status? There are no PCS lanes in the 400GBASE-ZR PHY

SuggestedRemedy
Looks like this was intended to be PMA lane alignment status

Response  Response Status  C  ACCEPT IN PRINCIPLE.
See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

Comment ID 202

Huber, Thomas
Nokia

Comment Type TR
Comment Status A
rewrite bucket

There is inconsistency wording between Figure 155-2 (which shows m lanes in the receive direction between the PMA and PCS), the text in 155.2.1 (which indicates two streams of m-bit symbols), and text in 155.2.5.1 and in 155.3 2 (both of which reference DP-16QAM symbols digitized to m-bit resolution).

Suggested Remedy:
Change
"When communicating with the PMA in the receive direction, the 400GBASE-ZR PCS receives two streams of digitally encoded m-bit 16QAM symbols." to
"When communicating with the PMA in the receive direction, the 400GBASE-ZR PCS receives digitally encoded m-bit DP-16QAM symbols."

Response Response Status W
ACCEPT IN PRINCIPLE.
See response to comment #346.

Comment ID 203

Huber, Thomas
Nokia

Comment Type T
Comment Status A
rewrite bucket

The two paragraphs of 155.2.4.1 jump back and forth between 66b and 257b blocks in a way that could confuse a reader who is unfamiliar with the details of the clause 119 PCS.

Suggested Remedy:
Rewrite the text as follows:
The transmit PCS generates 66-bit blocks based upon the TXD<63:0> and <TXC<7:0> signals received from the 400GMII, as specified in the transmit state diagram shown in Figure 119-14. One 400GMII data transfer is encoded into one 66-bit block. The contents of each block are contained in a vector tx-coded<65:0>, which is passed to the 64B/66B to 256B/257B transcoder. tx-coded<1:0> contains the sync header and the remainder of the bits contain the block payload. The rate matching described in 119.2.4.1 is not required for the 400GBASE-ZR PCS because the mapping of the transcoder block stream into the 400GBASE-ZR frame structure performs clock compensation between the two clock domains.

Response Response Status C
ACCEPT IN PRINCIPLE.
See response to comment #346.

Comment ID 204

Huber, Thomas
Nokia

Comment Type TR
Comment Status A
rewrite bucket

Clause 9.4.3.2 of ITU-T G.709 does not discuss GMP. Since the GMP OH being used aligns with 400ZR, maybe it is better to point to 155.2.4.5.3 (which then points to the OIF 400ZR IA). ITU-T G.709 and G.709.x don't specifically discuss the GMP encoding that is used in 400ZR and 400GBASE-ZR.

Suggested Remedy:
Change
The principles of the GMP mapper are described in ITU-T G.709 (06/2020) Annex D, with details of the encoding of the GMP overhead in ITU-T G.709 Clause 9.4.3.2.

Response Response Status W
ACCEPT IN PRINCIPLE.
See response to comment #346.
This text could be clarified. GMP is converting from the clock domain of the payload (stream of 257b blocks) to the clock domain of the 400GBASE-ZR frame. Presumably the payload blocks are already aligned to the payload clock.

SuggestedRemedy
Rewrite as follows: The AM, pad, and OH fields are populated after the GMP mapping process has rate-matched the 257B block stream to the payload area of the 400GBASE-ZR frame.

Response  Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

The 'nD' in CnD(t) should be subscripted

SuggestedRemedy
Change the nD to subscript.

Response  Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

The convolutional interleaver and Hamming encoder are working with 10976 rows, but figure 155-7 indicates 10970 rows

SuggestedRemedy
Change 10970 to 10976 in Figure 155-7.

Response  Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

awkward grammar in the first sentence

SuggestedRemedy
Change "... adapt between the PCS layer digital symbols to and from the four analog signals." to "... adapt the PCS layer digital signals to and from the four analog signals."

Response  Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

**Comment ID 215**

Huber, Thomas
Nokia

**Comment Type** TR  **Comment Status** A  **rewrite bucket**

The intended interleaving is that first symbol of each of 16 codewords is transmitted, then the second symbol, etc. The example is not consistent with that - S(0,1) should follow S(0,2) (as seen in figure 155-11).

**SuggestedRemedy**

Change S0.2 to S1.1

**Response**  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment ID 216**

Huber, Thomas
Nokia

**Comment Type** T  **Comment Status** A  **rewrite bucket**

There is a horizontal line missing between the second and third sets of symbols in Figure 155-11

**SuggestedRemedy**

Add the missing line

**Response**  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment ID 217**

Huber, Thomas
Nokia

**Comment Type** TR  **Comment Status** A  **rewrite bucket**

In the GET_BLOCK state, the variable slip_done should be faw_slip_done

**SuggestedRemedy**

Change slip_done to faw_slip_done

**Response**  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment ID 224**

Law, David
Hewlett Packard Enterprise

**Comment Type** E  **Comment Status** A  **rewrite bucket**

The terms 'overhead fields' (page 36, line 40) and 'OH fields' (page 38, line 46), 'OH bytes' (page 38, line 2) then 'OH blocks' on the next line, and 'GMP overhead' (page 38, line 12), seem to be used interchangeable.

**SuggestedRemedy**

Please use a consistent term, 'overhead field' seems to be the most common.

**Response**  
ACCEPT IN PRINCIPLE.

See response to comment #346.

**Comment ID 225**

Law, David
Hewlett Packard Enterprise

**Comment Type** TR  **Comment Status** A  **rewrite bucket**

The only 'shall' statement regarding the PCS transmit path (155.2.4) is in subclause 155.2.4.9 'Frame synchronous scrambler', similarly the only 'shall' statement regarding the PCS receive path (155.2.5) is in subclause 155.2.5.3 'Descrambler' and 155.2.5.6 'CRC32 check and error marking'. Mandatory PCS transmit requirements, mandatory PCS receive requirements and other mandatory requirements need to be covered by 'shall' statements.

**SuggestedRemedy**

See comment.

**Response**  
ACCEPT IN PRINCIPLE.

See response to comment #346.
Subclause 155.2.4.3 'GMP mapper' says that 'The GMP mapper inserts the serialized stream of 257B blocks into the payload area of a 400GBASE-ZR frame.' and that 'The frame is illustrated as a structure with 256 rows of 10 280 bits with a logical transmission order of left to right, top to bottom.' This seems to imply that the stream of 257B blocks is inserted into one 400GBASE-ZR frame at a time.

Subclause 155.2.4.3 however then says that 'The Payload area of a four-frame multi-frame is divided into 10 220 GMP words ... encoded stream produced according to 155.2.4.2) ...'. This seems to imply that the 257B blocks are inserted into four 400GBASE-ZR frames, that form a single multi-frame, at a time.

Subclause '155.2.4.6 CRC32 and multi-block alignment signal (MBAS) insertion' then says 'The stream of 400GBASE-ZR frames, illustrated in Figure 155-3, provide the input ...' seems to imply 400BASE-ZR frames are formed one at a time, and does not reference multi-frames.

**Suggested Remedy**

Clarify the definition of a multi-frame, potentially through a figure, how 257B blocks are mapped to it, and how it is mapped to the SC-FEC message.

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Subclause 155.2.4.3 says 'The 400GBASE-ZR PCS payload is mapped ...' however this is the only use of the term '400GBASE-ZR PCS payload' in the draft.

**Suggested Remedy**

Suggest that the text 'The 400GBASE-ZR PCS payload is mapped ...' is changed to read 'The 400GBASE-ZR PCS payload of the serialized stream of 257B blocks is mapped ...'.

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.
Subclause 155.2.4.5.2 says 'The RPF bit indicates signal fail status was detected by the remote 400GBASE-ZR receive function ...' which seems to imply that the RPF bit is mapped from the SIGNAL_OK parameter of the PMA:IS_SIGNAL.indication primitive.

Suggested Remedy
If the RPF bit is mapped from the PMA:IS_SIGNAL.indication primitive, replace the second sentence of the second paragraph of subclause 155.2.4.5.2 with 'The bit is set based on the most recently received SIGNAL_OK parameter of the PMA:IS_SIGNAL.indication primitive. It is "0" if the value was OK and "1" if the value was FAIL.'.

If the RPF bit is not mapped from the PMA:IS_SIGNAL.indication primitive, please define where it is mapped from, or the conditions for when it is set and cleared.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Subclause 155.2.4.5.2 'Link status monitoring and signaling' says 'RPF is set to "1" to indicate a remote 400GBASE-ZR PHY defect indication' however there appears to be no definition of a 400GBASE-ZR PHY defect in the draft.

Suggested Remedy
Please provide a definition of the conditions considered a 400GBASE-ZR PHY defect.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

SIGNAL_OK is a parameter that is passed by the PMA:IS_SIGNAL.indication primitive.

Suggested Remedy
Suggest that '... the SIGNAL_OK primitive has the value FAIL.' should be changed to read '... the SIGNAL_OK parameter has the value FAIL.'.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Subclause 155.3.3 'Functions within the PMA' says 'The purpose of the PMA is to ... and optionally to provide test signals and loop-back.'.

There, however, doesn't appear to be any subclauses under subclause 155.3 'Physical Medium Attachment (PMA) sublayer, type 400GBASE-ZR' that define test signals or loop-back.

Suggested Remedy
Either add definitions defining test signals and loop back within the PMA or remove this text from subclause 155.3.3.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.
Subclause 155.3.3 'Functions within the PMA' says '... elements of a symbol, namely IX, QX, IY, or QY, ...', referencing IX, QX, IY, and QY as 'elements' of a DP-16QAM symbol.

Subclause 155.3.3.1 'Gray mapping and polarization distribution' says '- (c8i, c8i+1) maps to the in-phase (I) component of the X-polarization of si' referencing IX, QX, IY, and QY as 'components' of a DP-16QAM symbol.

**Suggested Remedy**

Suggest that either 'element' or 'component' be used consistently to describe IX, QX, IY, and QY used to form a DP-16QAM symbol.

**ACCEPT IN PRINCIPLE.**

See response to comment #346.

---

The terms 'DP-16QAM symbol' (e.g., page 52, line 32), 'Gray-coded signals' (e.g., page 52, line 44), SD-FEC codewords (e.g., page 53, line 36), 'Hamming code words' (e.g., page 52, line 53), and just 'code word' (page 53, line 32) seem to be used interchangeably in the subclauses of 155.3.3 'Functions within the PMA'. For example, subclause 155.3.3.2 'Symbol interleaving' says 'The DP-16QAM symbols are time interleaved ...' yet the following subclause 155.3.3.3 'Insert FAW, TS and PS symbols' says '... the stream of Gray mapped, interleaved symbols are ...'. It, however, appears the 'symbols' in both cases are the same.

**Suggested Remedy**

Suggest that a consistent terminology should be used for DP-16QAM symbols.

**ACCEPT IN PRINCIPLE.**

See response to comment #346.

---

The terms '128-bit code word' (e.g., page 52, line 32), 'FEC codeword' (e.g., page 52, line 44), SD-FEC codewords (e.g., page 53, line 36), 'Hamming code words' (e.g., page 52, line 53), and just 'code word' (page 53, line 32) seem to be used interchangeably to describe the 128-bit code word that is passed across the 8 lane PMA service interface to the PMA sublayer as 16 groups of 8.

**Suggested Remedy**

Suggest that the term ‘SD-FEC codeword’ be used consistently in subclause 155.3.3 to describe the 128-bit code word passed across the PMA service interface.

**ACCEPT IN PRINCIPLE.**

See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

# 239
Cl 155 SC 155.3.3.2 P 52 L 54 #
Law, David Hewlett Packard Enterprise

Comment Type T
Comment Status A
rewrite bucket

On page 52, line 54, the symbol number is in normal font whereas it is in subscript font in the remainder of subclause 155.3.3.2.

SuggestedRemedy
Suggest that, based on page 52, line 54, the symbol number should be in normal rather than subscript font in the rest of the subclause to make it clear the two numbers following 'S' separated by a comma are the code word number followed by the symbol number in the code word. Alternatively, perhaps it should be stated that two numbers following 'S' separated by a comma are the code word number followed by the symbol number in the code word.

Response Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.

# 240
Cl 155 SC 155.3.3.2 P 53 L 33 #
Law, David Hewlett Packard Enterprise

Comment Type TR
Comment Status A
rewrite bucket

According to 155.3.3.1 Gray mapping and polarization distribution the 'S' code word is an array of DP-16QAM symbols (page 52, line 35). As a result, aren't 'Symbols from eight code words [S0,...,S7] ...' (page 52, line 54) a total of 128 DP-16QAM symbols? This seems to be confirmed by Figure 155-11 'Eight-way Hamming code interleaver' which shows symbols S0,0 through S7,15 which is 128 symbols.

SuggestedRemedy
Suggest the text 'When the 64-symbol buffer is full ...' be changed to read 'When the 128-symbol buffer is full ...'.

Response Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.

# 241
Cl 155 SC 155.3.3 P 54 L 27 #
Law, David Hewlett Packard Enterprise

Comment Type TR
Comment Status A
rewrite bucket

There is no specification of how the output from PAM symbol interleaving function is mapped into the payload fields of the sub-frame of a super-frame.

SuggestedRemedy
Add a subclause to describe how the output of the PAM symbol interleaving function is mapped into the payload fields of the sub-frame of a super-frame.

Response Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.

# 242
Cl 155 SC 155.3.3 P 54 L 31 #
Law, David Hewlett Packard Enterprise

Comment Type T
Comment Status A
rewrite bucket

Subclause 155.3.3.3 'Insert FAW, TS and PS symbols' however says 'A super-frame is defined as a set of 181 888 symbols in each of the X and Y polarizations including ...'. Since a separate super-frame for each of the X and Y polarizations, the 'symbols' seem to be 16QAM symbols rather than DP-16QAM symbols.

SuggestedRemedy
Suggest that the text 'A super-frame is defined as a set of 181 888 symbols in each of the X and Y polarizations including 175 616 payload symbols and 6272 additional symbols.' be changed to read 'A super-frame is defined as a set of 181 888 16QAM symbols for each of the X and Y polarizations including 175 616 payload 16QAM symbols and 6272 additional 16QAM symbols.'

Response Response Status C
ACCEPT IN PRINCIPLE.

See response to comment #346.
The second paragraph of subclause 155.3.3.3 'Insert FAW, TS and PS symbols' says 'The first sub-frame of a super-frame includes ... 76 reserved symbols (rsvd<0:75> ...'; however, there is no specification of what 16QAM symbol should be transmitted for these reserved symbols.

Suggested Remedy
Define the 16QAM symbol to be transmitted for these 76 reserved symbols.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

The contents of the sub-frame 0 between P4 and P115, and sub-frame 1 and 48 between P2 and P115, are not defined in Figure 155-12.

For sub-frame 0, the number of symbols shown in Figure 155-12 after P0, P1, P2, P3 and P115 is 31. A sub-frame is 3712 symbols long, and there are 116 PS symbols, and since 3712/32 = 116 it seems reasonable to assume that there are 31 symbols after each PS symbol for sub-frame 0, but this needs to be specified.

For sub-frame 1, the number of symbols shown in Figure 155-12 after P0 is 31, after P1 is 31, however, after P115 it is 32. Similarly, for sub-frame 48, the number of symbols shown in Figure 155-12 after P0 is 42, after P1 is 31, and after P115 it is 32. It is therefore difficult to make an assumption about the number of symbols after each PS between P2 and P115, so this needs to be specified.

Suggested Remedy
Specify the contents of the sub-frame 0 between P4 and P115, and sub-frame 1 and 48 between P2 and P115.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.
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<td>It appears that the 10-bit interleaver isn't specified.</td>
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<td>Specify the 10-bit interleaver.</td>
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<td>rewrite bucket</td>
<td>Subclause 155.2.4.6 'CRC32 and multi-block alignment signal (MBAS) insertion' says that 'Each SC-FEC block has 119 x 10 280 / 5 bits = 244 664 bits.' but isn't an input SC-FEC block 244 736 bits, formed of 244 664 information bits, 32 CRC bits, 6 MBAS bits, and 34 bits of padding (see figure 155-5). In addition, based on figure 155-5 and subclause 155.2.4.7, subclause 155.2.4.6 describes the input SC-FEC block.</td>
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<td>Suggest that: [1] The first paragraph of subclause 155.2.4.6 should be changed to read 'The stream of 400GBase-ZR frames, illustrated in Figure 155-3, provide the information bits for the calculation of SC-FEC input blocks. To conform with the format of the input SC-FEC block, 119 rows from the stream of 400GBase-ZR frames are mapped to the information bits in 5 successive SC-FEC input blocks. Each SC-FEC input block has 119 x 10 280 / 5 bits = 244 664 information bits.'</td>
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<td>[2] The text '... cyclic redundancy code is calculated over 244 664 input bits as ...' in the second paragraph of subclause 155.2.4.6 should be changed to read '... cyclic redundancy code is calculated over the 244 664 information bits as ...'.</td>
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<td>[3] The term 'SC-FEC block' be changed to read 'SC-FEC input block' in subclause 155.2.4.6.</td>
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<td>Law, David Hewlett Packard Enterprise</td>
<td>T</td>
<td>rewrite bucket</td>
<td>Suggest that subclause 155.2.4.7 be retitled 'SC-FEC adapt and encoding' to match the equivalent block in Figure 155-2.</td>
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Cl/ 155 SC 155.2.4.7 P 41 L 11 # 252
Law, David Hewlett Packard Enterprise

Comment Type E Comment Status A rewrite bucket

Subclause 155.2.4.7 ‘400GBASE-ZR frame to SC-FEC adaptation’ says ‘... which are added to the 400GBASE-ZR SC-FEC frame as ...’. This seems to be the only time the term ‘400GBASE-ZR SC-FEC frame’ is used and the title of the referenced figure 155-6 is ‘400GBASE-ZR SC-FEC encoded frames’.

Suggested Remedy
Both instances of block 7.11 in figure 155-6 are marked with an asterisk which, I assume, is meant to reference a footnote that says that only the information bits of block 7.11 are included, that the CRC32 and MBAS bits are appended after the parity bits, and the pad is discarded.

Suggested Remedy
Add a new paragraph to subclause 155.4.7 to specify the mapping of the CRC32 and MBAS bits from block 7.11 and add a suitable footnote to figure 155-6.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl/ 155 SC 155.2.4.7 P 42 L 11 # 254
Law, David Hewlett Packard Enterprise

Comment Type T Comment Status A rewrite bucket

There is no specification of how the 8 parity blocks are mapped into bits 10280 to 10970 of the 400GBASE-ZR SC-FEC encoded frames.

Suggested Remedy
Add a new paragraph to subclause 155.4.7 to specify the mapping of the 16384 parity bits into bits 10280 to 10970 of the 400GBASE-ZR SC-FEC encoded frames.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl/ 155 SC 155.2.4.7 P 43 L 20 # 255
Law, David Hewlett Packard Enterprise

Comment Type E Comment Status A rewrite bucket

Subclause 155.2.4.7 ‘400GBASE-ZR frame to SC-FEC adaptation’ says ‘... which are added to the 400GBASE-ZR SC-FEC frame as ...’. This seems to be the only time the term ‘400GBASE-ZR SC-FEC frame’ is used and the title of the referenced figure 155-6 is ‘400GBASE-ZR SC-FEC encoded frames’.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl/ 155 SC 155.2.4.10 P 43 L 22 # 256
Law, David Hewlett Packard Enterprise

Comment Type T Comment Status A rewrite bucket

IEEE Std 802.3 doesn't specify implementations.

Suggested Remedy
Suggest, based on the in subclause 155.2.4.9 above (page 43, line 8), that the text The convolutional interleaver is described in ITU-T G.709.3 subclause 15.4.3. It contains 16 parallel delay lines that are accessed sequentially for each block of 119 bits.’ is changed to read ‘The convolutional interleaver shall be functionally equivalent to the convolutional interleaving process described in ITU-T G.709.3 subclause 15.4.3’.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

Comment ID: 257
Law, David
Hewlett Packard Enterprise

Cl 155 SC 155.2.4.11 P 44 L 36

Comment Type: T  Rewrite bucket
Comment Status: A

Suggested Remedy
Subclause seems to use the terms '119b', '119-bit block' and '119-bit message' interchangeably. Suggest that '119-bit message' is used to match subclause 155.2.5.1.

Suggested Remedy
[Suggest that:
1] The text 'The 119b outputs of the convolutional interleaver are encoded ...' is changed to read 'The 119-bit messages output by the convolutional interleaver are encoded ...'
2] The text '... to each of the 10 976 119-bit blocks as output ...' is changed to read '... to each of the 10 976 119-bit messages as output ...'.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Comment ID: 258
Law, David
Hewlett Packard Enterprise

Cl 155 SC 155.2.4.11 P 44 L 40

Comment Type: T  Rewrite bucket
Comment Status: A

Suggested Remedy
The 128-bit code word referenced in subclause 155.2.4.11 'Hamming SD-FEC encoder' is called the 'SD-FEC codeword' in Figure 155-8, subclause 155.2.5.1 (page 46, line 5) and subclause 155.3.3.2 (page 53, line 36). Suggest the same terminology should be used in subclause 155.2.4.11 'Hamming SD-FEC encoder'.

Suggested Remedy
[Suggest that:
1] The text '... results in 10 796 128-bit blocks.' be changed to read '... results in 10 796 128-bit SD-FEC codewords.'
2] The text '... is encoded to the 128-bit code word ...' be changed to read '... is encoded to the 128-bit SD-FEC codeword ...'.
3] The text 'The 128-bit code words are ...' should be changed to read 'The 128-bit SD-FEC codewords are ...'.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Comment ID: 259
Law, David
Hewlett Packard Enterprise

Cl 155 SC 155.2.4.12 P 45 L 50

Comment Type: T  Rewrite bucket
Comment Status: A

Suggested Remedy
Suggest that Figure 155-8 and the last paragraph of subclause 155.2.4.11 be updated to describe how the 128-bit code word from the SD-FEC encoder is passed across the PMA service interface. In addition, the fourth paragraph of subclause 155.3.3.1 should be updated to note that the 128-bit code word is passed across the PMA service interface to the PMA where the Gray mapping and polarization distribution described occurs.

Suggested Remedy
[Suggest that the PMA service interface be added to Figure 155-8. To do this suggest that the label 'PMA:IS_UNIDATA_0.request' be added to the leftmost arrow at the bottom of the figure, with the label 'PMA:IS_UNIDATA_1.request' and 'PMA:IS_UNIDATA_2.request' staggered above on the next two arrows to the right. The label 'PMA:IS_UNIDATA_7.request' should be added to the rightmost arrow. As an existing example, see Figure 119-10 '200GBASE-R Transmit bit ordering and distribution'.

2] Suggest that the last paragraph of subclause 155.2.4.11 be changed to read 'The 128-bit code word is then passed across the 8 lane PMA service interface to the PMA sublayer as 16 groups of 8 bits, each representing a DP-16QAM symbol. The first group of 8 bits are c0 through c7, the last group of 8 bits are c120 through c127, with the LSB through the MSB or each group of 8 bits mapped in order to the tx_symbol parameter of the PMA:IS_UNIDATA_0.request through the PMA:IS_UNIDATA_7.request primitive respectively (see Figure 155-8)'.

3] Suggest that the text 'Each 128-bit code word from the SD-FEC encoder c = [c0, c1, ...c127], is mapped ...' in the fourth paragraph of subclause 155.3.3.1 should be changed to read 'Each 128-bit code word from the SD-FEC encoder is passed across the PMA service interface as described in 155.2.4.11. Each 128-bit code word c = [c0, c1, ....c127], is mapped ...'.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.

Comment ID: 259
Law, David
Hewlett Packard Enterprise

Cl 155 SC 155.2.4.12 P 45 L 50

Comment Type: T  Rewrite bucket
Comment Status: A

Suggested Remedy

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.
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Comment Type: E  Comment Status: A  rewrite bucket

The vast majority of references to the in-phase and quadrature-phase X and Y polarization use the symbols I<subscript>X</subscript>, Q<subscript>X</subscript>, I<subscript>Y</subscript>, and Q<subscript>Y</subscript> (e.g., Figure 155-10 on page 51, line 28 and subclause 155.3.3, page 52, line 9). There, however, seem to be a few instances where the X and Y are not in subscript, or the phase and polarization symbols are reversed.

Suggested Remedy

On the assumption that they are referencing the same signals, please use I<subscript>X</subscript>, Q<subscript>X</subscript>, I<subscript>Y</subscript>, and Q<subscript>Y</subscript> in the following locations:

- Subclause 155.2.5.1, page 46, line 12
- Table 155-3, page 55, line 38
- Table 155-4, page 56, line 35
- Table 155-7, page 59, line 5 through 16

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment Type: E  Comment Status: A  rewrite bucket

Since [1] the subclause of 156.5 'PMD functional specifications' lists more than just a transmit and receive function, and [2] to parallel the text 'The PMA allows the 400GBASE-ZR PCS (specified in 155.2) ...' suggest that '... media-independent way to a coherent transmitter and receiver specified in Clause 156.' should be changed to read '... media-independent way to the 400GBASE-ZR PMD (specified in 156).'

Suggested Remedy

See comment.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.
Subclause 155.2.4.11 ‘Hamming SD-FEC encoder’ says that ‘The 128-bit code words are sent as 8-bit symbols to the 400GBASE-ZR PMA sublayer on the PMA:IS_UNITDATA_0.request to PMA:IS_UNITDATA_7.request inter-sublayer signals.’ Further, subclause 155.2.5.1 ‘Hamming SD-FEC decoder’ says ‘The incoming DP-16QAM symbols are digitized to an m-bit resolution by the PMA sublayer receive direction (see 155.3.3.5) and provided to the PCS receive direction by PMA:IS_UNITDATA_0.indication to PMA:IS_UNITDATA_m-1.indication inter-sublayer signals.’ and that ‘The Hamming SD-FEC decoder is a soft decision decoder and so requires a higher resolution than 2 bits / 4 levels for each of the signals XI, XQ, YI, and YQ.’. Finally, Figure 155-10 ‘400GBASE-ZR PMA functional block diagram’ says ‘m is implementation dependent and is the number of bits of resolution of the DP-16QAM symbols.’

Rather than operating as n parallel asynchronous PCS lanes that carry alignment markers and lane numbers that enable the original data to be restored or n lanes to be multiplex into m lanes, it appears the 400GBASE-ZR PMA service interface between the PCS and the PMA operates as an n-bit synchronous data path, transferring a single DP-16QAM symbol during each operation. This is confirmed by clause 155.2.4.11 ‘GMP mapper’ that says ‘... 400GBASE-ZR frames are not mapped to 16 PCS lanes ...’. In the case of the transmit path, the DP-16QAM symbols are encoded as 8-bit words, 2 bits representing the 4 levels for each of the in-phase and quadrature components of the X and Y polarizations. In the case of the receive path, the DP-16QAM symbols are encoded as p bits representing q levels, where p and q are implementation dependant.

It, therefore, doesn't seem correct to define the 400GBASE-ZR PMA service interface through reference to the lane-based PMA service interface definition in 116.3 when it doesn't support the features of a lane-based service interface. Based on this, suggest that the 400GBASE-ZR PMA service interface be defined using a single .request and .indicate primitive, with a tx_symbol and rx_symbol parameter respectively, to reflect the synchronous data path nature of the interface.

Suggested Remedy

Specify the 400GBASE-ZR PMA as a single .request and .indicate primitive, with a tx_symbol and rx_symbol parameter respectively as follows:

- Change the three instances of 'PMA:IS_UNITDATA_i.request' to read 'PMA_UNITDATA.request' in subclause 155.2.1 'Functions within the PCS'.

- Change subclause 155.1.4.2 'Physical Medium Attachment (PMA) service interface' to read as follows:

The 400GBASE-ZR PMA service interface provided by the 400GBASE-ZR PMA for the 400GBASE-ZR PCS is described in an abstract manner and does not imply any particular implementation. The 400GBASE-ZR PMA Service Interface supports the exchange of encoded DP-16QAM symbols between the PCS and PMA sublayer. The 400GBASE-ZR PMA service interface is defined in 155.3.2.

- Change the last paragraph of subclause 155.2.4.11 'Hamming SD-FEC encoder' to read:

The 128-bit code words are sent as 8-bit encoded DP-16QAM symbols to the 400GBASE-ZR PMA sublayer using sixteen PMA_UNITDATA.request messages.

- Change the text ‘...’ by PMA:IS_UNITDATA_0.indication to PMA:IS_UNITDATA_m-1.indication inter-sublayer signals.’ to read ‘... by the PMA_UNITDATA.indication primitive.’ in subclause 155.2.5.1 ‘Hamming SD-FEC decoder’.

- Change subclause 155.3.2 '400GBASE-ZR PMA service interface', adding new subclauses 155.3.2.1 through 155.3.2.2.3, to read:

155.3.2 400GBASE-ZR PMA service interface

The 400GBASE-ZR PMA Service Interface supports the exchange of encoded DP-16QAM symbols between the PCS and PMA sublayer. The inter-sublayer 400GBASE-ZR PMA service interface is described in an abstract manner and does not imply any particular implementation. The inter-sublayer service interface primitives are defined as follows:

PMA_UNITDATA.request

This primitive defines the transfer of encoded DP-16QAM symbols in the tx_symbol parameter from the 400GBASE-ZR PCS to the 400GBASE-ZR PMA. The PMA_UNITDATA.indication primitive is used to define the transfer of signal status from the 400GBASE-ZR PMA to the 400GBASE-ZR PCS.

155.3.2.1 PMA_UNITDATA.request

This primitive defines the transfer of encoded DP-16QAM symbols in the tx_symbol parameter from the 400GBASE-ZR PCS to the 400GBASE-ZR PMA.

155.3.2.1.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symbol)

During transmission, the PMA_UNITDATA.request simultaneously conveys 8 bits of a 128-bit code word generated by the SD-FEC encoder (see 155.2.4.11) representing an encoded DP-16QAM symbol to the PMA. The encoding used for the in-phase and quadrature-phase components of the X and Y polarization is defined in subclause 155.3.3.1.
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155.3.2.1.2 When generated

The PCS generates sixteen PMA_UNITDATA.request messages for each 128-bit code word from the PCS SD-FEC encoder. The messages convey the least significant octet C<7:0> first, most significant octet C<127:120> last, with code word bits C<n+7:n> mapped to tx_symbol<7:0>. The nominal rate of PMA_UNITDATA.indication messages is 57.78 Gb/s.

155.3.2.1.3 Effect of receipt

The PCS continuously forms the tx_symbol parameters received in sixteen consecutive PMA_UNITDATA.indication messages into 128-bit code words that are passed to the PCS Gray mapping and polarization distribution function (see 155.3.3.1).

155.3.2.2 PMA_UNITDATA.indication

This primitive defines the transfer of encoded DP-16QAM symbols in the rx_symbol parameter from the 400GBASE-ZR PMA to the 400GBASE-ZR PCS.

155.3.2.2.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symbol)

During reception, the PMA_UNITDATA.indication simultaneously conveys m bits of an n-bit code word generated by the symbol de-interleaving function (see 155.3.3.8) representing an encoded DP-16QAM symbol to the 400GBASE-ZR PCS where m is implementation dependent, representing the number of bits of the encoded DP-16QAM symbol, and n = 16 x m.

155.3.2.2.2 When generated

The PCS generates sixteen PMA_UNITDATA.indication messages for each n-bit code word generated by the PMA symbol de-interleaving function. The messages convey the least significant m bits of the n-bit code word first. The nominal rate of PMA_UNITDATA.indication messages is 57.78 Gb/s.

155.3.2.2.3 Effect of receipt

The PCS continuously forms the rx_symbol parameters received in sixteen consecutive PMA_UNITDATA.indication messages into n-bit code words that are passed to the PCS Hamming SD-FEC decoder function (see 155.2.5.1).

155.3.2.3 PMA_SIGNAL.indication

This primitive defines the transfer of the status of the PMA receive process in the SIGNAL_OK parameter from 400GBASE-ZR PMA to the 400GBASE-ZR PCS.

155.3.2.3.2 When generated

The PMA generates a PMA_SIGNAL.indication message whenever there is change in the value of the SIGNAL_OK parameter (see 155.3.3.9).

155.3.2.2.3 Effect of receipt

The PMA_Signal Indicator Logic monitors the PMA_SIGNAL.indication primitive for a change in the SIGNAL_OK parameter (see 155.2.1).

- Move the last paragraph of the current subclause to a new subclause 155.3.3.9 titled 'Signal Indication Logic (SIL)'.

- Change the last paragraph of subclause 155.3.3.8 'Polarization combining and symbol de-interleaving' to read:

The sixteen encoded DP-16QAM symbols are transferred to the 400GBASE-ZR PCS sublayer as m-bit DP-16QAM symbols using sixteen PMA_UNITDATA.indication messages.

- Change 'PMA:IS_UNITDATA_0.request to PMA:IS_UNITDATA_7.request' to read 'PMA_UNITDATA.request' and 'PMA:IS_UNITDATA_0.indication to PMA:IS_UNITDATA_7.indication' to read 'PMA_UNITDATA.indication' in Figure 155-2 'Functional block diagram'.

- Change 'PMA:IS_UNITDATA_0.request to PMA:IS_UNITDATA_7.request' to read 'PMA_UNITDATA.request' and 'PMA:IS_UNITDATA_0.indication to PMA:IS_UNITDATA_7.indication' to read 'PMA_UNITDATA.indication' in Figure 155-10 '400GBASE-ZR PMA functional block diagram'.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

Cl 155 SC 155.3.2 P 50 L 3 # 264

Law, David Hewlett Packard Enterprise

Comment Type E Comment Status A rewrite bucket

Since subclause 155.3.2 only summarizes the primitives, a cross reference to where they are defined should be added.

Suggested Remedy

Suggest that 'The 400GBASE-ZR PMA service interface is provided ...' should be changed to read 'The 400GBASE-ZR PMA service interface (see 155.1.4.2) is provided ...'.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.3.2 P 50 L 16 # 265

Law, David Hewlett Packard Enterprise

Comment Type T Comment Status A rewrite bucket

Subclause 155.3.2 says '... sends eight parallel bit streams to the PMA, each at a nominal signaling rate of ...'. Since this is a signalling rate, the unit of measurement should be in Bd rather than Hz (see the following paragraph).

Suggested Remedy

Suggest that '... ~50.212875 Gb/s +/-20 ppm (~57.78 Gb/s).' should read '... ~50.212875 GBd +/-20 ppm (~57.78 GBd)' (where +/- is a plus-minus symbol).

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl 155 SC 155.3.2 P 51 L 18 # 266

Law, David Hewlett Packard Enterprise

Comment Type E Comment Status A rewrite bucket

There is a rectangle to the right of the 'Carrier phase recovery', 'PMD equalizer' and 'chromatic dispersion equalizer' within the 400GBASE-ZR PMA sublayer box in Figure 155-10 '400GBASE-ZR PMA functional block diagram' that is unlabelled.

Suggested Remedy

Either label the rectangle or delete it.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 267

Subclause 155.3.3.4.1 says that 'All of the coherent signal to physical lane mappings in Table 155-7 are allowed for the Tx signal. This is because receivers can determine which physical lane is carrying which signal based on the contents of the FAW'. As a result, it seems that the in-phase and quadrature-phase components of the X and Y polarizations can be mapped to the receive PMD service interface primitives in any of the eight ways listed in Table 155-7.

Further, subclause 155.3.3.7 'FAW, TS, and PS symbol removal' says 'The 400GBASE-ZR PMA receive path attains alignment lock to the 22-symbol FAW that is transmitted on each of the two transmission polarizations on the in-phase and quadrature-phase lanes.' and 'When the X and Y polarization symbol streams are identified and aligned to the super-frame format of Figure 155-12, the FAW, TS, and PS symbols are removed ...'. As a result, it seems the X and Y polarizations identification is performed by the FAW lock function, and pilot removal occurs after the FAW lock function.

Suggested Remedy

[1] Suggest that the labels 'IX', 'QX', 'IY' and 'QY' be removed from below the 'ADC' block in Figure 155-10.

[2] Suggest that the Pilot removal (X) Pilot removal (Y) block be removed from Figure 155-10.

[3] Suggest that the label 'Align CFEC and FAW/TS symbols (X) remove' be changed to read:

FAW alignment
Remove FAW, PS, TS symbols

[4] Suggest that the label 'Align CFEC and FAW/TS symbols (Y) remove' be changed to read:

FAW alignment
Remove FAW, PS, TS symbols

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

Law, David
Hewlett Packard Enterprise

Comment Type: E
Comment Status: A
SuggestedRemedy

Comment ID: 268

Suggest that ‘... through a signal indication logic (SIL) that reports ...’ should read ‘... through a signal indication logic (SIL) function that reports ...’.

SuggestedRemedy
See comment.

ACCEPT IN PRINCIPLE.
See response to comment #346.

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Law, David
Hewlett Packard Enterprise

Comment Type: TR
Comment Status: A
SuggestedRemedy

Subclause 155.3.2 '400GBASE-ZR PMA service interface' says that 'The PMA:IS_SIGNAL.indication primitive is generated through a signal indication logic (SIL) that reports signal health based on receipt of the PMD:IS_SIGNAL.indication from the 400GBASE-ZR PMD sublayer, data being processed successfully by the signal processing functions, and symbols being sent to the PCS on all of the output lanes.' however subclause 156.5.4 'PMD global signal detect function' says that 'The PMD global signal detect function shall set the state of the SIGNAL_DETECT parameter to a fixed OK value.' and that 'The presence of a valid signal is determined only by the 400GBASE-ZR PCS (see 155.2.1).'. In addition, subclause 155.2.1 says 'The PCS Synchronization process continually monitors PMA:IS_SIGNAL.indication(SIGNAL_OK). When SIGNAL_OK indicates OK, then the PCS synchronization process accepts the streams of symbols via the PMA:IS_UNITDATA_i.indication primitive.'.

Based on the signal indication logic (SIL) contained in the PMA sublayer described in subclause 155.3.2, and subclause 155.2.1 describing only the use of the SIGNAL_DETECT parameter in the PCS sublayer, it doesn't seem correct to say in subclause 156.5.4 that a valid signal is determined only by the PCS sublayer. And based on subclause 156.5.4 setting the SIGNAL_DETECT parameter of the PMD:IS_SIGNAL.indication to a fixed 'OK' value, it doesn't seem correct to say that the SIL will report signal health based on the PMD:IS_SIGNAL.indication primitive since it is fixed.

SuggestedRemedy

Suggest that:

[1] The PMD:IS_SIGNAL.indication primitive is disconnected from the SIL box in figure 155-10 and is shown as not used by the PMA sublayer.

[2] In subclause 155.3.2 the text ‘... reports signal health based on receipt of the PMD:IS_SIGNAL.indication from the 400GBASE-ZR PMD sublayer, data being processed successfully by the signal ...’ be changed to read ‘... reports signal health based on data being processed successfully by the signal ...’.

[3] In subclause 156.5.4 the text ‘The presence of a valid signal is determined only by the 400GBASE-ZR PCS (see 155.2.1).’ should be changed to read ‘The presence of a valid signal is determined only by the SIL function in the PMA (see 155.3.2).’.

Response
ACCEPT IN PRINCIPLE.
See response to comment #346.
While sub-frames 1 and 48 are annotated with 3 and 0 in P0, sub-frame 0 doesn't have this annotation. In addition, it isn't clear what the 3 to 0 signifies, perhaps that each DP-16QAM symbol has four components, but subclause 155.3.3.3 (page 54, line 29) says 'For each polarization, the stream of Gray mapped, interleaved symbols are assembled into a frame format suitable for transmission over...' which seems to imply a separate frame for each polarization.

Suggested Remedy
Either remove the 3 to 0 annotation for sub-frames 1 and 48 or add to sub-frames 0 and define the meaning.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Subclause 155.3.3.3 'Pilot sequence (PS)' says that 'The seed is reset at the start of every sub-frame ...'. Isn't it the generator that is reset at the start of every sub-frame using the seed value?

Suggested Remedy
Suggest that the text 'The seed is reset at the start of every sub-frame, so that the same ...' be changed to read 'The generator is initialized using the seed at the start of every sub-frame, so that the same ...'.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.
There is no specification of how the PRBS10 sequence is mapped to 16QAM symbols.
From review of Table 155-6 it appears that the generator in Figure 155-13 is used to produce 232 bits. The even bits are mapped to the in-phase component of the 16QAM symbol, odd bits mapped to the quadrature-phase component of the 16QAM symbol, with a 0 mapped to a '-3' and a 1 mapped to a '3'.

Suggested Remedy

Suggest that the second paragraph of subclause 155.3.3.3.3 be changed to read:

The seed is reset at the start of every sub-frame, so that the same 116 symbols, \([P_0, \ldots, P_{115}]\) are inserted into every sub-frame of the same polarization. For each polarization X and Y, the generator produces 232 bits PRBS\([231:0]\) that are mapped to 116 16QAM symbols, \([P_0, \ldots, P_{115}]\) where for \(i = 0 \) to 115,

- PSBR[2i] maps to the in-phase (I) component of the 16QAM symbol \([P_i]\) for the respective polarization
- PSBR[2i+1] maps to the quadrature-phase (Q) component of the 16QAM symbol \([P_i]\) for the respective polarization

and where,

- 0 maps to -3 for the respective 16QAM symbol component
- 1 maps to +3 for the respective 16QAM symbol component

The generator polynomial and seed values are listed in Table 155-6 and the complete PS sequence is shown in Table 155-6.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.

Since the abbreviation 'PS' is 'pilot sequence' the text '... PS sequence ...' expands to '... pilot sequence sequence ...'.

Suggested Remedy

Suggest the text '... the complete PS sequence is ...' be changed to read '... the complete PS is ...'.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.

There appear to be two separate tables number 155-6, the first labelled 'Table 155-5-PS generator polynomial and seed values', the second labelled 'Table 155-6-PS'.

Suggested Remedy

[1] Suggest that the second Table 155-6 'PS' be renumbered to be 155-7, with subsequent tables renumbered, and its title should be
[2] Suggest that the title of the second Table 155-6 should be changed from 'PS' to read 'Pilot sequence'.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.
Response #277

Cl 155 SC 155.3.3.4 P 58 L 30 # 277

Law, David Hewlett Packard Enterprise

Comment Type T Comment Status A rewrite bucket

The title of subclause 155.3.3.4 is '16QAM encode and signal drivers' however I don't think IEEE P802.3cw specifies a physical instantiation of the PMD service interface, and I don't see any text related to signal drivers in subclause 155.3.3.4. Perhaps it would be better to reference the DAC (see Figure 155-10) to parallel the title of subclause 155.3.3.5 below.

Suggested Remedy
Suggest that the title of subclause 155.3.3.4 is changed to read '16QAM encode and DAC'.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Response #280

Cl 155 SC 155.4.2.1 P 60 L 29 # 280

Law, David Hewlett Packard Enterprise

Comment Type T Comment Status A rewrite bucket

Assuming this is a boolean variable, suggest this should be noted in the variable description, as with other boolean variables.

Suggested Remedy
Suggest that 'A variable set by the ...' should read 'A boolean variable set by the ...'.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Response #281

Cl 155 SC 155.4.2.1 P 60 L 26 # 281

Law, David Hewlett Packard Enterprise

Comment Type T Comment Status A rewrite bucket

The description of the 'pma_enable_deskew' variable says 'A boolean variable that enables and disables the PMA deskew process.'. Is this correct as 'pma_enable_deskew' is an output of the Figure 155 15 'PMA deskew state diagram' that doesn't appear to be used anywhere else.

Suggested Remedy
Suggest the description of the 'pma_enable_deskew' variable should be changed to read 'A Boolean variable that set to true when deskew is enabled and set to false when deskew is disabled. Received symbols may be discarded whenever deskew is enabled.'.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.
Comment Type  T  Comment Status  A  rewrite bucket

The description of the 'reset' variable says that it is 'A boolean variable that controls the resetting of the PCS and PMA sublayers' and that 'it is true whenever a reset is necessary including when reset is initiated from the MDIO ... and when the MDIO has put the PCS and PMA sublayers into low-power mode.'.

The PMA and PCS are separate MMDs (see Table 45-1). The PMA/PMD reset bit is 1.0.15 and the low power bit is 1.0.11, both found in PMA/PMD control 1 register. The PCS reset bit is 3.0.15 and the low power bit is 3.0.11, both found in the PCS control 1 register. Since these registers are in separate MMDs, and since their state is not communicate across the PMA service interface, the PMA and PCS resets can operate independently.

Suggested Remedy

[1] Rename the 'reset' variable used in Figure 155-14 'Frame alignment word (FAW) lock state diagram' to be 'pma_reset'.

[2] Rename the 'reset' variable used in Figure 155-15 'PMA deskew state diagram' to be 'pma_reset'.

[3] Rename the 'reset' variable used in Figure 155-16 'Alignment marker lock state diagram' to be 'pcs_reset'.

[4] Rename the 'reset' variable defined in subclause 155.4.2.1 'Variables' to be 'pma_reset' and change the description to read 'A Boolean variable that controls the resetting of the PMA sublayer. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PMA sublayer into low-power mode.'.

[5] Add a definition of the 'pcs_reset' variable to subclause 155.4.2.1 'Variables' with the description 'A Boolean variable that controls the resetting of the PCS sublayer. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS sublayer into low-power mode.'.

Response  Response Status  C

ACCEPT IN PRINCIPLE.

See response to comment #346.
Subclause 155.4.2.1 'Variables' says 'The PMA:IS_SIGNAL.indication primitive is generated through a signal indication logic (SIL) that reports signal health based on ... symbols being sent to the PCS on all of the output lanes.' The SIGNAL_OK parameter of the PMA:IS_SIGNAL.indication primitive is, however, used to derive the signal_ok variable (page 60, line 45) which is used as an 'open arrow' entry condition to the 'LOCK_INIT' state of the Figure 155-14 Frame alignment word (FAW) lock state diagram.

As a result, it appears that if the SIGNAL_OK parameter is ever set to FAIL, setting 'signal_ok' to FALSE, the figure 155-14 Frame alignment word (FAW) lock state diagram will enter the 'LOCK_INIT' state. I assume this will mean that symbols will not be sent to the PCS since the PMA will not have FAW alignment. This in turn will mean the condition 'symbols being sent to the PCS' for the SIL to set the SIGNAL_OK parameter to OK will not be met.

The PMA will then be locked in this condition permanently. The SIL cannot set the SIGNAL_OK parameter to OK until symbols are sent to the PCS. Yet symbols won't be sent to the PCS until the SIGNAL_OK parameter is set to OK.

Suggested Remedy

Please clarify the operation of the signal indication logic. Suggest, based on Figure 155-10, and the dotted line from the 'Carrier phase recovery block to the SIL', that the 'signal_ok' variable used by the Frame alignment word (FAW) lock state diagram should be based on the status of the blocks below the 'Pilot removal' blocks while the SIGNAL_OK parameter sent to the PCS should also use the FAW alignment status.

See also my other comment suggest separate 'pma_signal_ok' and 'pcs_signal_ok' variables.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.

The description of the 'restart_lock' variable says 'A boolean variable that is set by the frame alignment word (FAW) lock process to reset the synchronization process on all PMA lanes. It is set to TRUE when 15 FAWs in a row fail to match (15_BAD state)'. While the restart_lock variable is used in the frame alignment word (FAW) lock process described in Figure 155-14, it is also used in the Alignment marker lock process described in Figure 155-16.

Suggested Remedy

[1] Rename all instances of the 'restart_lock' variable used in Figure 155-14 'Frame alignment word (FAW) lock state diagram' to be 'pma_restart_lock'.

[2] Rename all instances of the 'restart_lock' variable used in Figure 155-16 'Alignment marker lock state diagram' to be 'pcs_restart_lock'.

[3] Rename 'restart_lock' variable in subclause 155.4.2.1 'Variables' to be 'pma_restart_lock'.

[4] Add a definition of the 'pcs_restart_lock' variable to subclause 155.4.2.1 'Variables'.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.
The description of the 'faw_valid' variable says 'The FAW consists of one of the sequences listed in Table 155-3.' but then 'The sequence is considered to be valid if at least 36 bits match the 44 known bits of the FAW pattern described in 155.3.3.3.' The sequence listed in Table 155-3 and the candidate sequences received over the PMD service interface, are both 22 DP-16QAM symbols, not 44 bits. Based on slide 4 of the contribution 'faw_valid analysis' from Mike Sluyski referencing a 'QPSK FAW' value of 44 in the spreadsheet, I assume the reference to 36 bits matching the 44 known bits should be to 36 16QAM symbols matching the 44 16QAM symbols (which form the 22 DP-16QAM symbol FAW sequence), defined in Table 155-3.

Additionally, isn't it the case that the four components of the DP-16QAM symbols of the candidate 22 symbol block received over the four-lane PMD service interface can be mapped to the four lanes in any of eight ways defined in Table 155-7? If that is the case, suggest that this is also addressed in the description of the 'faw_valid' variable.

Suggested Remedy
Suggest that the 'faw_valid' variable description should be changed to read:

A Boolean variable that is set to true if the candidate 22 DP-16QAM symbol block received over the four-lane PMD service interface is a valid FAW sequence. The candidate 22 DP-16QAM symbol block is compared to the FAW sequence defined in Table 155-3, considering all permitted PMD service interface lanes mappings defined in Table 155-7. The candidate 22 DP-16QAM symbol block is considered to be a valid FAW sequence if at least 36 of its component 16QAM symbols match, in value, sequence position, and the 44 known 16QAM symbols of the FAW sequence defined in Table 155-3.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

The definition of the 'faw_valid' variable says '... set to true if the received 22-symbol block is a valid FAW.'. According to the super-frame format defined in subclause 155.3.3.3 the 22 FAW symbols are transmitted over a total of 23 symbols, as Pilot Sequence index P1 is inserted between the symbols faw<20> and faw<21> (see figure 155-12). As a result, a valid FAW will never be found in a received 22-symbol block, only in a received 23-symbol block after the 22nd symbol is deleted.

Suggested Remedy
If needed, clarify the definition of the 'faw_valid' variable to account for the P1 symbol inserted between the faw<20> and faw<21> symbols.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Subclause 155.3.3.3 'Insert FAW, TS and PS symbols' says that 'A super-frame is defined as .... including 175 616 payload symbols and 6272 additional symbols.' and that 'The first sub-frame of a super-frame includes ... a 22-symbol FAW (faw<20>) ... and 3488 payload symbols (m<0:3487>).'. Based on this it seems that the FAW is not considered part of the payload.

Suggested Remedy
Since the title of subclause 155.3.3.3.1 'Frame alignment word (FAW) sequence', suggest that the four instances of 'FAW payload ...' (page 61, lines 16, 18, 20 and 23) be changed to read 'FAW sequence ...'.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.
The description of the variable 'current_pmal' says 'The PMA lane number is determined by the FAW payloads based on the mapping defined in 155.3.3.3.1.' and the description of the variable 'pma_lane' says 'The PMA lane number is determined by matching the received 22-symbol sequence to the values in one of the columns of Table 155-3...'. Subclause 155.3.3.3.1, nor Table 155-3, provide any lane numbers. The PMA lane number is not referenced outside the state diagrams, other than in Table 155-9 where pma_lane_mapping<ξ> is mapped to register 3.400 through 3.403, which doesn't seem correct as these are PCS lane registers, not PMA lane registers (see my other comment on this). As a result, rather than add PMA lane numbers to subclause 155.3.3.3.1 and/or Table 155-3, suggest references to 'PMA lane numbers' be changed to 'PMA lane identifiers' with the values 'Ix', 'Qx', 'Iy' and 'Qy'. The state diagram can compare PMA lane identifiers to see if they match and can test for a unique PMA lane identifier for each PMA lane as easily as it can for PMA lane numbers.

In addition, the description of the 'faw_valid' variable says 'The sequence is considered to be valid if at least 36 bits match the 44 known bits of the FAW pattern described in 155.3.3.3.1.' The description of the variable 'current_pmal' however says 'The PMA lane number is determined by the FAW payloads based on the mapping defined in 155.3.3.3.1.' Similarly, the description of the variable 'pma_lane' says 'The PMA lane number is determined by matching the received 22-symbol sequence to the values in one of the columns of Table 155-3...'. Neither mention the '36 out 44' approach used for the 'faw_valid' variable.

The 'current_pmal' description could imply a requirement for a full match to a column of Table 155-3, and the 'pma_lane' description requires a full match to a column of Table 155-3. Since the entry into states where 'current_pmal' is used is based on faw_valid = TRUE, doesn't this mean that the use of the '36 out 44' approach, which permits 8 16QAM symbols to not match, needs to be considered when determining 'current_pmal' and 'pma_lane'. As a worst-case example, couldn't a faw_valid = TRUE result from eight 16QAM symbols not matching due to errors on just one phase of just one polarization. This would seem to imply that the compare for the values received on a lane with the columns of Table 155-3 also needs to permit eight values not matching.

In the case of 'current_pmal' and 'pma_lane', as there are only 22 values in a column of Table 155-3, it would seem a match would have to be valid if at least 14 values received on the lane match the 22 known values defined in a column to address the worst-case of all eight errors on one phase of one polarization. It seems there may, however, be another approach to determine 'current_pmal' and 'pma_lane'. Doesn't the PMD lane mapping row selected from Table 155-7 to achieve faw_valid = TRUE inherently provide the 'current_pmal' and 'pma_lane' values (see my comment on faw_valid)?

Finally, as this variable is used by a state diagram within the PMA, which sits above the PMD, the text "... is recognized on a given lane of the PMA service interface." should read ...
... is recognized on a given lane of the PMD service interface.".

SuggestedRemedy

[1] Change the description of the first_pmal variable to read as follows (note my other comment to change the coherent signal labels in Table 155-7 would impact this item if accepted):

A variable that holds the PMA lane identifier corresponding to the first FAW sequence that is recognized on a given lane of the PMD service interface. It is compared to the PMA lane identifier corresponding to the next FAW payload that is tested. The PMA lane identifier is the value for the given lane in the row of Table 155-7 that defines the PMD service interface lane mapping used to find the match for the current FAW sequence as described in the faw_valid variable.

Values:
Ix: Value for given lane from mapping used in Table 155-7 to find the current FAW sequence is XI.
Qx: Value for given lane from mapping used in Table 155-7 to find the current FAW sequence is XQ.
Iy: Value for given lane from mapping used in Table 155-7 to find the current FAW sequence is YI.
Qy: Value for given lane from mapping used in Table 155-7 to find the current FAW sequence is YQ.

[2] Change the description of the current_pmal variable to read as follows:

A variable that holds the PMA lane identifier corresponding to the current FAW sequence that is recognized on a given lane of the PMD service interface. It is compared to the variable first_pmal to confirm that the location of the FAW sequence has been detected. The PMA lane identifier is the value for the given lane in the row of Table 155-7 that defines the PMD service interface lane mapping used to find the match for the current FAW sequence as described in the faw_valid variable.

Values:
See first_pmal.

[3] Change the description of the pma_lane variable to read as follows:

pma_lane

A variable that holds the PMA lane identifier received on lane x of the PMA service interface when faws_lock<ξ> = TRUE. The PMA lane identifier is determined by matching the received 22-symbol FAW sequence to the values in one of the columns of Table 155-3. The PMA lane identifier is the value for the given lane in the row of Table 155-7 that defines the PMD service interface lane mapping used to find the match for the current FAW sequence as described in the faw_valid variable.

Values:
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<table>
<thead>
<tr>
<th>Comment ID</th>
<th>Type</th>
<th>Status</th>
<th>Comment Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>291</td>
<td>TR/technical required</td>
<td>W</td>
<td>E</td>
<td>There are nine instances of ‘super-frame’ and two instances of ‘DSP super-frame’. Suggest that one term is used consistently.</td>
</tr>
<tr>
<td>292</td>
<td>TR/technical required</td>
<td>W</td>
<td>TR</td>
<td>The description of the ‘FAW_COMPARE’ function in subclause 155.4.2.2 ‘Functions’ says that ‘If current_pmal and first_pmal both found a match and ... faw_match is set to true.’. Since faw_valid ‘... is considered to be valid if at least 36 bits match the 44 known bits of the FAW pattern ‘...’ I assume rather than a ‘match’, this really should say something along the lines of ‘If at least 36 symbols of the current receive 22-symbol block match the 44 known bits of the FAW pattern’.</td>
</tr>
</tbody>
</table>

Law, David
Hewlett Packard Enterprise

Comment ID 292
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10/20/2022 10:55:56 A
**IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments**

**Comment ID 293**  
Law, David  
Hewlett Packard Enterprise  
**Comment Type** E  
**Comment Status** A  
**Rewrite Bucket**  
**Subclause 155.4.2.3 'Counters' defines the 'cw_bad_count' counter, however this counter is not reference anywhere else in the draft.**  
**Suggested Remedy**  
Delete the 'cw_bad_count' counter definition.  
**Response**  
**Response Status** C  
ACCEPT IN PRINCIPLE.  
See response to comment #346.  

**Comment ID 294**  
Law, David  
Hewlett Packard Enterprise  
**Comment Type** E  
**Comment Status** A  
**Rewrite Bucket**  
**As the PMA is 'above' the PMD, the PMA would detect alignment in the symbols for a given lane of the PMD service interface.**  
**Suggested Remedy**  
Change the text ‘... the PMA service interface.’ to read ‘... the PMD service interface.’.  
**Response**  
**Response Status** C  
ACCEPT IN PRINCIPLE.  
See response to comment #346.  

**Comment ID 295**  
Law, David  
Hewlett Packard Enterprise  
**Comment Type** T  
**Comment Status** A  
**Rewrite Bucket**  
**Subclause 155.4.2.4 'State diagrams' says that 'The PCS shall implement the alignment marker lock process as shown in Figure 155-16 to identify the AM sequence at the start of each 4000BASE-ZR frame by observing data from the SC-FEC decoder output.' , however Figure 155-2 (page 55, line 20) shows the 'AM/OH detect & removal' block after the 'CRC32 check' block and subclause 155.2.5.7 'AM and OH detect and removal' says ‘... after removal of CRC32, MBAS, and pad, ...’**  
**Suggested Remedy**  
Suggest that the text ‘... by observing data from the SC-FEC decoder output.’ be changed to read ‘... by observing data from the CRC32 check and error marking output.’.  
**Response**  
**Response Status** C  
ACCEPT IN PRINCIPLE.  
See response to comment #346.

**Comment ID 296**  
Law, David  
Hewlett Packard Enterprise  
**Comment Type** TR  
**Comment Status** A  
**Rewrite Bucket**  
**Based on the description of the 'faw_valid' variable, and slide 4 of the contribution 'faw_valid analysis' from Mike Sluyski <https://www.ieee802.org/3/cw/public/22_0523/sluyski_3cw_01a_220523.pdf#page=4> referencing a 'QPSK FAW' value of 44, it seems a valid FAW sequence can only be detected across all four lanes. As a result, it will only be possible to achieve FAW lock on all lanes, or no lanes. There is no case where some lanes can be FAW locked, and others are not. There, therefore, seems no need to have four instances of the Frame alignment word lock state diagram (page 63, line 3). If there were, they wouldn’t operate independently on each lane (page 63, line 5), and instead would operate in lock step.**  
**Suggested Remedy**  
[1] Delete the variables 'pma_alignment_valid', 'all_locked', and PMA_lane_mapping from subclause 155.4.2.1 'Variables' and Figure 155-14.  
[2] Change the description of the 'faws_lock' variable (page 61, line 1) to read:  
faws_lock  
A Boolean variable that is set to true when the receiver has detected the location of the FAW.  
[3] Change the description of the faw_valid as suggested in my comment about faw_valid.  
[4] Change the description of the first_pmal to read (this overrides my other comment about first_pmal):  
A variable that holds the PMA lane mapping number found in the first column of Table 155-7 corresponding to the first FAW sequence. It is compared to the PMA lane mapping number corresponding to the next FAW payload that is found.  
[5] Change the description of the current_pmal to read (this overrides my other comment about current_pmal):  
A variable that holds the PMA lane mapping number found in the first column of Table 155-7 corresponding to the PMA service interface lane mapping used to find the match for the current FAW sequence. It is compared to the variable first_pmal to confirm that the location of the FAW sequence has been detected.  
[6] Change all instances of '... PMA lane number ' to '... PMA lane mapping number ...'.
[7] Change the text ‘... of the next FAW on a PMA lane.’ to read ‘... of the next FAW.’ in the 'faw_counter' description.

[8] Change the first paragraph of subclause 155.4.2.4 ‘State diagrams’ to read ‘The PMA shall also implement the deskew process as shown in Figure 155-14.

[9] Delete the second paragraph of subclause 155.4.2.4.

[10] Add the assignment 'pma_align_status <= FALSE' to the 'LOCK_INIT' state of Figure 155-14.

[11] Add the assignment 'pma_align_status <= TRUE' to the '2_GOOD' state of Figure 155-14.

[12] Delete Figure 155-15.

[13] Change the 'Value/Comment' field of PICS item SM1 in subclause 155.7.4.4 'State diagrams' to read 'Meets the requirements of Figure 155-14.'

[14] Delete the SM2 row from subclause 155.7.4.4 and renumber following items.

Response

[15] The 'slip_done' variable assigned to FALSE in the GET_BLOCK state of the Frame alignment word (FAW) lock state diagram is not defined. Suspect it should read 'faw_slip_done' so that it is set to FALSE before the FAW_SLIP function, which sets it TRUE, is called in the FAW_SLIP state.

SuggestedRemedy

Change the text 'slip_done <= FALSE' in the GET_BLOCK state in Figure 155-14 to read 'faw_slip_done <= FALSE'.

ACCEPT IN PRINCIPLE.

See response to comment #346.

[16] There is no definition of the 'prev_pmal' variable used in the 'INVALID_FAW' state of figure 155-14 Frame alignment word (FAW) lock state diagram, and there is no use or reference to the 'prev_pmal' variable elsewhere in the IEEE P802.3cw draft.

SuggestedRemedy

Delete the assignment ' prev_pmal <= prev_pmal + 4) mod 252' from the 'INVALID_FAW' state.

ACCEPT IN PRINCIPLE.

See response to comment #346.

[17] The description of the 'first_pmal' variable says it ‘... the PMA lane number that corresponds to the first FAW payload ...’ however, it is updated by the assignment 'first_pmal <= current_pmal' every cycle through the '2_GOOD' and 'GOOD_FAW' states. With that said, the assignment 'first_pmal <= current_pmal' in the '2_GOOD' and 'GOOD_FAW' states appear to be redundant since the only way to enter these states is if 'faw_match' is TRUE and for 'faw_match' to be TRUE the first_pmal and current_pmal variables have to be equal (see FAWCOMPARE function, page 62, line 29).

SuggestedRemedy

Consider removing the assignment 'first_pmal <= current_pmal' from the '2_GOOD' and 'GOOD_FAW' states.

ACCEPT IN PRINCIPLE.

See response to comment #346.
### Comment #300

**Comment Type**: Technical (T)<br>
**Comment Status**: Accepted (A)<br>
**Comment**: Subclause 155.4.2.3 'Counters' defines the 'faws_bad_count' whereas the Figure 155-14 'Frame alignment word (FAW) lock state diagram' uses 'faw_bad_count' ('faw' vs 'faws').<br>
**Suggested Remedy**: Suggest that:<br>
1. The transition from the 'INVALID_FAW' state to the '15_BAD' state be changed to read 'faws_bad_count = 15'.<br>
2. The transition from the 'INVALID_FAW' state to the 'COUNT_2' state be changed to read 'faws_bad_count < 15'.

**Response Status**: Accepted in Principle (C)<br>
See response to comment #346.

### Comment #301

**Comment Type**: Editorial (E)<br>
**Comment Status**: Accepted (A)<br>
**Comment**: The 'restart_lock' variable is set to TRUE on entry to the '15_BAD' state. This will cause the state diagram to transition to the 'LOCK_INIT' state because 'restart_lock' is one of the OR conditions in the 'open arrow' entry to that state. The actions in the 'LOCK_INIT' state will be executed, but since 'restart_lock' remains set to TRUE, and 'open arrow' transitions are evaluated continuously whenever any state is evaluating its exit conditions (see 21.5.3), on exit the state diagram will loop back to the 'LOCK_INIT' state. The state diagram will then be locked in this loop permanently.<br>
**Suggested Remedy**: Suggest that either the action 'restart_lock <= FALSE' be added to the 'LOCK_INIT' state or the 'restart_lock' be deleted and a 'UCT' be added from the '15_BAD' state to the 'LOCK_INIT' state.<br>
**Response Status**: Accepted in Principle (C)<br>
See response to comment #346.

### Comment #303

**Comment Type**: Editorial (E)<br>
**Comment Status**: Accepted (A)<br>
**Comment**: The variable 'PMA_lane_mapping' in the 2_GOOD state of the Frame alignment word (FAW) lock state diagram should read 'pma_lane_mapping' based on the definition in subclause 155.4.2.1 (page 61, line 34).<br>
**Suggested Remedy**: Change the text 'PMA_lane_mapping<x> <= current_pmal' in the 2_GOOD state in Figure 155-14 to read 'pma_lane_mapping<x> <= current_pmal'.

**Response Status**: Accepted in Principle (C)<br>
See response to comment #346.

### Comment #304

**Comment Type**: Editorial (E)<br>
**Comment Status**: Accepted (A)<br>
**Comment**: Since the title of Figure 155-15 is 'PMA deskew state diagram' suggest that PMA should be added to the title of Figure 155-14 and PCS to the title of Figure 155-16.<br>
**Suggested Remedy**: Suggest that:<br>
1. The title of Figure 155-14 should be changed to read 'PMA Frame alignment word (FAW) lock state diagram'.<br>
2. The title of Figure 155-16 should be changed to read 'PCS Alignment marker lock state diagram'.

**Response Status**: Accepted in Principle (C)<br>
See response to comment #346.
There are two instances of `amps_lock` and one of `amps_lock<x>` in figure 155-16 Alignment marker lock state diagram. Since subclause 155.2.4.3 'GMP mapper' says '... 400GBASE-ZR frames are not mapped to 16 PCS lanes ...', and since subclause 155.4.2.1 'Variables' defines `amps_lock` without an index, it seems that `amps_lock<x>` should read 'amps_lock'.

**Suggested Remedy**

Change 'amps_lock<x> <= FALSE' in the LOCK_INIT state to read 'amps_lock <= FALSE'.

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.

The figure 155-16 PCS alignment marker lock state diagram uses the variable 'pma_align_status', however that variable is generated by the figure 155-14 PMA frame alignment word (FAW) lock state diagram, and it is not passed across the PMA service interface from the PMA to the PCS. As a result, it is not available to be used in the figure 155-16 PCS alignment marker lock state diagram.

Suggest that 'pma_align_status' being 'TRUE' be used as a condition to set the SIGNAL_OK parameter of the PMA:IS_SIGNAL.indication primitive to OK and therefore communicate it across the PMA service interface. Since 'signal_ok', derived from the SIGNAL_OK parameter, is already used as an 'open arrow' entry to the 'LOCK_INIT' state of the figure 155-16 PCS alignment marker lock state diagram, 'pma_align_status' can be deleted as an exit condition from that state.

**Suggested Remedy**

[1] Add 'pma_align_status' being 'TRUE' as a condition to set the SIGNAL_OK parameter of the PMA:IS_SIGNAL.indication primitive to OK in subclause 155.3.2 '400GBASE-ZR PMA service interface'

[2] Delete that exit condition 'pma_align_status' from the LOCK_INIT state in figure 155-16.

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.
Strictly speaking, protocol agnostic management 'objects' are defined in Clause 30, with protocol specific 'objects' defined in IEEE Std 802.3.1 and IEEE Std 802.3.2.

SuggestedRemedy
Since the title of subclause 45.2 in IEEE Std 802.3-2022 is 'MDIO Interface registers', suggest that the text 'The following objects apply ...' in subclause 155.5 be changed to read 'The following registers apply ...'.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Law, David
Hewlett Packard Enterprise

Register bits 3.52.3:0 (IEEE Std 802.3-2022 subclause 45.2.3.25) are PCS lane alignment lock status registers, yet they are mapped to PMA lane alignment lock variables (pma_align_status). Similarly, register bit 3.50.12 is the PCS alignment status register, yet it is mapped to the PMA alignment status variable (pma_align_status).

If there was a 400GBASE-ZR framing issue on a link where the PMA framing was operating correctly, the faw_lock<3:0> bits and the pma_align_status would all be true based on the respective frame alignment word (FAW) lock state diagrams, while the PCS would not be aligned based on the alignment marker lock state diagram. In that case, the current register mapping would indicate that all the PCS lanes were aligned, and the overall PCS was aligned, when in fact this is not the case. This would seem to be misleading information to provide in the management registers in such a case.

Further, register 3.400 (IEEE Std 802.3-2022 subclause 45.2.3.49) through 3.419 are the 'PCS lane mapping registers, lanes 0 through 19' and these registers report the PCS lane number provide by the alignment marker for the respective PMA service interface lane. Table 155-9, however, maps these PCS lane mapping registers to the PAM lane mapping variable 'pma_lane_mapping<xx>' output by Figure 155-14, the 'Frame alignment word (FAW) lock state diagram'.

Subclause 155.2.4.3 'GMP mapper' says 'The first 1920 bits of the frame contain alignment markers (AM), and that these are identical to the 16 x 120b markers defined for 400GBASE-R in 119.2.4.4.2,'. Since the 16 different 400GBASE-R PCS lane alignment markers are all placed in a single 400GBASE-ZR alignment marker (see 155.2.4.4.1) it seems that 400GBASE-ZR frames are not mapped to 16 PCS lanes. This seems to be confirmed in subclause 155.2.4.3 'GMP mapper' which says '...400GBASE-ZR frames are not mapped to 16 PCS lanes ...'. As a result, there are no PCS lanes across the PMA service interface, therefore there is no PCS lane alignment lock status nor PCS Lane mapping.

Finally, register bits 3.52.3:0, 3.50.12, and 3.400 through 3.403, which are all PCS register bits defined for MMD 3 (see IEEE Std 802.3-2022 Table 45-1), are mapped to variables found in the PMA. As illustrated in Figure 120A-9 (page 103), MMD 3 does not have access to the PMA (or PMD) as they are in MMD 1.

Based on the above, suggest that two new subclauses are added to say that registers 3.52, 3.53 and 3.400 through 3.403 are not used by the 400GBASE-ZR PCS because the 400GBASE-ZR PCS does not use PCS lanes across the PMA service interface. Require all PCS lane alignment bits to be set to zero. The content of the PCS lane mapping registers does not need to be defined because their content is only valid when the respective PCS lane alignment bit is set to one. In addition, suggest that the PCS lane alignment status bit be mapped from the 'amps_lock' variable generated by the Figure 155-16, the PCS alignment marker lock state diagram.

SuggestedRemedy

See response to comment #346.

Law, David
Hewlett Packard Enterprise
Suggested changes:

[1] Delete the antepenultimate row of Table 155-9.

[2] Add a new subclause 155.5.1 as follows:

155.5.1 PCS lane alignment registers

The PCS lane alignment registers (registers 3.52 and 3.53) are not used as the 400GBASE-ZR PCS does not use PCS lanes across the PMA service interface (see 155.2.4.3). A 400GBASE-ZR PCS shall return a zero for all bits in these registers.

[3] Change the variable 'pma_align_status' in the 'ZR-PCS/PMA variable' column of the penultimate row of Table 155-9 to 'amps_lock'.


[5] Add a new subclause 155.5.2 as follows:

155.5.2 PCS lane mapping registers

The PCS lane mapping registers (registers 3.400 through 3.419) are not used as the 400GBASE-ZR PCS does not use PCS lanes across the PMA service interface.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment Type: TR/technical required
Comment Status: A
SuggestedRemedy

[1] Suggest that in subclause 156.2 (page 75, line 14) the text ‘... X and Y polarizations with binary values of 3, 1, -1, and -3 using the ...’ should be changed to read ‘... X and Y polarizations with the values of 3, 1, -1, and -3 using the ...’.

[2] Suggest that in subclause 156.5.2 (page 77, line 39) the text ‘... X and Y polarizations with binary values of 3, 1, -1, and -3.’ should be changed to read ‘... X and Y polarizations with the values of 3, 1, -1, and -3.’.

Response

ACCEPT IN PRINCIPLE.

See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

### Comment #317

**Comment Type:** TR  
**Comment Status:** A

**Law, David**  
**Hewlett Packard Enterprise**

**Subclause 156.3.2 'Skew constraints'** says that 'The Skew (relative delay) between the lanes is kept within limits so that the information on the FEC lanes can be reassembled by the FEC.' On review of Clause 155, 400GBASE-ZR doesn't seem to mention FEC lanes anywhere else. Further, subclause 155.2.4.3 'GMP mapper' says '... 400GBASE-ZR frames are not mapped to 16 PCS lanes ...'. As far as I can see, the 8-bit PMA service interface carries an 8-bit word that describes an DP-16QAM symbols based on the mapping defined in Table 155-2. As a result, the only lanes seem to be the PMD service interface which has four lanes which carry four analogue streams representing the in-phase and quadrature-phase component of the two polarizations (page 75, line 13).

Table 156-6 specifies a maximum polarization skew of 5 ps (page 82, line 45) and a maximum quadrature skew is 0.75 ps (page 83, line 6). Subclause 156.3.2, however, says The Skew at SP3 (the transmitter MDI) shall be less than 54 ns and the Skew Variation at SP3 is limited to 600 ps. I suspect that the former values are correct. And based on this, assuming no retiming in the PMD, the other values in subclause 156.3.2 don't seem correct either.

**Suggested Remedy**

Since 400GBASE-ZR doesn't seem to support FEC lanes, and says it doesn't support PCS lanes, suggest that subclause 156.3.2 is deleted.

**Response**

**Response Status:** W

ACCEPT IN PRINCIPLE.

See response to comment #346.

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### Comment #321

**Comment Type:** E  
**Comment Status:** A

**Law, David**  
**Hewlett Packard Enterprise**

Rather than being requested by the PMD service interface messages, messages are passed across the PMD service interface, either from the PMA to the PMD or from the PMD to the PMA. In addition, abstract service interfaces pass data in the parameters of primitives. In the case of the inter-sublayer service interface primitives defined in subclause 116.3 referenced by IEEE P802.3cw, these parameters are tx_symbol (see 116.3.3.1.1) and rx_symbol (see 116.3.3.2.1).

**Suggested Remedy**

Suggest:

[1] The text 'The PMD Transmit function shall convert the four analog streams requested by the PMD service interface messages PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request into ...' (page 77, line 35) should be changed to read 'The PMD Transmit function shall convert the four analog streams from the PMA passed across the PMD service interface in the tx_symbol parameters of the PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request primitives into ...'.

[2] The text 'The PMD Receive function shall convert the composite optical signal received from the MDI into four analog streams for delivery to the PMD service interface using the messages PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication, all according ...' (page 77, line 45) should be changed to read 'The PMD Receive function shall convert the composite optical signal received from the MDI into four analog streams passed across the PMD service interface to the PMA in the rx_symbol parameters of the PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication primitives, all according ...'.

[3] The text 'The analog signals are sent to the 400GBASE-ZR PMD sublayer over the PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request sublayer signals.' in subclause 155.3.3.4 (page 58, line 33) is changed to read 'The four analog signals are passed across the PMD service interface to the PMD in the tx_symbol parameters of the PMD:IS_UNITDATA_0.request to PMD:IS_UNITDATA_3.request primitives.'.

[4] The text 'Four coherent signals IX, QX, IY, and QY are supplied by the receive function of the 400GBASE-ZR PMD and input to the 400GBASE-ZR PMA over the PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication.' in subclause 155.3.3.5 (page 58, line 47) is changed to read 'Four coherent signals IX, QX, IY, and QY received by the PMD are passed across the PMD service interface to the PMA in the rx_symbol parameters of the PMD:IS_UNITDATA_0.indication to PMD:IS_UNITDATA_3.indication primitives.'

**Response**

**Response Status:** C

ACCEPT IN PRINCIPLE.

See response to comment #346.
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Cl 155 SC 155.1.5 P 55 L 3 # 338
Zimmerman, George CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type E Comment Status A rewrite bucket
The sentence says 400GBASE-Z PCS sublayer, but the figure is labeled and used as the 400GBASE-ZR PCS sublayer (also the "R" generally is used to refer to the BASE-R encoding used here.)

SuggestedRemedy
change 155.1.5, page 34 line 3, to "400GBASE-ZR PCS sublayer" to agree with the figure
Response ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 155 SC 155.3.3.5 P 58 L 45 # 341
Zimmerman, George CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type TR Comment Status A rewrite bucket
"The signals are sampled by an ADC on each lane at a sampling rate." "The details of the ADC are implementation specific". This is a description of an implementation, not appropriate for an interoperability specification. If someone could do the signal processing optically, analog, or by magic, it would still comply with the standard. The fact that an ADC is used, isn't a part of the interoperability standard, or even any of the characteristics of the ADC. Hence the mention is inappropriate and should be deleted. The sentence works just fine anyways and describes the processing without the "by an ADC".

SuggestedRemedy
Change header of 155.3.5 to Receive signal sampling.
On line 50, Delete "by an ADC"
Change line 54 to "The details of the sampling, including any quantization and the chosen sampling rate are implementation specific."
Replace "ADC" with "Sampler" in figure 155-10.
Response ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 155 SC 155.3.3.1 P 52 L 28 # 542
Zimmerman, George CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type TR Comment Status A rewrite bucket
"The received symbol signals are digitized into more than 4 discrete levels by the analog to digital converters (ADC) in the PMA sublayer and the number of bits for each signal is m/4 bits." This is a description of an implementation and is inappropriate for an interoperability standard. If some description is needed, one could rewrite this more generally, as is suggested in the remedy. Further, it appears that the "m/4 bits" is a detail that is unused in the draft (I searched). If it is used somewhere, please provide a pointer to where it is relevant. Otherwise delete the unnecessary detail which looks like a specification but isn't.

SuggestedRemedy
Preferably - delete the indicated sentence. Alternatively, change the indicated sentence to read "The received symbol signals are sampled and quantized in the PMA sublayer."
If the m/4 bits is used somewhere, provide a reference.
Response ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 155 SC 155.3.3.5 P 58 L 45 # 343
Zimmerman, George CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type TR Comment Status A rewrite bucket
"The signals are sampled by an ADC on each lane at a sampling rate." "The details of the ADC are implementation specific". This is a description of an implementation, not appropriate for an interoperability specification. If someone could do the signal processing optically, analog, or by magic, it would still comply with the standard. The fact that an ADC is used, isn't a part of the interoperability standard, or even any of the characteristics of the ADC. Hence the mention is inappropriate and should be deleted. The sentence works just fine anyways and describes the processing without the "by an ADC".

SuggestedRemedy
Change header of 155.3.5 to Receive signal sampling.
On line 50, Delete "by an ADC"
Change line 54 to "The details of the sampling, including any quantization and the chosen sampling rate are implementation specific."
Replace "ADC" with "Sampler" in figure 155-10.
Response ACCEPT IN PRINCIPLE.
See response to comment #346.
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<th>Cl 155</th>
<th>SC 155.3.1.3</th>
<th>P 49</th>
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**Figure 155-10 is separated from the text which describes it, by the intervening description of the service interface.**

**Suggested Remedy**

Beat on frame, and move the figure 155-10 be after 155.3.1.3 and before 155.3.2 (one way to do this may be forcing a page break before 155.3.2)

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.

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This figure is supposed to be a functional block diagram, not an implementation diagram. There are no characteristics for the DAC blocks defined in the specification. The closest thing in the text is 155.3.3.4 which are called the 16QAM encode and signal drivers. However, most other 802.3 PHY clauses leave out signal drivers, DACs and the like, and there are no specific requirements in 155.3.3.4, so deleting the blocks seems the right approach to making a functional block diagram.

**Suggested Remedy**

Preferably, delete the "DAC" blocks from Figure 155-10 (going straight to the output is fine) Alternatively, Relabel "16QAM Encoder and Signal Driver" (probably drawing as 2 blocks since you show I&Q paths)

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.

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This is a general comment on the requirements. I am attaching it to these PICS because this is where it became apparent. The style of IEEE SA standards (and IEEE Std 802.3) is that requirements use the term "shall". Each PICS item should have an associated "shall" and each "shall" should have a PICS. However, 155.7.4.1 is a list of the subclauses for the most part. Further, looking at the subclauses, they are largely without "shall". Most of the items in clause 155 are descriptive of an implementation, and do not use the term shall. They use "is" or other descriptive language. The PICS are a list of the functional blocks described, but most of those functional blocks are lacking actual requirements. Instead they often describe an implementation or, worse yet, sometimes try to require a particular implementation ("an implementation shall"). What needs to happen is that the clause needs to be rewritten carefully considering what requirements are needed for interoperability, and deleting the unnecessary implementation description. This is a big job, and, in my opinion, means the draft is not technically complete, and should not have begun initial working group ballot. I truly regret having to make a comment like this, but I believe this is a great example of why we have working group ballots in 802.

**Suggested Remedy**

Unfortunately, the draft is so far from complete that I cannot propose a specific remedy for the systematic problem. I can suggest that the TF look at each subblock, determine what the observed behavior is, determine which parts matter to interoperability, and write "shall" statements in the subclauses. Then those shall statements can be made as PICS. Additionally, this will highlight where there is implementation description that can be deleted. When this is done, restart working group ballot.

**Response**

ACCEPT IN PRINCIPLE.

With editorial license, restructure and clarify Clause 155 and 156 as appropriate:
- to identify interoperability requirements using "SHALL" statements, as needed.
- to address issues noted in https://www.ieee802.org/3/cw/public/22_10/dambrosia_3cw_01b_221018.pdf

**Response**

ACCEPT IN PRINCIPLE.

With editorial license, restructure and clarify Clause 155 and 156 as appropriate:
- to identify interoperability requirements using "SHALL" statements, as needed.
- to address issues noted in https://www.ieee802.org/3/cw/public/22_10/dambrosia_3cw_01b_221018.pdf

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<table>
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<th>Cl 155</th>
<th>SC 155.2.4.5.4</th>
<th>P 40</th>
<th>L 30</th>
<th># 348</th>
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<td>Maniloff, Eric</td>
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<td><strong>rewrite bucket</strong></td>
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**Suggested Remedy**

Add a figure showing the interleaved OH mapping

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.
<table>
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<tr>
<td>155</td>
<td>155.4.2.1</td>
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<td>A bad CW can be detected either by detecting errors after FEC decoding or by CRC errors. This should be clarified in the counter definition.</td>
<td>Add the following to the definition of cw_bad: An uncorrected codeword is detected if either errors remain after FEC correction or if the CRC32 check fails.</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
<td>A</td>
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<td>155</td>
<td>155.2.5.3</td>
<td>E</td>
<td>A</td>
<td>You should refer to the equation.</td>
<td>Change: polynomial given in 155.2.4.9. To: polynomial given by Equation (155-1).</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
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<tr>
<td>155</td>
<td>155.3.2</td>
<td>E</td>
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<td>It's hard to see the text with the line through it.</td>
<td>Add a box around &quot;400GBASE-ZR PMA sublayer&quot; so the line is &quot;behind&quot; it.</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
<td>A</td>
<td></td>
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<tr>
<td>155</td>
<td>155.2.4.4.1</td>
<td>TR</td>
<td>A</td>
<td>The name of the section include 400GBASE-ZR, why? Cl119 uses &quot;for 200GBASE-R&quot; and &quot;for 400GBASE-R&quot; since it has two different methods done for the different rates. But this is only 1 rate clause and Clause 91 and 135 don't attach the rate to it's section heading</td>
<td>Remove &quot;400GBASE-ZR&quot; from the section title of 155.2.4.4.1 and 155.2.4.4.2</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>C</td>
<td>A</td>
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<td>155</td>
<td>155.2.4.7</td>
<td>TR</td>
<td>A</td>
<td>Figure 155-6 does not show the 6x119b pad</td>
<td>Add box at the end of the i+119 row to the right of the CRC+MBAS labeled 6x119b PAD</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>W</td>
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<tr>
<td>155</td>
<td>155.2.4.5.2</td>
<td>TR</td>
<td>A</td>
<td>Per Figure 155-4 the RPF field is in bit location 0 of the Status Octect. But the Text states it's bit location 1.</td>
<td>Change &quot;in bit 1&quot; to &quot;the first bit&quot;</td>
<td>ACCEPT IN PRINCIPLE.</td>
<td>W</td>
<td>W</td>
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</tbody>
</table>

**Comment ID:** 389 | **Page:** 57 of 71 | **Date:** 10/20/2022 10:55:56 A
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

Slavick, Jeff  
Broadcom  

Comment Type TR  Comment Status A  rewrite bucket

Comment: What is the contents of the PAD?

SuggestedRemedy
Change "pad bits added" to "pad bits of all zeroes added"

Response  Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.

Slavick, Jeff  
Broadcom  

Comment Type TR  Comment Status A  rewrite bucket

Comment: We traditionally refer to the 257b blocks as 257-bit blocks not 257B blocks (which could be inferred as 257 Byte)

SuggestedRemedy
Change the seven instances of 257B block to 257-bit block

Response  Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.

Slavick, Jeff  
Broadcom  

Comment Type TR  Comment Status A  rewrite bucket

Comment: I could not find a Clause 9.4.3.2 in ITU-T G.709 but I did find a 19.4.3.2 that talks about GMP

SuggestedRemedy
Change 9.4.3.2 to 19.4.3.2

Response  Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.

Slavick, Jeff  
Broadcom  

Comment Type TR  Comment Status A  rewrite bucket

Comment: Figure 155-9 is identical to 155-4 and is not referenced

SuggestedRemedy
Delete Figure 155-9. Add "(see Figure 155-4)" to the end of last paragraph

Response  Response Status W
ACCEPT IN PRINCIPLE.

See response to comment #346.
The OH section of the 400GBASE-ZR frame is 1280 bits in size. This intro sentence states that OH is only a 40-byte is only 320 bits of data.

**Suggested Remedy**

Remove 155.2.4.5.4 and update 155.2.4.5 as follows (retaining Figure 155-4):

155.2.4.5 Overhead (OH)

The 400GBASE-ZR frame contains a 1280-bit OH field. This field is logically composed of four 320-bit structures. The 40-byte overhead frame described in 155.2.4.5.1 is the first such 320-bit structure. The second, third, and fourth 320-bit structures are all zeros. The four 320-bit structures are 10-bit interleaved to form the 1280-bit overhead field.

155.2.4.5.1 40-byte overhead frame

The 40-byte overhead frame is a 40-byte frame structure that uses a four-frame multi-frame, as shown in Figure 155-4 and described in 155.2.4.5.1 through 155.2.4.5.1.3. The contents of the 40-byte overhead frame is dependent upon the two LSB bits of the MFAS (see 155.2.4.5.1.1) 155.2.4.5.1.1 Multi-frame alignment signal (MFAS)

The MFAS is in the first byte of the 40-byte overhead frame. It is a wrapping counter that is incremented each frame to provide a 256-frame multi-frame sequence as defined by ITU-T G.709.1 Clause 9.2.1.

Renumber 155.2.4.5.2 and 155.2.4.5.3 to 155.2.4.5.1.2 and 155.2.4.5.1.3 keeping the text unchanged for those sections.

**Response**

ACCEPT IN PRINCIPLE.

See response to comment #346.
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<td>47</td>
<td>53</td>
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<td>Uncorrectable blocks are not tracked in MDIO registers</td>
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<td>Add references to the MDIO register for counting corrected and uncorrected FEC CW and bits</td>
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<td>Reference is to 155.4 which is all the FSM blocks, call out the specific AM lock one.</td>
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<td>Change 155.4 to Figure 155-16</td>
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<td>60</td>
<td>51</td>
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<td>T</td>
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<td>Definition of restart_lock begins by talking about how it affects all lanes, then states it activates when 15 FAWs fail to match, but doesn't clearly define that's 15 failures in a row on a single PMA lane.</td>
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<td>Change &quot;fail to match&quot; to &quot;fail to match on a given PMA lane&quot;</td>
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<td>The MDIO references for corrected and uncorrected codeword counters only point to the Clause 45 register, which then points you back to Clause 153 for the definition of the counter. In Clause 153 it refers to &quot;fec_align_status&quot; which does not exist in Clause 155.</td>
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<td>Add sub-clauses for corrected and uncorrected codeword counters:</td>
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<td>155.5.1.x FEC_corrected_cw_counter</td>
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<td>A corrected FEC codeword is a codeword that contained errors and was corrected.</td>
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<td>The FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected FEC codeword processed when pma_alignment_valid is TRUE. This variable is mapped to the registers defined in 45.2.1.227 (1.2276, 1.2277).</td>
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<td>153.5.1.y FEC_uncorrected_cw_counter</td>
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<td>An uncorrected FEC codeword is a codeword that contains errors that were not corrected, including FEC codewords that may have been mis-corrected or not completely corrected.</td>
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<td>The FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected FEC codeword processed when pma_alignment_valid is TRUE. This variable is mapped to the registers defined in 45.2.1.228 (1.2278, 1.2279).</td>
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<td>Bring in 45.2.1.227 and 45.2.1.228 and references to the newly added sub-clauses in Clause 155.</td>
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</table>

**Slavick, Jeff**

**Comment Type**: TR

**Comment Status**: rewrite bucket

The corrected bit and total bit MDIO registers refer to Clause 153 only but are being used in Clause 155 now.

**Suggested Remedy**

Add the following sub-clauses:

- 155.5.1.x FEC_total_bits_counter

See 153.2.5.3 for the definition of this counter.

- 155.5.1.y FEC_corrected_bits_counter

See 153.2.5.4 for the definition of this counter.

Bring in 45.2.1.229 and 45.2.1.230 and add appropriate references to these new sub-clauses

**Response**

**Response Status**: W

ACCEPT IN PRINCIPLE.

See response to comment #346.

<table>
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</table>

**Slavick, Jeff**

**Comment Type**: TR

**Comment Status**: rewrite bucket

The last paragraph states that the link degrade function is provided and that the bit error ratio is used to indicate this. But in the MDIO mapping (Table 155-8) points to fields that exist but reference 119.2.5.3 which specifies the thresholds in terms of rs-symbol error rates and FEC codewords.

**Suggested Remedy**

Replace the last paragraph of 155.2.5.5 with the following:

The 4000GBASE-ZR PCS may optionally provide the ability to signal degradation of the received signal. The presence of this option is indicated by the assertion of the FEC_degraded_SER_ability_variable (see 155.4.2.1). When the option is provided it is enabled by the assertion of the FEC_degraded_SER_enable variable (see 155.4.2.1).

When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the PCS. The PCS counts the number of bits corrected by the SC-FEC decoder in consecutive nonoverlapping SC-FEC frames of FEC_degraded_SER_interval (see 155.4.2.1). If the SC-FEC decoder determines that a codeword is uncorrectable or errors are detected by the CRC32 check (see 155.2.5.6), the number of symbol errors detected is increased by 957 x 257. When the number of bit errors exceeds the threshold set in FEC_degraded_SER_activate_threshold (see 155.5.1), the FEC_degraded_SER bit (see 155.5.1) is set. At the end of each interval, if the number of symbol errors is less than FEC_degraded_SER_deactivate_threshold, the FEC_degraded_SER bit is cleared. If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is de-asserted then the FEC_degraded_SER bit is cleared.

Bring in 45.2.3.60.1 and add "155.2.5.5" to the see list
Bring in 45.2.3.61.1 and add "155.4.2.1" to the see list
Bring in 45.2.3.61.3 and add "155.2.5.5" to the see list
Bring in 45.2.3.61.4 and add "155.4.2.1" to the see list

**Response**

**Response Status**: W

ACCEPT IN PRINCIPLE.

See response to comment #346.
Cl 155 SC 155.4.2.1 P 68 L 26 # 409
Slavick, Jeff Broadcom
Comment Type TR Comment Status A rewrite bucket
FEC high SER is not a feature of 400GBASE-ZR
SuggestedRemedy
Remove the FEC high SER row from Table 155-9
Response Response Status W
ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 155 SC 155.1.4 P 34 L 2 # 424
Dawe, Piers Nvidia
Comment Type E Comment Status A rewrite bucket
8 x 59.84375 x (28/29) ...
SuggestedRemedy
use multiplication sign as elsewhere
Response Response Status C
ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 155 SC 155.1.4 P 34 L 2 # 425
Dawe, Piers Nvidia
Comment Type E Comment Status A rewrite bucket
Giving an encoded rate in "Gb/s" is confusing because that's how we express MAC rates.
SuggestedRemedy
Something like:
The 400GBASE-ZR PCS has a nominal transfer rate rate at the 8-wide PMA service interface of 59.84375 x (28/29) Gtransfers/s +/- 20 ppm for a total of ~462.2414 Gtransfers/s.
Response Response Status C
ACCEPT IN PRINCIPLE.
See response to comment #346.

Cl 155 SC 155.2.1 P 36 L 14 # 430
Dawe, Piers Nvidia
Comment Type E Comment Status A rewrite bucket
"receives two streams of digitally encoded m-bit 16QAM symbols" we need an explanation of why "m-bit".
SuggestedRemedy
Add sentence explaining that m is an implementation choice, for SD-FEC.
Response Response Status C
ACCEPT IN PRINCIPLE.
See response to comment #346.
Comment #433

**Comment Type**: T  **Comment Status**: A  **Rewritten**: Bucket

"transmit data is encoded with a concatenated forward error correction (CFEC) code consisting of an inner SC-FEC code and an outer Hamming code SD-FEC": this is intuitive but not the accepted (Forney's) use of inner and outer.

**Suggested Remedy**

transmit data is encoded with a concatenated forward error correction (CFEC) code consisting of an outer SC-FEC code and an inner Hamming code SD-FEC

**Response**

**Response Status**: C

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Comment #434

**Comment Type**: T  **Comment Status**: A  **Rewritten**: Bucket

As interleavers are a significant feature of this scheme

**Suggested Remedy**

Mention the interleavers in the transmit direction. (There is one mention in the receive direction.)

**Response**

**Response Status**: C

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Comment #437

**Comment Type**: E  **Comment Status**: A  **Rewritten**: Bucket

PCS Receive process

**Suggested Remedy**

PCS Receive function or PCS receive process

**Response**

**Response Status**: C

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Comment #438

**Comment Type**: T  **Comment Status**: A

SC-FEC blocks of 510 x 512

**Suggested Remedy**

whats? bits? bytes?

**Response**

**Response Status**: C

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Comment #439

**Comment Type**: E  **Comment Status**: A

SC-FEC codewords (as on line 39)

**Response**

**Response Status**: C

ACCEPT IN PRINCIPLE.

See response to comment #346.

---

Comment #440

**Comment Type**: E  **Comment Status**: A

257B

**Suggested Remedy**

257-bit, many places. Compare base doc. "256B/257B" can stay.

**Response**

**Response Status**: C

ACCEPT IN PRINCIPLE.

See response to comment #346.
IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

**Response #443**

**Comment ID**: 443  
**Comment Type**: E  
**Comment Status**: A  
**Rewritten**:  
**Dawe, Piers**  
**Nvidia**  
**Comment Type**: E  
**Comment Status**: A  
**Rewritten**:  
**ITU-T G.709 Clause 9.4.3.2**

**Suggested Remedy**:  
ITU-T G.709 Clause 19.4.3.2 ?

**Response**:  
See response to comment #346.

**Response #445**

**Comment ID**: 445  
**Comment Type**: T  
**Comment Status**: A  
**Rewritten**:  
**Dawe, Piers**  
**Nvidia**  
**Comment Type**: T  
**Comment Status**: A  
**Rewritten**:  
**The clock rate of the 400GBASE-ZR frame (GMP clock domain) is not given, although 155.1.4 gives the PMA service interface rate**

**Suggested Remedy**:  
Define the GMP rate in the PCS section

**Response**:  
See response to comment #346.

**Response #446**

**Comment ID**: 446  
**Comment Type**: E  
**Comment Status**: A  
**Rewritten**:  
**Dawe, Piers**  
**Nvidia**  
**Comment Type**: E  
**Comment Status**: A  
**Rewritten**:  
```plaintext
-10 214.684 -eh?
```

**Suggested Remedy**:  
Wow, this is hard to read! Spaces inside indivisible things such as numbers or variable names are bad!

**Response**:  
See response to comment #346.

**Response #448**

**Comment ID**: 448  
**Comment Type**: TR  
**Comment Status**: A  
**Rewritten**:  
**Dawe, Piers**  
**Nvidia**  
**Comment Type**: TR  
**Comment Status**: A  
**Rewritten**:  
**G.709.1 is not a normative reference**

**Suggested Remedy**:  
Remove GMP, define the 256-frame multi-frame sequence here, or add the reference

**Response**:  
See response to comment #346.
Comment ID 450
Dawe, Piers  Nvidia

Comment Type TR
Comment Status rewrite bucket

"The RPF bit indicates signal fail status was detected by the remote 400GBASE-ZR receive function": why is this here? Doesn't Ethernet RF do that job?

SuggestedRemedy
If the idea is that a 400GBASE-ZR PHY should continue to transmit data while its input is bad, then changes elsewhere would be needed for unidirectional operation

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 451
Dawe, Piers  Nvidia

Comment Type E
Comment Status rewrite bucket

Two sections, both called "Link status monitoring and signaling", say different things about e.g. STAT<6> 155.2.5.7.2 says "in the received STAT<6>", this earlier Tx one doesn't have the equivalent.

SuggestedRemedy
Add extra words to make the context clear. "in the transmitted" would help, but more may be needed

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 452
Dawe, Piers  Nvidia

Comment Type T
Comment Status rewrite bucket

"the received status byte in the receive direction": eh?

SuggestedRemedy
Change "then the value of RD in STAT<6> is set to the value of LD in STAT<6> of the received status byte in the receive direction" to "then the value of RD in the transmitted STAT<6> is set to the value of LD in the received STAT<6>"?

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 453
Dawe, Piers  Nvidia

Comment Type TR
Comment Status rewrite bucket

Reference to OIF-400ZR-01.0, March 10, 2020, subclause 8.9. Note that this document is subject to active maintenance

SuggestedRemedy
If feasible, write the specification here. If not, check that the reference is complete, correct and detailed enough, add a normative reference. Refer to a later OIF-400ZR if appropriate.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 454
Dawe, Piers  Nvidia

Comment Type T
Comment Status rewrite bucket

Needs a figure showing the 400GBASE-ZR frame rows, SC-FEC blocks, CRC32 and MBAS

SuggestedRemedy
Please add a figure per comment.

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.

Comment ID 455
Dawe, Piers  Nvidia

Comment Type T
Comment Status rewrite bucket

between source and sink

SuggestedRemedy
eh? Change to the usual terminology

Response
ACCEPT IN PRINCIPLE.

See response to comment #346.
<table>
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<tr>
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<th>CI</th>
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Dawe, Piers, Nvidia

**Comment Type:**的技术要求
**Comment Status:**接受
**Response Status:**已写

1. **Comment:** 定义 x
   **Suggested Remedy:**
   - 定义 x

2. **Comment:** 哪一端先发送？
   **Suggested Remedy:**
   - 在 #346 中接受原则。

3. **Comment:** 需要更多信息。给定“生成多项式”，需要做什么？这里有关生成的示例？
   **Suggested Remedy:**
   - 需要良好定义的示例？

4. **Comment:** 这里说 8 位符号，155.2.1 说两路 4 位数据。
   **Suggested Remedy:**
   - 这个差异在我们讨论抖动限制时可能很重要。

**Comment ID:** 464

10/20/2022 10:55:57 A
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<td>155.2.5.1</td>
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<td>11</td>
<td>“The Hamming SD-FEC decoder is a soft decision decoder”</td>
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<td>11</td>
<td>“Logic described generically in ITU-T G.709.3 Annex D”: generically - vague, and Annex D doesn't address FEC decoding at all, only check-block generation.</td>
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Comment Type: T/technical required  ER/editorial required  GR/general required  T/technical  E/editorial  G/general
COMMENT STATUS: D/dispatched  A/accepted  R/rejected  RESPONSE STATUS: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn
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<td>L 40</td>
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<td>in Clause 45 and why green when line 4 has black?</td>
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<td>FEC degraded SER activate threshold register should be PCS FEC degraded SER activate threshold register, but it’s for Clause 119 PCS RS(544,514) FEC and there is no FEC degraded SER feature in this draft.</td>
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<td>Delete the four FEC degraded SER rows</td>
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IEEE P802.3cw D2.0 400 Gb/s over DWDM systems Initial Working Group ballot comments

**Comment ID 491**

**Cl 155 SC 155.5.1 P 67 L 47 # 491**

Dawe, Piers Nvidia

**Comment Type** E  **Comment Status** A
broken variable names

**SuggestedRemedy**
Widen the right column width until they fit

**Response**
**Response Status** C
ACCEPT IN PRINCIPLE.
See response to comment #346.

**Comment ID 498**

**Cl 156 SC 156.3.2 P 75 L 52 # 498**

Dawe, Piers Nvidia

**Comment Type** TR  **Comment Status** A
Are these Skew and SV limits plausible? What does the PMA need? This is a hybrid of "parallel" and "serial", needs new numbers.

**SuggestedRemedy**
Revise to limits that are appropriate to DP-16PAM technology and the channel.

**Response**
**Response Status** W
ACCEPT IN PRINCIPLE.
See response to comment #346.

**Comment ID 581**

**Cl 120A SC 120A.6 P 103 L 43 # 581**

Dawe, Piers Nvidia

**Comment Type** E  **Comment Status** A
two 400GMII and 400GAUI-8 interfaces

**SuggestedRemedy**
Only one 400GAUI-8 interface

**Response**
**Response Status** C
ACCEPT IN PRINCIPLE.
See response to comment #582.