Cl **FM** *SC* **FM** *P* **3** *L* **18** # 154

Grow, Robert — RMG Consulting

Comment Type **ER** *Comment Status* **A** *bucket*

This is not the current mandatory front matter. Because it contains legal disclaimers and notices it should be current.

SuggestedRemedy

Replace mandatory frontmatter with that in the current IEEE SA templates.

Response *Response Status* **U**

ACCEPT.

Cl **116** *SC* **116.1.3** *P* **27** *L* **22** # 419

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **R**

The manipulations described in this draft don't describe a BASE-R "native Ethernet"; rather, they are like 10GBASE-W. An Ethernet signal is packed into a telecoms wrapper (then, based on SONET, here, based on OTN).
The combination is clumsy and messy. Starting from Ethernet building blocks, one would not engineer it like this. I understand that the rationale is because those designs were already there, and the cost of a clean design was thought to outweigh the inefficiencies of this scheme. But that calls "broad market potential" into question.
800G coherent will affect the market for this.

SuggestedRemedy

I can think of three options:

Redo Clause 155, leaving out GMP and FAW and simplifying the training sequence and pilot sequence to make an Ethernet PHY;

Cancel this project, and encourage those interested to feed their learnings into OIF's "400ZR" maintenance;

Rename this PHY to 400GBASE-ZW, which is more honest and leaves the "400GBASE-ZR" name available to any future native Ethernet PHY, should the broad market potential be found.

Response *Response Status* **U**

REJECT.

No consensus within the CRG to change the name of the 400GBASE-ZR PHY

Cl **116** *SC* **116.1.4** *P* **28** *L* **10** # 164

Grow, Robert — RMG Consulting

Comment Type **TR** *Comment Status* **A**

Base text is not correct. P802.3db/D3.2 inserted two columns under clause 167 (400GBASE-SR4 PMD is missing). The column is also missing from P802.3ck/D3.3

SuggestedRemedy

Add column for 400GBASE-SR4 PMD under Clause 157 as found in the latest version of P802.3db (or if approved or published IEEE Std 802.3db).

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See response to comment 4

Cl **155** *SC* **155.1.5** *P* **35** *L* **1** # 427

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **R**

This PCS is too complicated for just a "directive" specification. We need examples.

SuggestedRemedy

Create examples of e.g. FEC and other blocks before and after coding. Smallish ones can go in the document, all can be uploaded to the directory that IEEE provides for these things. They might need to cover some of the PMA.

Response *Response Status* **U**

REJECT.

A detailed suggested remedy containing an editor's instruction on how to modify the draft was not provided.

The following straw poll was taken:

I would support rejecting comment #427
Yes - 10
N- 2

Cl **155** *SC* **155.2.4.11** *P* **44** *L* **36** # 463

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **R**

generic operation ... in ITU-T G.709.3 Annex D: but that contains undefined symbols and terms.

SuggestedRemedy

As it seems it is not very long, write it out cleanly here

Response *Response Status* **U**

REJECT.

No consensus to make a change.

Cl **155** *SC* **155.3.1.3** *P* **51** *L* **26** # 345

Zimmerman, George — CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type **TR** *Comment Status* **A** *rewrite bucket*

This figure is supposed to be a functional block diagram, not an implementation diagram. There are no characteristics for the DAC blocks defined in the specification. The closest thing in the text is 155.3.3.4 which are called the 16QAM encode and signal drivers. However, most other 802.3 PHY clauses leave out signal drivers, DACs and the like, and there are no specific requirements in 155.3.3.4, so deleting the blocks seems the right approach to making a functional block diagram.

SuggestedRemedy

Preferably, delete the "DAC" blocks from Figure 155-10 (going straight to the output is fine)
Alternatively, Relabel "16QAM Encoder and Signal Driver" (probably drawing as 2 blocks since you show I&Q paths)

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl **155** *SC* **155.3.3.1** *P* **52** *L* **28** # 342

Zimmerman, George — CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type **TR** *Comment Status* **A** *rewrite bucket*

"The received symbol signals are digitized into more than 4 discrete levels by the analog to digital converters (ADC) in the PMA sublayer and the number of bits for each signal is m/4 bits." This is a description of an implementation and is inappropriate for an interoperability standard. If some description is needed, one could rewrite this more generally, as is suggested in the remedy. Further, it appears that the "m/4 bits" is a detail that is unused in the draft (I searched). If it is used somewhere, please provide a pointer to where it is relevant. Otherwise delete the unnecessary detail which looks like a specification but isn't.

SuggestedRemedy

Preferably - delete the indicated sentence.
Alternatively, change the indicated sentence to read "The received symbol signals are sampled and quantized in the PMA sublayer."
If the m/4 bits is used somewhere, provide a reference.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl **155** *SC* **155.3.3.5** *P* **58** *L* **45** # 343

Zimmerman, George — CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type **TR** *Comment Status* **A** *rewrite bucket*

"The signals are sampled by an ADC on each lane at a sampling rate." "The details of the ADC . are implementation specific". This is a description of an implementation, not appropriate for an interoperability specification. If someone could do the signal processing optically, analog, or by magic, it would still comply with the standard. The fact that an ADC is used, isn't a part of the interoperability standard, or even any of the characteristics of the ADC. Hence the mention is inappropriate and should be deleted. The sentence works just fine anyways and describes the processing without the "by an ADC".

SuggestedRemedy

Change header of 155.3.5 to Receive signal sampling.
On line 50, Delete "by an ADC"
Change line 54 to "The details of the sampling, including any quantization and the chosen sampling rate are implementation specific."
Replace "ADC" with "Sampler" in figure 155-10.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl **155** *SC* **155.3.3.5** *P* **58** *L* **45** # 341

Zimmerman, George — CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type **TR** *Comment Status* **A** *rewrite bucket*

"The signals are sampled by an ADC on each lane at a sampling rate." "The details of the ADC . are implementation specific". This is a description of an implementation, not appropriate for an interoperability specification. If someone could do the signal processing optically, analog, or by magic, it would still comply with the standard. The fact that an ADC is used, isn't a part of the interoperability standard, or even any of the characteristics of the ADC. Hence the mention is inappropriate and should be deleted. The sentence works just fine anyways and describes the processing without the "by an ADC".

SuggestedRemedy

Change header of 155.3.5 to Receive signal sampling.
On line 50, Delete "by an ADC"
Change line 54 to "The details of the sampling, including any quantization and the chosen sampling rate are implementation specific."
Replace "ADC" with "Sampler" in figure 155-10.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See response to comment #346.

Cl **155** *SC* **155.7.4.1** *P* **70** *L* **24** # 346

Zimmerman, George — CME Consulting/APL Group, Cisco, Commscope, Ma

Comment Type **TR** *Comment Status* **A** *rewrite bucket*

This is a general comment on the requirements. I am attaching it to these PICS because this is where it became apparent. The style of IEEE SA standards (and IEEE Std 802.3) is that requirements use the term "shall". Each PICS item should have an associated "shall" and each "shall" should have a PICS. However, 155.7.4.1 is a list of the subclauses for the most part. Further, looking at the subclauses, they are largely without "shalls". Most of the items in clause 155 are descriptive of an implementation, and do not use the term shall. They use "is" or other descriptive language. The PICS are a list of the functional blocks described, but most of those functional blocks are lacking actual requirements. Instead they often describe an implementation or, worse yet, sometimes try to require a particular implementation ("an implementation shall"). What needs to happen is that the clause needs to be rewritten carefully considering what requirements are needed for interoperability, and deleting the unnecessary implementation description. This is a big job, and, in my opinion, means the draft is not technically complete, and should not have begun initial working group ballot. I truly regret having to make a comment like this, but I believe this is a great example of why we have working group ballots in 802.

SuggestedRemedy

Unfortunately, the draft is so far from complete that I cannot propose a specific remedy for the systematic problem. I can suggest that the TF look at each subblock, determine what the observed behavior is, determine which parts matter to interoperability, and write "shall" statements in the subclauses. Then those shall statements can be made as PICS. Additionally, this will highlight where there is implementation description that can be deleted. When this is done, restart working group ballot.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

With editorial license, restructure and clarify Clause 155 and 156 as appropriate:
to identify interoperability requirements using “SHALL” statements, as needed.
to address issues noted in
https://www.ieee802.org/3/cw/public/22_10/dambrosia_3cw_01b_221018.pdf

Cl **156** *SC* **156.7** *P* **84** *L* **22** # 334

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **R**

The receiver must tolerate 26 dB OSNR and meet the requried error rate, it is not clear what receive OSNR (min) of 29 dB provides

SuggestedRemedy

Need discustions on the intent

Response *Response Status* **U**

REJECT.

Receiver OSNR tolerance is measured without line immpairments, see 156.9.24, which is different than Receiver OSNR which includes line impairments, see 156.9.23

Cl **156** *SC* **156.7.1** *P* **82** *L* **48** # 337

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **R**

For full interoperability using EVM may need additional constrains based on the data in rahn_3cw_01a_220223 and way_3cw_01a_220523

SuggestedRemedy

Need more data to prove that EVM will provide the IEEE level of interoperability

Response *Response Status* **U**

REJECT.

No suggested remedy provided

Cl **156** *SC* **156.10.1.1** *P* **93** *L* **44** # 336

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **TR** *Comment Status* **R**

Assuming just 4 bits ENOB from 10 MHz to 29.9 MHz the reference receiver will have additional penalty than real receiver that has typically 6+ bits ENOB at low frequncies and about 4 bits at high frequncy

SuggestedRemedy

If there is interest I can bring a frequncy dependent ENOB mask

Response *Response Status* **U**

REJECT.

No suggested remedy provided

Cl **156** *SC* **156.10.1.2.2** *P* **94** *L* **36** # 564

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **R**

Need a bigger block size for at least one of these, to go with the jitter corner frequency

SuggestedRemedy

Response *Response Status* **U**

REJECT.

The CRG had no consensus to make a change at this, more study on a suitable solution is required.