In support of comments #8, 9, 10, 11 against D1.2

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Nov 15th, 2021

IEEE P802.3cw 400 Gb/s over DWDM systems Task Force

Comment #8: Need detailed functions and state machines at 155.4

PCS block diagram

Transmit state diagram from Fig 119-14

Receive state diagram from Fig 119-15

AM synchronization state diagram (new)

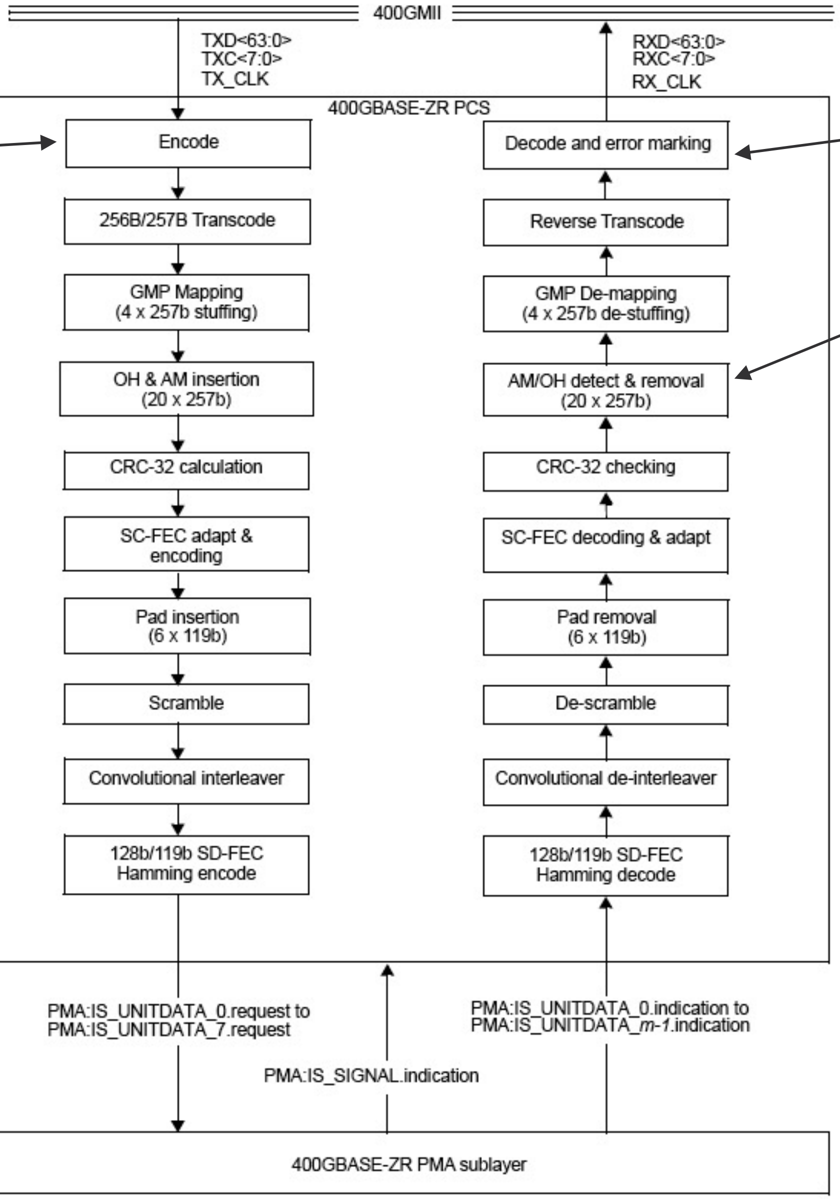
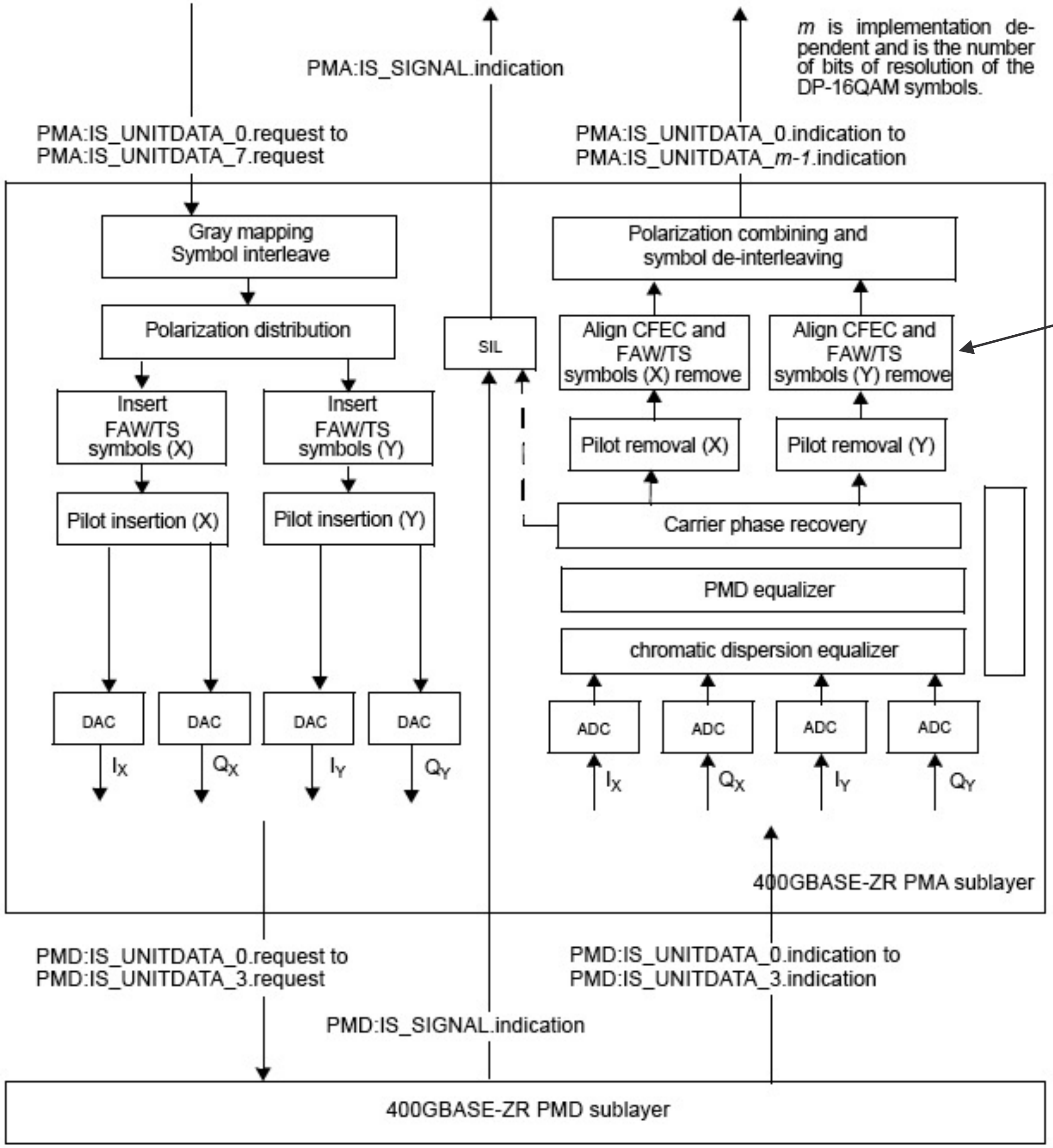


Figure 155–2—Functional block diagram

PMA block diagram



DSP FAW synchronization state diagram and PMA deskew state diagram (new)

Where are new state diagrams needed? PCS receive direction

4 physical lanes from PMD

3.04 µs

DSP super-frame: 181888 symbols

Align to DSP super-frame FAW sequence on 4 physical lanes
Remove FAW, TS, PS and rsvd symbols

← DSP FAW synchronization state diagram and PMA deskew state diagram (new)

Hamming FEC input: 175616 symbols (10976 x 16)

119/(16 x 8)

Hamming FEC output: 1306144 bits (10976 x 119)

De-interleave, de-scramble, remove 6x119b pad

SC-FEC input: 1305430 bits (10970 x 119 = 5 x 261086)

Remove 5x (parity blocks+CRC-32+MBAS)

CRC-32 bytes to checker
MBAS used by SC-FEC decoder

SC-FEC output: 1223320 bits (5 x 244664)

Align to AM block (1920b). Assemble ZR frames from ~ 10.7563 SC-FEC output blocks.

← AM synchronization state diagram (new)

6.54 µs

400GBASE-ZR frame: 2631680 bits (256 x 10280)

Remove AM, OH, pad bits (5140b)

STAT bytes to RPF and link degrade signaling
MFAS/ JC1-JC6 to GMP demapper

GMP input: 2626540 bits (10220 x 257B)

Remove GMP stuff data (2 to 6 times 1028b over 4 frames)

GMP output: (10214 to 10218) x 257B

Reverse transcode. Decode 66B to 400GMII outputs.

← Receive state diagram from clause 119 (Figure 119-15) + associated state variables

Decoder output: (40856 to 40872) x 72b

DSP FAW lock state diagram

- Based on 802.3ct Figure 153-7 with fas replaced by faw, and fecl replaced by pmal
- 4 lanes instead of 20

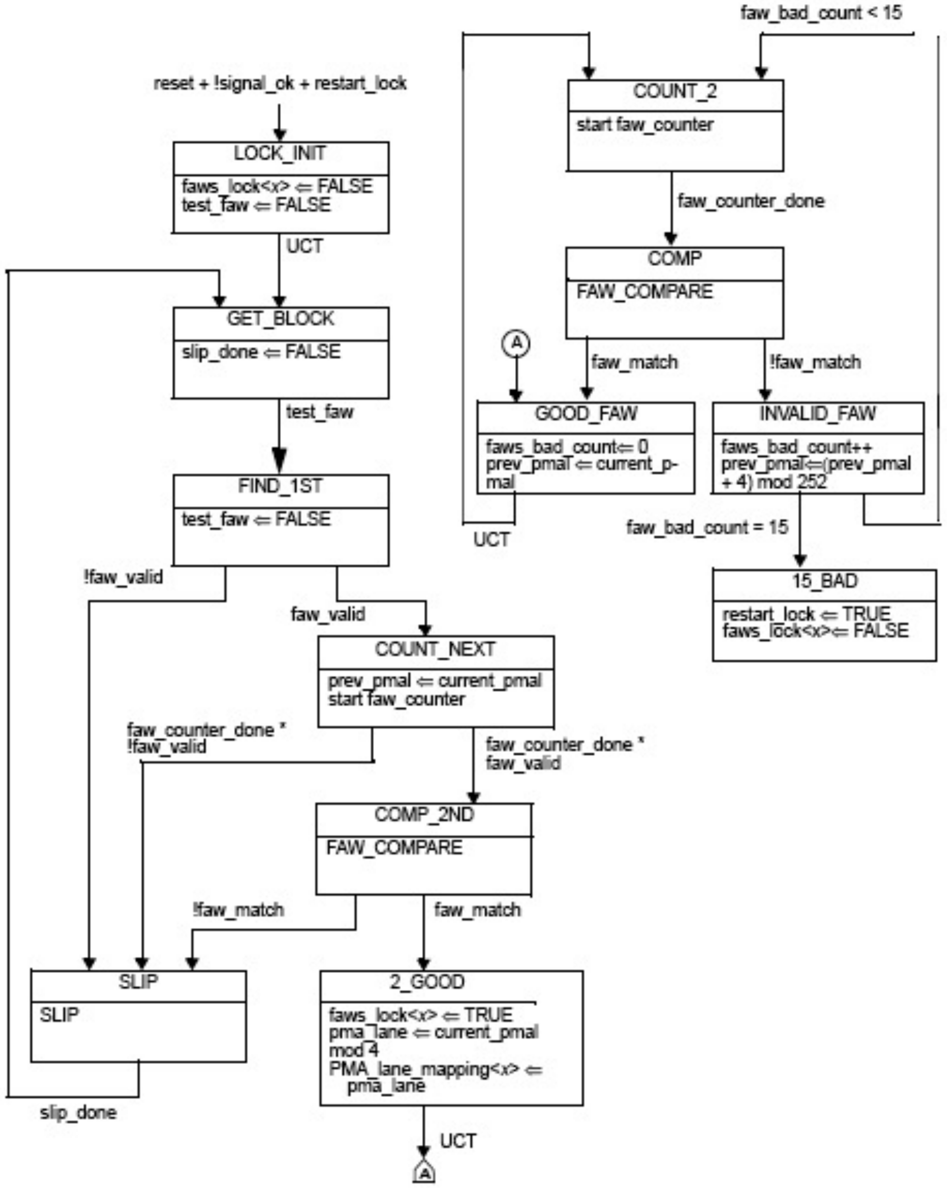


Figure 155–13—DSP FAW synchronization state diagram

PMA deskew state diagram

- Based on 802.3ct Figure 153-8 with fec_align replaced by pma_align

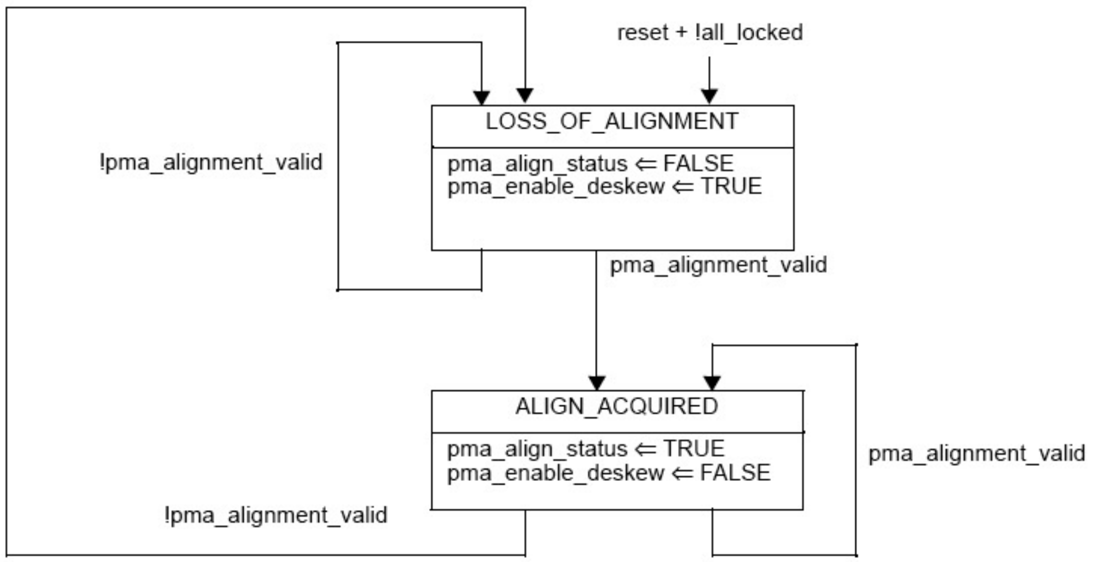


Figure 155–14—PMA deskew state diagram

Alignment marker lock state diagram

- Based on Figure 119-12 (400GBASE-R PCS) but for a single lane
- No need for lane mapping
- Look for all 1920 bits (16x120) instead of just a single 120-bit sequence?

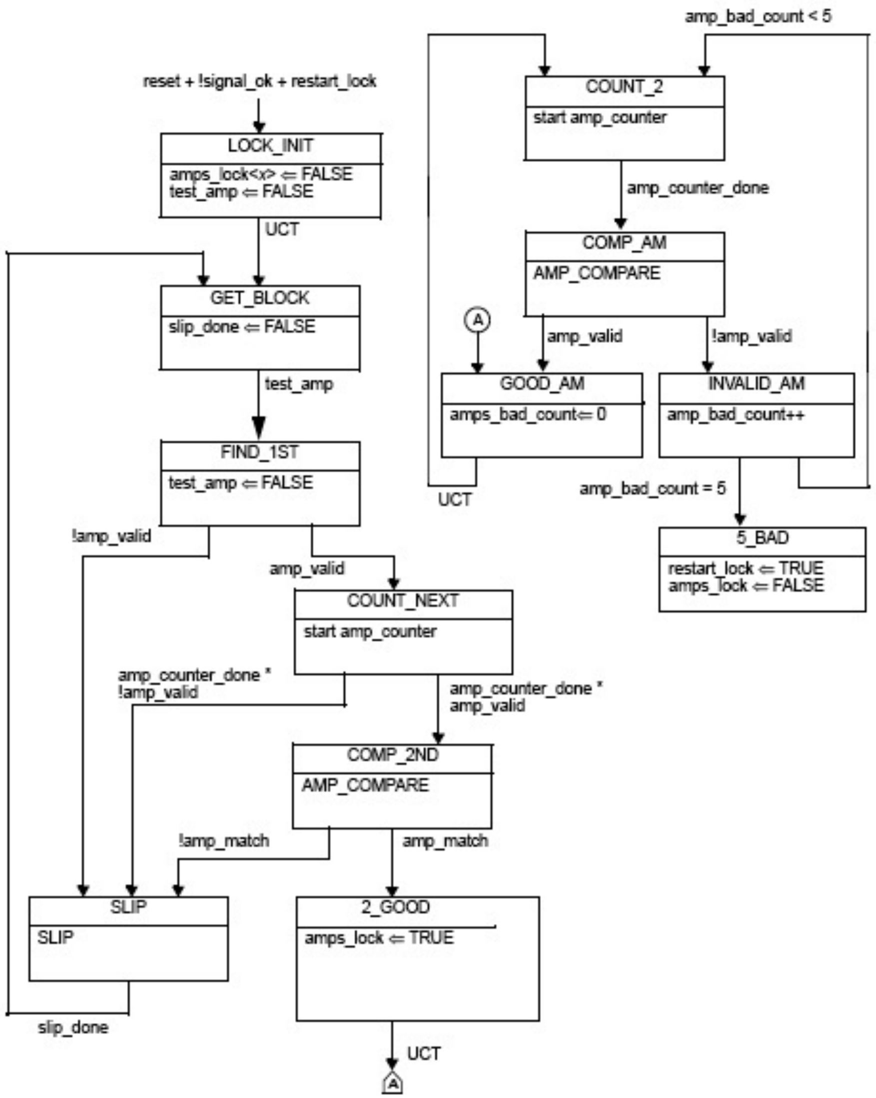


Figure 155–15—Alignment marker lock state diagram

Accompanying proposed text:

155.4 400GBASE-ZR PCS and PMA detailed functions and state diagrams

Editor's Note (to be removed prior to publication):
Task force has not yet considered a baseline for detailed functions and state diagrams.

The body of this subclause includes state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

155.4.1 State variables

155.4.1.1 Variables

align_status
amp_counter_done
amp_match
amp_valid
amps_lock
cw_bad
hi_ser
PCS_status
rx_local_degraded
rx_rm_degraded

all_locked
A Boolean variable that is set to TRUE when faws_lock<x> is TRUE for all x and is set to FALSE when faws_lock<x> is FALSE for any x.

current_pmal
A variable that holds the PMA lane identification octet corresponding to the current FAW that is recognized on a given lane of the PMA service interface. The value of this variable modulo 4 represents the PMA lane number. It is compared to the expected value based on the variable prev_pmal to confirm that the location of the FAW has been detected. This value is interpreted with the most significant bit transmitted first

faws_counter_done
Boolean variable that indicates that faws_counter has reached its terminal count.

faw_match
Boolean variable that holds the output of the function FAW_COMPARE.

faw_valid
Boolean variable that is set to TRUE if the received 22-symbol sequence is a valid FAW. The FAW consists of one of the sequences listed in Table 155–3. The sequence is considered to be valid if at least TBD symbols match the known bits of the pattern described in 155.3.3.3.1.

faws_lock<x>
Boolean variable that is set to TRUE when the receiver has detected the location of the FAW for a given lane on the PMA service interface, where x = 0:3.

pma_align_status
A Boolean variable set by the PMA alignment process to reflect the status of PMA lane-to-lane alignment. Set to TRUE when all lanes are synchronized and aligned and set to FALSE when the deskew process is not complete.

pma_alignment_valid
Boolean variable that is set to TRUE if all PMA lanes are aligned. PMA lanes are considered to be aligned when faws_lock<x> is TRUE for all x, each PMA lane has a unique lane number, and the PMA lanes are deskewed. Otherwise, this variable is set to FALSE.

pma_enable_deskew
A Boolean variable that indicates the enabling and disabling of the deskew process. Data may be discarded whenever deskew is enabled. TRUE when deskew is enabled. FALSE when deskew is disabled.

pma_lane
A variable that holds the PMA lane number (0 to 3) received on lane x of the PMA service interface when faws_lock<x> = TRUE. The PMA lane number is determined by matching the received 22-symbol sequence to the values in one of the columns of Table 155–3, interpreted with the most significant bit transmitted first, modulo 4. It is set to current_pmal modulo 4 when the expected FAW is found in the expected location in a second consecutive DSP super-frame.

PMA_lane_mapping<x>
This variable indicates which PMA lane is received on lane x of the PMA service interface when faws_lock<x> = TRUE, where x = 0:3.

prev_pmal
A variable that holds the value of the lane identification octet (or the expected value of the lane identification octet) from the previous DSP super-frame. The value is interpreted with the most significant bit transmitted first. The lane represented is this value modulo 4. It is used to calculate the expected value of the lane identification octet in the next DSP super-frame period that is tested.

reset
Boolean variable that controls the resetting of the PMA sublayer. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO and during power on.

restart_lock
Boolean variable that is set by the PMA alignment process to reset the synchronization process on all PMA lanes. It is set to TRUE when 15 FAWs in a row fail to match (15_BAD state).

rx_align_status
Boolean variable that is set by the receive signal processing function (see 155.3.3.6).

signal_ok
Boolean variable that is set based on the most recently received value of PMA:IS_SIGNAL.indication (SIGNAL_OK). It is TRUE if the value was OK and FALSE if the value was FAIL.

slip_done
Boolean variable that is set to TRUE when the SLIP requested by the DSP FAW synchronization state diagram has been completed indicating that the next candidate FAW position can be tested.

test_faw
Boolean variable that is set to TRUE when a candidate FAW position is available for testing and FALSE when the FIND_1ST state is entered.

155.4.1.2 Functions

AMP_COMPARE
FAW_COMPARE
This function compares the FAW with its expected value to determine if a valid frame alignment word sequence has been detected and returns the result of the comparison using the variable faws_match. FAW_COMPARE is TRUE if faw_valid is TRUE, and current_pmal (interpreted with the most significant bit transmitted first) is equal to the prev_pmal plus 4 modulo 252. Otherwise, faws_match is FALSE.

SLIP
Causes the next candidate FAW position to be tested. The precise method for determining the next candidate FAW position is not specified and is implementation dependent. However, an implementation shall ensure that all possible frame alignment word positions are evaluated.

155.4.1.3 Counters

amp_bad_count
Counts the number of consecutive AM blocks that don't match the expected value.

amp_counter
Counts the interval of 10 240 257B blocks containing normal AM sequences.

cw_bad_count
Counts the number of uncorrected SC-FEC codewords. This counter is set to zero when an SC-FEC codeword is received and cw_bad is false.

faws_bad_count
Counts the number of consecutive FAWs that don't match the expected value for a given PMA lane.

faw_counter
Counts the 181 888 symbols between the starting position of one FAW and the expected starting position of the next FAW on a PMA lane. This counter starts with a value of zero when start faw_counter is asserted (at the position of the first symbol of a matched FAW pattern on a PMA lane), is incremented for each symbol on that PMAlane, and reaches a terminal value of 181 888 at the expected position of the next FAW pattern on that PMA lane.

155.4.1.4 State diagrams

The PMA shall implement 4 DSP FAW synchronization processes as shown in Figure 155–13 to identify the boundaries of DSP super-frames by observing the stream of symbols on four physical lanes. The synchronization process operates independently on each lane. The synchronization state diagram determines when the PMA has detected the location of the frame alignment word sequence in the received symbol stream for a given lane of the PMA service interface.

The PMA shall also implement the deskew process as shown in Figure 155–14.

The PCS shall implement the alignment marker lock process as shown in Figure 155–15 to identify the AM sequence at the start of each 400GBASE-ZR frame by observing data from the SC-FEC decoder output.

Comment #9: Need management information at 155.5.

Defer to next meeting, pending decision on state machines (comment #8)

Comment #10: Need loopback information at 155.6.

Defer to next meeting, pending decision on state machines (comment #8)

Comment #11: Need PICs tables at 155.8.

Defer to next meeting, pending decision on state machines (comment #8)