

In support of comments #9 & 11 against D1.2

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IEEE P802.3cw 400 Gb/s over DWDM systems Task Force

Comment #9: Need management information at 155.5.

400GBASE-ZR PCS and PMA MDIO function mapping

- With the acceptance in principle of comment #8 we will have detailed definitions of variables, counters and state diagrams for Tx and Rx directions
- The following maps control and status variables for the 400GBASE-ZR PCS/PMA to existing MDIO registers, including those added by 802.3ct

400GBASE-ZR PCS/PMA MDIO function mapping: control variables

MDIO control variable	MDIO register name	Register/bit number	ZR-PCS/PMA variable
Reset	PCS control 1 register	3.0.15	reset
Loopback	PCS control 1 register	3.0.14	loopback
Transmit test-pattern enable	BASE-R PCS test-pattern control register	3.42.3	tx_test_mode
LPI_FW	EEE control and capability	3.20.0	LPI_FW
FEC degraded SER enable	PCS FEC control register	3.800.2	FEC_degraded_SER_enable
FEC degraded SER activate threshold	FEC degraded SER activate threshold register	3.806, 3.807	FEC_degraded_SER_activate_threshold
FEC degraded SER deactivate threshold	FEC degraded SER deactivate threshold register	3.808, 3.809	FEC_degraded_SER_deactivate_threshold
FEC degraded SER interval	FEC degraded SER interval interval	3.810, 3.811	FEC_degraded_SER_interval

400GBASE-ZR PCS/PMA MDIO function mapping: status variables

MDIO status variable	MDIO register name	Register/bit number	ZR-PCS/PMA variable
Receive link status	BASE-R and MultiGBASE-T PCS status 1 register	3.32.12	PCS_status
SC-FEC AM lock	SC-FEC align status	1.2246.12	amps_locked
FEC corrected codewords	SC-FEC corrected codewords counter register	1.2276, 1.2277	FEC_corrected_cw_counter
FEC uncorrected codewords	SC-FEC uncorrected codewords counter register	1.2278, 1.2279	FEC_uncorrected_cw_counter
FEC total bits	SC-FEC total bits register	1.2280, 1.2281, 1.2282, 1.2283	FEC_total_bits_counter
FEC corrected bits	SC-FEC corrected bits register	1.2284, 1.2285, 1.2286, 1.2287	FEC_corrected_bits_counter
Tx LPI indication	PCS status 1	3.1.9	Tx LPI indication
Tx LPI received	PCS status 1	3.1.11	Tx LPI received
Rx LPI indication	PCS status 1	3.1.8	Rx LPI indication
Rx LPI received	PCS status 1	3.1.10	Rx LPI received
EEE wake error counter	EEE wake error counter	3.22	Wake_error_counter
FEC degraded SER ability	PCS FEC status register	3.801.3	FEC_degraded_SER_ability
FEC degraded SER	PCS FEC status register	3.801.4	FEC_degraded_SER
Local degraded SER received	PCS FEC status register	3.801.6	rx_local_degraded
Remote degraded SER received	PCS FEC status register	3.801.5	rx_rm_degraded
FEC high SER	PCS FEC status register	3.801.2	hi_ser
Lane x aligned, x = 0 to 3	Multi-lane BASE-R PCS alignment status 3 register	3.52.3:0	faws_lock<x>
PCS lane alignment status	Multi-lane BASE-R PCS alignment status 1 register	3.50.12	pma_align_status
Lane x mapping, x=0 to 3	Lane x mapping register	3.400 through 3.403	pma_lane_mapping<x>

Proposed actions

- Add the 2 new tables on previous pages to 155.5 and add text descriptions with editorial license
- Also add (comment hijack) the following new entries to Table 156-2 and 156-3 in the PMD subclause:

Table 156-2

MDIO control variable	PMA/PMD register name	Register/bit number	PMD control variable
Reset	PMA/PMD control 1 register	1.0.15	PMD_reset
Global PMD transmit disable	PMD transmit disable register	1.9.0	PMD_global_transmit_disable
Tx optical channel index	Tx optical channel control register	1.800.5:0	Tx_optical_channel_index
Rx optical channel index	Rx optical channel control register	1.820.5:0	Rx_optical_channel_index

Proposed actions (cont'd)

Table 156-3

MDIO status variable	PMA/PMD register name	Register/bit number	PMD status variable
Fault	PMA/PMD status 1 register	1.1.7	PMD_fault
Transmit fault	PMA/PMD status 2 register	1.8.11	PMD_transmit_fault
Receive fault	PMA/PMD status 2 register	1.8.10	PMD_receive_fault
Global PMD receive signal detect	PMD receive signal detect register	1.10.0	PMD_global_signal_detect
Tx index ability 0 to Tx index ability 63	Tx optical channel ability 1 register to Tx optical channel ability 4 register	1.801 to 1.804	Tx_index_ability_0 to Tx_index_ability_63
Tx Rx different optical channel ability	Rx optical channel control register	1.820.15	Tx_Rx_diff_opt_chan_ability
Rx index ability 0 to Rx index ability 63	Rx optical channel ability 1 register to Rx optical channel ability 4 register	1.821 to 1.824	Rx_index_ability_0 to Rx_index_ability_63

Comment #11: Need PICs tables at 155.8.

PICs tables – major capabilities & options

Item	Feature	Subclause	Value/Comment	Status	Support
DC	Delay constraints	155.7	Device conforms to delay constraints	M	Yes []
MD	MDIO capability	155.5	Registers and interface supported	O	Yes [] No []
EEE	EEE capability	156.1	Capability is supported	O	Yes [] No []
JTM	Supports test-pattern mode	155.2.1	Capability is supported	M	Yes []
FDD	Support for FEC degraded detection	155.2.4.4.5	The SC-FEC decoder can detect SER degraded at a programmable threshold	M	Yes []

PICs tables – Transmit Function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	400GMII to 64B/66B encoder	155.2.4.1	Generate 66B blocks per 155.2.4.1	M	Yes []
TF2	64B/66B to 256B/257B transcoder	155.2.4.2	tx_xcoded<256:0> constructed per 155.2.4.2	M	Yes []
TF3	GMP mapper	155.2.4.3	Create the 400GBASE-ZR frame and GMP map the 257B encoded blocks into the payload area of the frame, adding stuffing blocks as determined by the rate difference.	M	Yes []
TF4	Alignment marker insertion	155.2.4.4.1	1920 bits (16 x 120) inserted into 400GBASE-ZR frame	M	Yes []
TF5	Pad insertion	155.2.4.4.2		M	Yes []
TF6	Overhead insertion	155.2.4.4.3		M	Yes []
TF7	Frame to SC-FEC adaptation	155.2.4.6		M	Yes []
TF8	Pad insertion	155.2.4.7		M	Yes []
TF9	Frame synchronous scrambler	155.2.4.8		M	Yes []
TF10	Convolutional interleaver	155.2.4.9		M	Yes []
TF11	Hamming SD-FEC encoder	155.2.4.10		M	Yes []
TF12	Transmit bit ordering and distribution	155.2.4.11		M	Yes []
TF13	Gray mapping and polarization distribution	155.3.3.1		M	Yes []
TF14	Symbol interleaving	155.3.3.2		M	Yes []
TF15	Insert FAW, TS and PS symbols	155.3.3.3		M	Yes []
TF16	16QAM encode and signal drivers	155.3.3.4		M	Yes []
TF17	Symbol mapping to physical lanes	155.3.3.4.1		M	Yes []

PICs tables – Receive Function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Receive signal ADCs	155.3.3.5		M	Yes []
RF2	Receive signal processing	155.3.3.6		M	Yes []
RF3	FAW, TS and PS symbol removal	155.3.3.7		M	Yes []
RF4	Polarization combining and symbol de-interleaving	155.3.3.8		M	Yes []
RF5	Hamming SD-FEC decoder	155.2.5.1	Soft decision error correction 16 symbols to 119 bits	M	Yes []
RF6	Convolutional de-interleaver	155.2.5.2		M	Yes []
RF7	Descrambler	155.2.5.3	De-scramble according to 155.2.5.3	M	Yes []
RF8	Remove pad	155.2.5.4		M	Yes []
RF9	SC-FEC decoder	155.2.5.5	Correct errors by decoding SC-FEC parity	M	Yes []
RF10	CRC-32 checker	155.2.5.6		M	Yes []
RF11	Alignment marker lock	155.2.5.7		M	Yes []
RF12	Link status byte extraction	155.2.5.7.2		M	Yes []
RF13	GMP JC1-JC6 extraction	155.2.5.7.1		M	Yes []
RF14	GMP demapping	155.2.5.8	Extract 257B encoded block stream from 400GBASE-ZR frame	M	Yes []
RF15	256B/257B to 64B/66B transcoder	155.2.5.9		M	Yes []
RF16	66B to 400GMII decoder	155.2.5.10		M	Yes []

PICs tables – State Diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	DSP FAW lock state diagram	tbd	Implements four FAW lock processes as depicted in Figure tbd	M	Yes []
SD2	PMA deskew state diagram	tbd	Meets the requirements of Figure tbd	M	Yes []
SD3	Alignment marker lock state diagram	tbd	Implements 1920-bit lock process as depicted in Figure tbd	M	Yes []
SD4	Transmit process	155.2.4.1	Implements transmit state diagram as depicted in Figure 119-14	M	Yes []
SD5	Receive process	155.2.5.10	Implements receive state diagram as depicted in Figure 119-15	M	Yes []

Proposed actions

- Insert PICS tables as presented and update with editorial license
- Possible other PICS tables for:
 - 64B/66B coding rules
 - Scrambler and descrambler
 - Test pattern modes
 - Bit order
 - Management
 - Loopback
 - Delay constraints