Cl **00** *SC* **0** *P* **0** *L* **0** # 5

Hajduczenia, Marek Charter Communications

Comment Type **ER** *Comment Status* **D**

No line numbers in most clauses

SuggestedRemedy

Add line numbers to individual clauses: 30, 45, 90

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **30** *SC* **30.13.1.3** *P* **26** *L* # 3

Hajduczenia, Marek Charter Communications

Comment Type **TR** *Comment Status* **D**

#UpdatesTo45
Multiple Clause 30 attributes need to be updated to match the set of changes already in place in subclauses 45.2.3.66/67/68 and potentially - my other comment (see comment tagged #UpdatesTo45)

SuggestedRemedy

Apply changes to 30.13.1.3, 30.13.1.4, 30.13.1.5, and 30.13.1.6 as shown in the diff highlight in P8023cx_2101_hajduczenia_2.pdf

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.??** *P* *L* # 7

Tse, Richard Microchip Technology

Comment Type **TR** *Comment Status* **D** *SFD*

Add writable register bits to select which message timestamp point to use (if available).

SuggestedRemedy

Add two writeable register bits to the new TimeSync message timestamp point capability register (see earlier comment):

Name and Description:
Select begining of SFD as message timestamp point
Select beginning of symbol after SFD as message timestamp point

Selection enables the corresponding message timestamp point. The register bit is only valid if the corresponding message timestamp point is supported (see corresponding read-only register bit in my previous comment).
Only one of these two register bits can be set to 1 at any time.

Definition for each bit:
0 = not selected
1 = selected

Default value is not defined by the standard. It is set by the implementation.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

While the change is reasonable, it is NOT clear where to add such a register. Should it be added into each and every sublayer capability register (for example, 1.1800.xx) or some place else?

Also, note that in Clause 90, only in 90.7 we reference the option of using SFD or first symbol after SFD. All diagrams, primitive definitions, etc. show SFD only option.

We need to discuss whether we even need to support SFD reference point in .3cx or just switch to post-SFD detection. It would take away the unnecessary optional capability away from implementations.

Cl **45** *SC* **45.2.??** *P* *L* # 6

Tse, Richard Microchip Technology

Comment Type **TR** *Comment Status* **D** *SFD*

Add read-only register bits to indicate which message timestamp points are supported.

SuggestedRemedy

A new register category (e.g., TimeSync message timestamp point capability) needs to be created for these read-only register bits.

Add the following two register bits:

Name and Description:
Beginning of SFD message timestamp point support
Beginning of symbol after SFD message timestamp point support

Definition for each bit:
0 = not supported
1 = supported

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

See comment #7 - it is not clear whether we need R/W or just R capabiluty bit for this function.

Cl **45** *SC* **45.2.3.66** *P* *L* # 9

Tse, Richard Microchip Technology

Comment Type **TR** *Comment Status* **D**

Add read-only register bit to indicate whether 802.3cx TimeSync multi-PCS lane distribution path data delay mechanism is supported.

SuggestedRemedy

Add read-only register bit to TimeSync PCS capability register.

Register bit name::
TimeSync 802.3cx multi-PCS lane path data delay mechanism support

Definition:
0 = not supported
1 = supported

Note: Writeable selection between the two modes is not needed. It is assumed that if the 802.3cx mode is supported, then it is used. if it is not supported, then the operation is specific to the implementation (since 802.3bf did not define how the PCS path data delay is dealt with for the multi-PCS lane distribution operation).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Suggest register 3.1800.4

Propagate change to 45.2.1.146 (PMA/PMD), 45.2.2.20 (WIS), 45.2.4.28 (XS), 45.2.5.28 (DTE), and 45.2.6.14 (TC) subclauses.

Cl **45** *SC* **45.2.3.66** *P* *L* # 8

Tse, Richard Microchip Technology

Comment Type **TR** *Comment Status* **D**

Add read-only register bit to indicate whether TX_num_blk_change and RX_num_blk_change are supported.

SuggestedRemedy

Add read-only register bits to TimeSync PCS capability register.

Name and Description:
TX_num_blk_change_support
RX_num_blk_change_support

Definition for each bit:
0 - does not support the *_num_blk_change function
1 - supports the *_num_blk_change function

Note: Writeable selection between the two modes is not needed. It is assumed that if the *_num_blk_change funciton is supported, then it is used. if it is not supported, then the operation is specific to the implementation (since 802.3bf did not define how PCS path data delay is dealt with for AM/CWM operations).

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Do we really need 2 bits for these? It seems that we only have two states, i.e., they are either supported together or they are not.

Suggest register 3.1800.5

Propagate change to 45.2.1.146 (PMA/PMD), 45.2.2.20 (WIS), 45.2.4.28 (XS), 45.2.5.28 (DTE), and 45.2.6.14 (TC) subclauses.

Cl **45** *SC* **45.2.3.66** *P* **30** *L* # 4

Hajduczenia, Marek Charter Communications

Comment Type **TR** *Comment Status* **D**

There are a number of changes in .3cx relative to .3bf, including timestamp reference point, new calculation rules, as well as support for sub-ns register portions. These need to be properly signalled to the system integrator so that calculations are performed correctly. The easiest way to achieve that is to have additinal capability register embedded in the given sublayer to signal whether the given sublayer does support .3bf or .3cx models.

SuggestedRemedy

Implement changes per P8023cx_2101_hajduczenia_3.pdf shown in highlight. If consented, similar changes need to be implemented in 45.2.1.146 (PMA/PMD), 45.2.2.20 (WIS), 45.2.4.28 (XS), 45.2.5.28 (DTE), and 45.2.6.14 (TC) subclauses, respectively
Add editorial note in aTimeSyncCapabilityTX and aTimeSyncCapabilityRX to make updates to logic calculating values of the given attributes in function of .3bf or .3cx support (likely a function representation with pseudo-code will be needed). This definition will be likely added next cycle when and if changes in this comment are accepted.
Add editorial note to add aTimeSyncCapabilityTypeTX and aTimeSyncCapabilityTypeRX indicating .3bf and .3cx capability for the given system (likely a function representation with pseudo-code will be needed). This definition will be likely added next cycle when and if changes in this comment are accepted.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **45** *SC* **45.2.3.66** *P* **30** *L* # 1

Hajduczenia, Marek Charter Communications

Comment Type **TR** *Comment Status* **D**

#UpdatesTo45
Draft R0.3 introduced a number of consented changes to register 3.1800 adding .2 and .3 registers indicating support for fine resolution (sub-nanosecond) registers at the PCS layer. It also added new registers in 45.2.3.67 and 45.2.3.68 to support fine resolution registers. Now the same set of changes needs to be done to other layers as well, for functional parity.

SuggestedRemedy

Propagate changes from 45.2.3.66/67/68 into the following subclauses 45.2.1.146/147/148 (PMA/PMD), 45.2.2.20/21/22 (WIS), 45.2.4.28/29/30 (XS), 45.2.5.28/29/30 (DTE), and 45.2.6.14/15/16 (TC) subclauses, respectively

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **90** *SC* **90.6** *P* **45** *L* # 2

Hajduczenia, Marek Charter Communications

Comment Type **TR** *Comment Status* **D**

#UpdatesTo45
Table 90-1 needs to be updated to match the set of changes already in place in subclauses 45.2.3.66/67/68 and potentially - my other comment (see comment tagged #UpdatesTo45) Note that even though we show ns and sub-ns registers in Clause 45, we do not show anywhere or reference to anywhere that shows how the resulting number is produced. a

SuggestedRemedy

Add new lines into table 90-1 as shown in the diff highlight in P8023cx_2101_hajduczenia_1.pdf
Add editorial note into 90.7 requesting a link to where explanation on ns and sub-ns number representation is defined, perhaps in IEEE Std 1588?

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **XX** *SC* **XX** *P* *L* # 10

Tse, Richard Microchip Technology

Comment Type **TR** *Comment Status* **D**

Informative text is needed to help a user understand the consequences of 802.3cx.

SuggestedRemedy

See tse_3cx_01_0121 for overview of what can be placed in this annex

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Material was not available at the time proposed responses were written.