Explanation or Clarification for comment group #355, #361, #367, #377, #383, #389 submitted during 802.3cx D2.1 review

For e.g, details comment #355 is given below

Cl 45 SC 45.2.1 P 24 L 16 # 355

Kabra, Lokesh Synopsys Inc

Comment Type **E** *Comment Status* **D** *bucket*

Title of registers can be made consistent

SuggestedRemedy

Modify the existing lines in Table 45-3 as follows

1.1801 through 1.1804 TimeSync PMA/PMD transmit path data delay in ns
45.2.1.176

1.1805 through 1.1808 TimeSync PMA/PMD receive path data delay in ns
45.2.1.177

1.1809 through 1.1810 TimeSync PMA/PMD transmit path data delay in fractional ns
45.2.1.176

1.1811 through 1.1812 TimeSync PMA/PMD receive path data delay in fractional ns
45.2.1.177

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The added value of changes to existing names is not clear.

The PMA/PMD TimeSync Register listing in current 802.3 Table 45-3 is given below.

1.1800	TimeSync PMA/PMD capability	45.2.1.165
1.1801 through 1.1804	TimeSync PMA/PMD transmit path data delay	45.2.1.166
1.1805 through 1.1808	TimeSync PMA/PMD receive path data delay	45.2.1.167
1.1809 through 1.1899	Reserved	

It does not differentiate between the Maximum & Minimum path delay registers but group them together in transmit & receive path data delay groups respectively.

But 802.3cx D2.1 proposes to add the following rows which is not consistent with existing listing because the max & min registers are listed separately.

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
...	...	...
1.1809	Maximum fine resolution PMA/PMD transmit path data delay	45.2.1.176
1.1810	Minimum fine resolution PMA/PMD transmit path data delay	45.2.1.176
1.1811	Maximum fine resolution PMA/PMD receive path data delay	45.2.1.177
1.1812	Minimum fine resolution PMA/PMD receive path data delay	45.2.1.177
1.181~~300~~ through 1.1899	Reserved	
...	...	...

However, the new registers are only extensions of the existing “TimeSync path delay” with an additional sub-ns (or fractional ns) field. Moreover, these registers are considered as a

register group or register set with “TimeSync path delay” value and being described in common sub-section clause.

For example

Change text of subclause 45.2.1.176 as shown below:

45.2.1.176 TimeSync PMA/PMD transmit path data delay (Registers 1.1801, 1.1802, 1.1803, 1.1804, 1.1809, and 1.1810)

This case is very similar to the data types defined in say, IEEE 1588 given below.

5.3.3 Timestamp

The Timestamp type represents a positive time with respect to the epoch.

```
Struct Timestamp
{
UInteger48 secondsField;
UInteger32 nanosecondsField;
};
```

The secondsField member is the integer portion of the timestamp in units of seconds.

The nanosecondsField member is the fractional portion of the timestamp in units of nanoseconds.

The nanosecondsField member is always less than 10^9.

Hence my proposal is to give consistent names to the register set and differentiate it based on the resolution of the time value.

Register Address	Register name	Sub-Clause
1.1801 through 1.1804	TimeSync PMA/PMD transmit path data delay **in ns**	45.2.1.176
1.1805 through 1.1808	TimeSync PMA/PMD receive path data delay **in ns**	45.2.1.177
1.1809 through 1.1810	TimeSync PMA/PMD transmit path data delay **in sub-ns**	45.2.1.176
1.1811 through 1.1812	TimeSync PMA/PMD receive path data delay **in sub-ns**	45.2.1.177

This will help to make it clear that these registers belong to 1 group and contain the same variable/field (e.g transmit path delay) but just gives values in ns and sub-ns respectively.

The same justification applies for the comments #361, #367, #374, #377, #383, #386, #389 for the TimeSync register sets listing for WIS, PCS, DTE XS, DTE PHY and TC layers.

I understand that the names of existing registers are updated but it does not affect the function of existing implementations. But it helps in properly organizing the register set/groups in new HW/SW implementations that go for the sub-ns resolution capability.

Explanation or Clarification for comment group #358, #360, #364, #366, #374, #376, #380, #382, #386, #388, #392, #394

With the same justification as provided for previous comment group, I proposed to update the detailed description of the register fields of the "TimeSync path data delay" registers as given below. For example, comment #358 is given below

Cl **45** *SC* **45.2.1.176** *P* **26** *L* **8** # 358

Kabra, Lokesh — Synopsys Inc

Comment Type **E** *Comment Status* **D** *bucket*

Names be made more consistent

SuggestedRemedy

Modify the existing lines in Table 45-140 as follows
1.1801.15:0 Maximum PMA/PMD transmit path data delay in ns, lower PMA_PMD_delay_ns_TX_max[15:0]
1.1802.15:0 Maximum PMA/PMD transmit path data delay in ns, upper PMA_PMD_delay_ns_TX_max[31:0]
1.1803.15:0 Minimum PMA/PMD transmit path data delay in ns, lower PMA_PMD_delay_ns_TX_min[15:0]
1.1804.15:0 Minimum PMA/PMD transmit path data delay in ns, upper PMA_PMD_delay_ns_TX_min[31:0]
1.1809.15:0 Maximum PMA/PMD transmit path data delay in sub-ns PMA_PMD_delay_sub-ns_TX_max[15:0]
1.1810.15:0 Minimum PMA/PMD transmit path data delay in sub-ns PMA_PMD_delay_sub-ns_TX_min[15:0]

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The added value of changes to existing names is not clear.

IEEE 802.3cx D2.1 proposed to make the following changes to Table 45-140

Table 45–140—TimeSync PMA/PMD transmit path data delay register

Bit(s)	Name	Description	R/W[a]
1.1801.15:0	Maximum PMA/PMD transmit path data delay, lower	PMA/PMD_delay_TX_max [15:0]	RO, MW
1.1802.15:0	Maximum PMA/PMD transmit path data delay, upper	PMA/PMD_delay_TX_max [31:16]	RO, MW
1.1803.15:0	Minimum PMA/PMD transmit path data delay, lower	PMA/PMD_delay_TX_min [15:0]	RO, MW
1.1804.15:0	Minimum PMA/PMD transmit path data delay, upper	PMA/PMD_delay_TX_min [31:16]	RO, MW
1.1809.15:0	Maximum fine resolution PMA/PMD transmit path data delay	PMA/PMD_fine_delay_TX_max [15:0]	RO
1.1810.15:0	Minimum fine resolution PMA/PMD transmit path data delay	PMA/PMD_fine_delay_TX_min [15:0]	RO

[a]RO = Read only, MW = Multi-word.

In my opinion, it does not give clarity on difference between “delay” and “fine_delay” register/fields.

Hence my proposal was to make the description consistent and further give clarity to the differences (“ns” and “subns” fields of the same variable) as shown below.

Bit(s)	**Name**	**Description**	
1.1801.15:0	Maximum PMA/PMD transmit path data delay **in ns,** lower	PMA/PMD_delay_**ns_**Tx_max[15:0]	
1.1802.15:0	Maximum PMA/PMD transmit path data delay **in ns**, upper	PMA/PMD_delay_**ns_**Tx_max[31:16]	
1.1803.15:0	Minimum PMA/PMD transmit path data delay **in ns**, lower	PMA/PMD_delay_**ns_**Tx_min[15:0]	
1.1804.15:0	Minimum PMA/PMD transmit path data delay **in ns**, upper	PMA/PMD_delay_**ns_**Tx_min[31:16]	
1.1809.15:0	Maximum PMA/PMD transmit path data delay **in sub-ns**	PMA/PMD_delay_**subns_**Tx_max[15:0]	
1.1810.15:0	Minimum PMA/PMD transmit path data delay **in sub-ns**	PMA/PMD_delay_**subns_**Tx_min[15:0]	

Similarly, comment #360 applies to the description of Max/Min PMA/PMD receive path delay register sets.

The same justification applies for comments #364/366, #374/376, #380/382, #386/388, and #392-394 for the TimeSync register field description in WIS, PCS, DTE XS, DTE PHY and TC layers