Improving PTP Timestamping Accuracy on Ethernet Interfaces

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802.3cx telephonic interim – May 12, 2020

Open Issues

For the last several meetings, the following issues have been discussed and identified

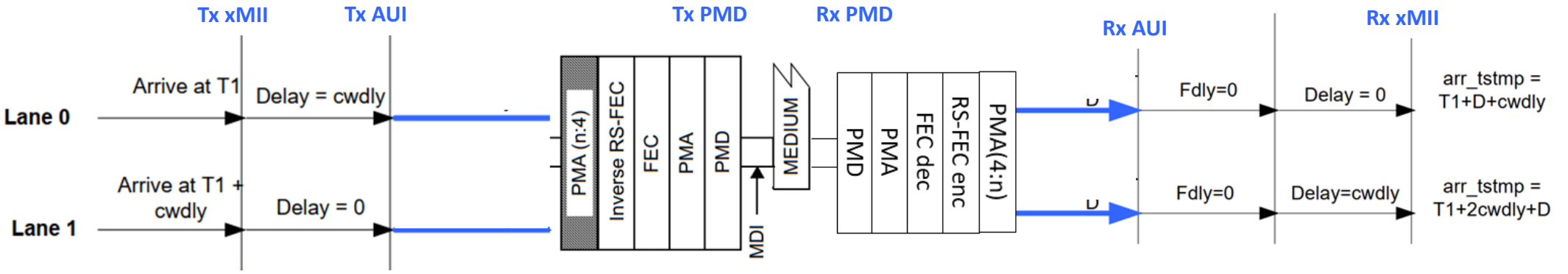
1. Timestamp reference point in IEEE 802.3 is different from IEEE 1588 and IEEE 802.1AS
2. Effect of idle insertion/deletion for AMs
3. Timestamp inaccuracy due to CWM Insertion/Deletion
4. Impact of PCS Lane Distribution

There are more issues to be considered:

5. Impact of split (or extended) PHY, such as oDSP?
6. Impact of asymmetric PHY (PCS/FEC) latency?

Example of Split PHY – oDSP with PCS functions

- Additional PHY sublayers on the link may cause additional delay variation and uncertainties.
  - Protocol-aware oDSP contains various functions such as FEC encoding/decoding, PCS lane aggregation and redistribution, etc. For example:
    - 802.3ct/cw defined stacks which include PCS deskew and reorder, RS FEC dec/enc, SC-FEC enc/dec, GMP…
    - Different implementations could introduce asymmetric delay, and different delay variations on each direction.
- Timestamp performance over such links should be thoroughly analyzed.



*Detailed view of the functions within the blocks are available in the back up slides.

Partially borrowed from [tse_3cx_02_0420]

Detailed Impact of Split PHY

- Delay variation
  - Rate adaptation and/or AM insertion/removal?
  - Jitter due to FEC conversions?
    - Additional FEC layer introduces different amount of parity bits, without knowing the SFD position, thus could introduce additional jitter.
  - Delay variation between power cycles or resets.
- Delay asymmetry
  - Different implementations have different process delay.
  - If treating the process delay as part of link delay, the delay asymmetry will cause timestamp errors.
- Delay report
  - In cases where this split PHY has fixed process delay, the delay shall be reported through a register or a message.
  - Sync client could use this reported delay for timestamp compensation.

Timestamp Reference Point Selection

- Current 802.3 Clause 90 recommended data delay measurement should be done from xMII to MDI.
  - This delay measurement is recommended not to include any part of medium.
  - Tx PDD is measured from xMII to MDI.
  - Rx PDD is measured from MDI to xMII.

  → The reference point with **“zero delay”** is at the MDI.
- Changing timestamp reference would cause interop problems.
  - Using actual departing time at xMII is equivalent to moving timestamp reference point to xMII.
  - Even if data delay defined in Clause 90.7 is compensated in the same way, the error could be as much as tens of nanoseconds (in case of 100GbE) if devices with different timestamp reference point are connected.

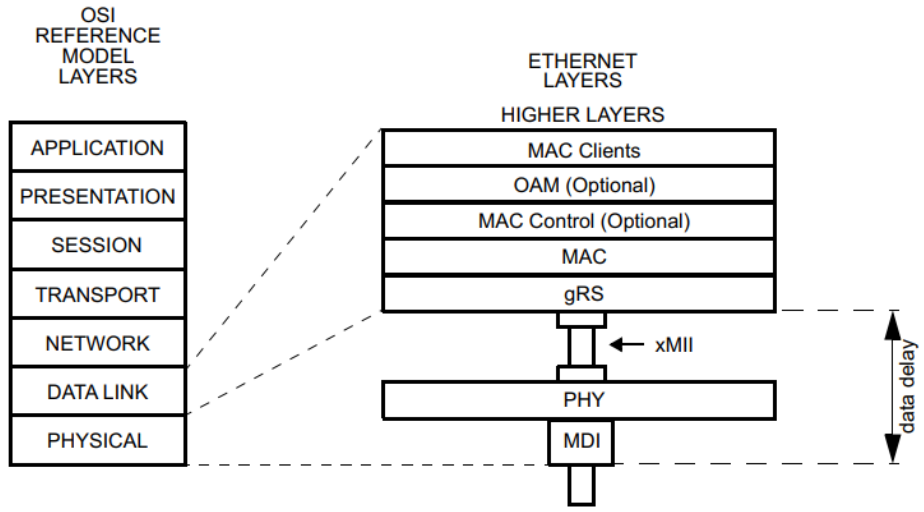
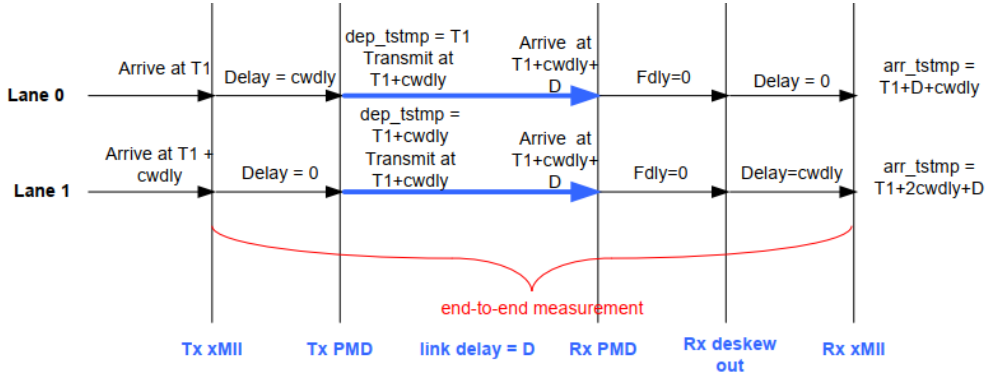


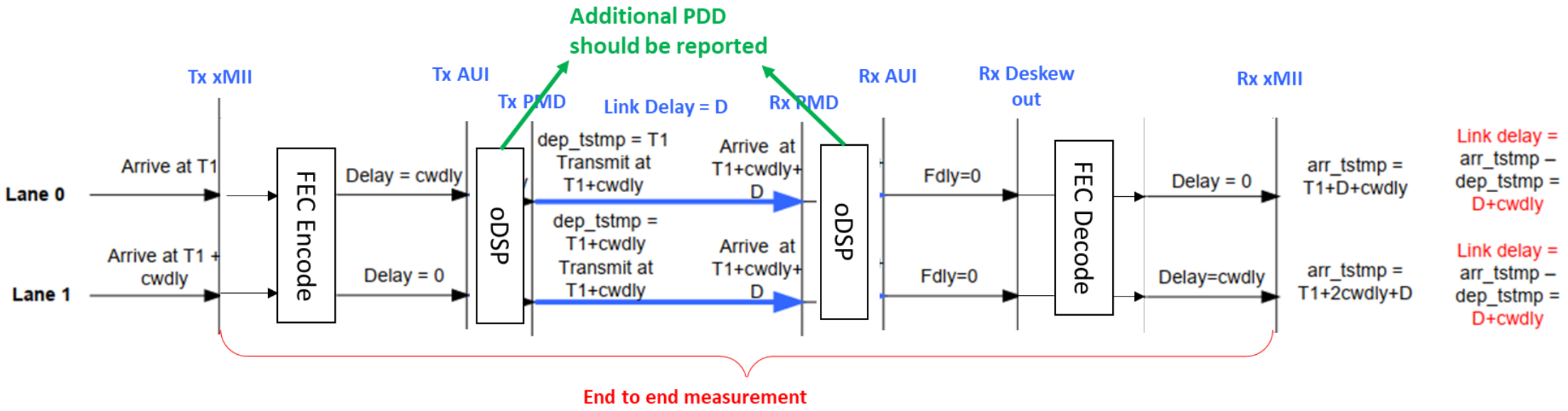
Figure 90–3—Data delay measurement



Option C in tse_3cx_02_0420

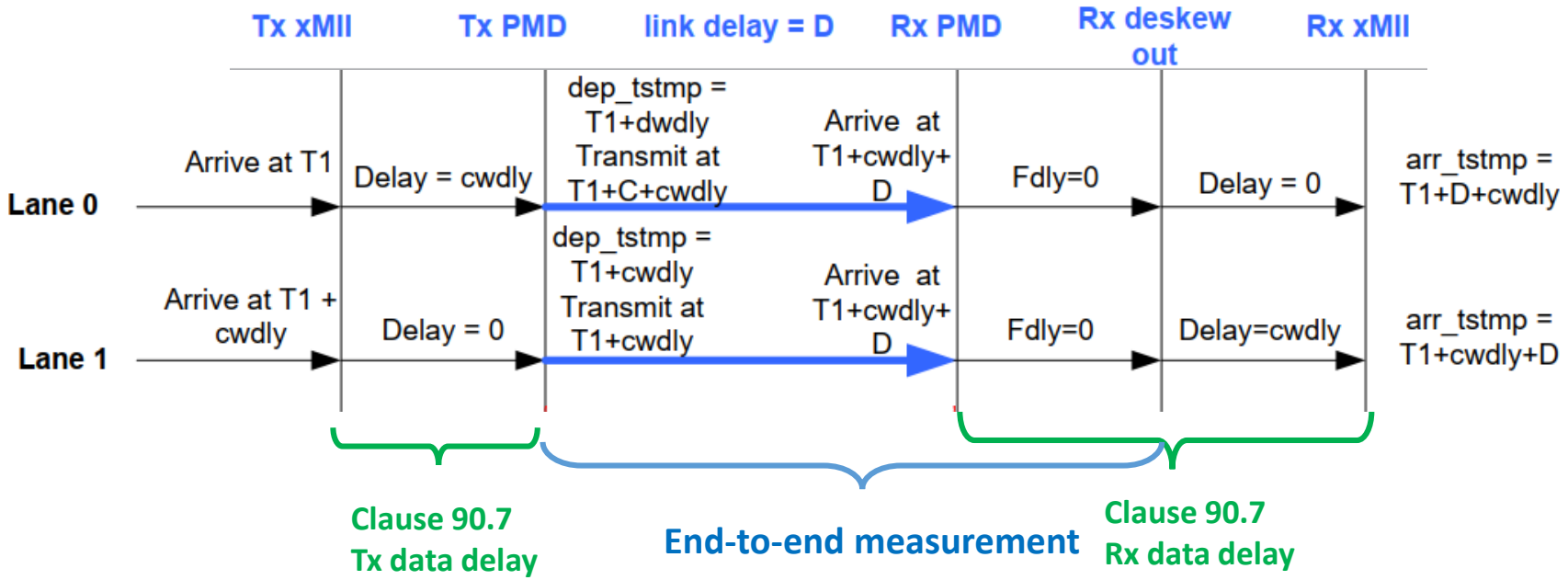
Relationship Between TS Reference Point and PCS/FEC Latency

- FEC parity bits insertion/removal were considered in previous discussions.
- Additional PCS/FEC latencies should also be considered.
  - Currently Clause 90.7 data delay measurement includes all PHY processes from xMII to MDI.
- Asymmetric latency should be considered when selecting timestamp reference point.
  - Different implementations will introduce different delays, easily to the order of ~100s of ns.
  - Split PHY complicates delay reporting and timestamp compensation.
  - Using lane-specific timestamp at xMII requires PDD reporting to be a dynamic and real-time process.



One Possible Solution

- Option B in tse_3cx_02_0420 provided a good start
  - Tx lanes and timestamps are aligned at PMD.
  - Rx lanes and timestamp are aligned after deskew, before FEC decoding.



- Aligns with current 802.3 Clause 90.7 recommendations.
- Additional delay in each PHY sublayers is compensated based on reported path data delays.
- Other potential solutions?

THANK YOU!

Detailed View of 802.3ct Defined Functions