Updated Annex Proposal for 802.3cx

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

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Proposed Annex for 802.3cx

- **Annex would help the reader understand:**
  - The purpose and effects of the 802.3cx specifications
  - How to use the 802.3cx specifications
  - How repeating and mirrored variable delays can be accounted for

Feedback on Initial Proposal for Annex

- **Initial proposal can be found at:**
  - Proposed Annex for 802.3cx
- **Feedback from Jan 19, 2021 meeting:**
  - For num_blk_change:
    - Also include an example for the Rx direction
  - For message timestamp point mismatch:
    - Without *num_blk_change, CWM could introduce error larger than one byte time on single-lane interfaces
    - For non-802.3cx compliant implementations, FEC could introduce an error larger than one byte time
  - For AM/CWM and corresponding idle insertion/removal:
    - Without *num_blk_change, the low frequency time error events might not be filtered out by a ToD recovery algorithm's LPF
  - Too much information can lead to comments that are difficult to address
    - Information that clarifies the concepts behind the normative text can help the reader

Response to Feedback (1/2)

- **For num_blk_change**
  - Add example for the Rx direction
- **For message timestamp point mismatch:**
  - Add CWM as item of consideration for time errors in non-802.3cx-compliant implementations
  - FEC (on its own) appears to be handled by subclause 90.7 in IEEE Std 802.3-2018 (see below) and its delay is a constant even for 802.3bf-based implementations. The effects that multi-PCS lanes might have on FEC are considered a problem of the multi-PCS lane function.
    - “For a PHY that includes an FEC function, the transmit and receive path data delays may show significant variation depending upon the position of the SFD within the FEC block. However, since the variation due to this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays be reported as if the SFD is at the start of the FEC block.”

Response to Feedback (2/2)

- **For AM/CWM and corresponding idle insertion/removal:**
  - Give general statement that corresponding time error events are typically irregular and infrequent and, thus, their time error effects might be attenuated by a LPF in the ToD recovery algorithm
    - Do not include any calculations or give any concrete conclusions about resulting PTP performance
- **Too much information can lead to comments that are difficult to address**
  - Only use generalized statements about non-802.3cx-compliant implementations
  - Do not make any conclusions on fixing time errors for non-802.3cx-compliant implementations

Outline of Proposed Annex

1. **Background on Timing Errors**
2. **Considerations for use of Different Message Timestamp Points**
   - Time error effects
3. **Considerations for Multi-PCS Lane Functions**
   - Time error effects
   - Use of constant delay model
   - Use of TimeSync PCS Tx/Rx path data delay registers
4. **Consideration for AM/CWM Functions**
   - Time error effects
   - Use of Tx/Rx num_blk_change signals and TimeSync PCS Tx/Rx path data delay registers
5. **Considerations for Tx skew**
   - Tx skew and its relationship with medium skew
6. **General Method for Dealing with Repeating Delay Variation Patterns**

Thank You