Considerations for Forward Error Correction (FEC) Mechanisms

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PTP and iterative, concatenated, and other FECs

- The existence of iterative FECs in IEEE 802.3 was brought up at the Jan 2020 IEEE 802.3 ITSA Study Group meeting, sparking a topic that should be investigated by this task force
- This presentation is from non-FEC experts and is meant to provoke discussions on FECs and how they can affect PTP
- Can we specify general method(s) to deal with the delay characteristics of known and expected FECs?

What are the general characteristics of FECs?

- **If the input to the FEC encoder(s) and the output from the FEC decoder(s) are identical, then the total delay of the encoder(s) and the decoder(s) must be a constant**
  - A mechanism similar to the solution, specified in clause 90.7, for existing IEEE 802.3 RS FECs should work for all such scenarios
  - Delays of concatenated FECs would add linearly
  - Iterative FECs
    - Does each successive iteration have a deterministic intrinsic delay value or characteristic?
    - Is the number of iterations fixed once steady-state operation has been reached?
    - Is the intrinsic delay of the 2nd, 3rd, etc iteration a static value?
    - Can an iterative FEC decoder show how many iterations are being used?
    - Can the number of FEC decoder iterations being used by the two endpoints of a link be different?
    - Is the FEC encoder's delay characteristic different from that of a non-iterative FEC?

A general method to deal with iterative FEC delays for PTP?

- **Require that each FEC decoder disclose how many iterations are being used**
- **Treat the intrinsic delay of the encoder and the first decoder iteration in the same way as existing 802.3 RS FECs**
  - Sum of the intrinsic delays of the encoder and of the first decoder iteration is a known static value
  - This value is distributed in a pre-determined manner between the encoder and the decoder (e.g., 100%/0% at the encoder/decoder, 50%/50% at the encoder/decoder)
- **Treat the intrinsic static delays of successive decoder iterations in the same way as transparent clock residence times**
  - Compensates for asymmetric delays in uplink and downlink due to different number of iterations

Proposal

- We need to find all the FECs that are used or will be used with 802.3 and find methods to make them work with PTP
- We might need to interact with the task forces that are working on these FECs if we need special features from them

Questions?

Thanks!