Higher Accuracy for IEEE 802.3 PCS Path Data Delay Registers

Richard Tse, Microchip Technology

Marek Hajduczenia, Charter Communications

IEEE 802.3cx Teleconference, Nov 17, 2020

Supporters:

- Andras de Koos, Microchip Technology
- Bill Powell, Independent
- Clark Carty, Cisco Systems
- David Law, Hewlett Packard Enterprise
- Denny Wong, Xilinx
- Dino Pozzebon, Microchip Technology
- Marek Hajduczenia, Charter Communications
- Mark Bordogna, Intel
- Richard Tse, Microchip Technology
- Sriram Natarajan, Cisco Systems
- Steve Carlson, High Speed Design Inc.
- Ulf Parkholm X, Ericsson

Limited Resolution Problem

- The PCS path data delay registers in clause 45 of IEEE 802.3 are 32-bits in size and have the resolution of 1ns
  - This might be insufficient for high accuracy applications

- We recommend to add a high precision 16-bit register to each of the existing registers to represent fractional nanoseconds
  - 16-bit fractional nanoseconds is compatible with the best resolution possible in IEEE 1588-2019 (used in the PTP common header's *correctionField*)

Current PCS Tx Path Data Delay Registers

45.2.3.67 TimeSync PCS transmit path data delay (Registers 3.1801, 3.1802, 3.1803, 3.1804)

The TimeSync PCS transmit path data delay register contains the maximum (Registers 3.1801, 3.1802, see Table 45–236) and minimum (Registers 3.1803, 3.1804, see Table 45–236) values of the transmit path data delay. The transmit path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.4).

Table 45–236—TimeSync PCS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
3.1801.15:0	Maximum PCS transmit path data delay, lower	PCS_delay_TX_max [15:0]	RO, MW
3.1802.15:0	Maximum PCS transmit path data delay, upper	PCS_delay_TX_max [31:16]	RO, MW
3.1803.15:0	Minimum PCS transmit path data delay, lower	PCS_delay_TX_min [15:0]	RO, MW
3.1804.15:0	Minimum PCS transmit path data delay, upper	PCS_delay_TX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

Current PCS Rx Path Data Delay Registers

45.2.3.68 TimeSync PCS receive path data delay (Registers 3.1805, 3.1806, 3.1807, 3.1808)

The TimeSync PCS receive path data delay register contains the maximum (Registers 3.1805, 3.1806, see Table 45–237) and minimum (Registers 3.1807, 3.1808, see Table 45–237) values of the receive path data delay. The receive path data delay is expressed in units of ns. The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.4).

Table 45–237—TimeSync PCS receive path data delay register

Bit(s)	Name	Description	R/W[a]
3.1805.15:0	Maximum PCS receive path data delay, lower	PCS_delay_RX_max [15:0]	RO, MW
3.1806.15:0	Maximum PCS receive path data delay, upper	PCS_delay_RX_max [31:16]	RO, MW
3.1807.15:0	Minimum PCS receive path data delay, lower	PCS_delay_RX_min [15:0]	RO, MW
3.1808.15:0	Minimum PCS receive path data delay, upper	PCS_delay_RX_min [31:16]	RO, MW

[a]RO = Read only, MW = Multi-word

correctionField in IEEE Std 1588-2019

13.3.2.9 correctionField (Integer64)

The correctionField is the value of the correction measured in nanoseconds and multiplied by 2^{16}. For example, 2.5 ns is represented as 0000000000028000_{16}.

A value of one in all bits, except the most significant, of the field shall indicate that the correction is too big to be represented.

Proposed Text (1/6)

Insertions are highlighted in blue and deletions are highlighted in ~~red~~.

45.2.3.66 TimeSync PCS capability (Register 3.1800)

The TimeSync PCS capability register (see Table 45–235) indicates the capability of the PCS to report the transmit ~~and receive~~ data delay~~, stored~~ (in ns-resolution registers 3.1801 through 3.1804 and, separately, in sub-ns-resolution registers 3.1809 and 3.1810) and receive data delay (in ns-resolution registers 3.1805 through 3.1808 and, separately, in sub-ns-resolution registers 3.1811 and 3.1812)~~, respectively~~.

Proposed Text (2/6)

- Modify Table 45-235–TimeSync PCS capability register as shown below

Bit(s)	Name	Description	R/W[a]
3.1800.15:4	Reserved	Value always 0	RO
3.1800.3	TimeSync fine resolution transmit path data delay	1 = PCS provides information on transmit path data delay with sub-ns-resolution in registers 3.1809 and 3.1810 0 = PCS does not provide information on transmit path data delay with sub-ns-resolution	RO
3.1800.2	TimeSync fine resolution receive path data delay	1 = PCS provides information on receive path data delay with sub-ns-resolution in registers 3.1811 and 3.1812 0 = PCS does not provide information on receive path data delay with sub-ns-resolution	RO
3.1800.1	TimeSync transmit path data delay	1 = PCS provides information on transmit path data delay with ns-resolution in registers 3.1801 through 3.1804 0 = PCS does not provide information on transmit path data delay with ns-resolution	RO
3.1800.0	TimeSync receive path data delay	1 = PCS provides information on receive path data delay with ns-resolution in registers 3.1805 through 3.1808 0 = PCS does not provide information on receive path data delay with ns-resolution	RO

Proposed Text (3/6)

45.2.3.67 TimeSync PCS transmit path data delay (Registers 3.1801, 3.1802, 3.1803, 3.1804, 3.1809, and 3.1810)

The TimeSync PCS transmit path data delay and fine resolution transmit path data delay registers contains the maximum ~~(Registers 3.1801, 3.1802, see Table 45–236)~~ and minimum ~~(Registers 3.1803, 3.1804, see Table 45–236)~~ values of the PCS transmit path data delay. ~~The transmit path data delay is expressed in units of ns.~~ The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.4), and when the corresponding capability register bit (see Table 45–235) is asserted.

The maximum PCS transmit path data delay value is given in two sets of registers. The first set (Registers 3.1801 and 3.1802, see Table 45–236) gives the integer nanoseconds portion of the maximum PCS transmit path data delay, in units of ns. The second set (Register 3.1809, see Table 45–236) gives the fractional nanoseconds portion of the maximum PCS transmit path data delay, in units of 2^{-16} ns. If both sets of registers are valid (see Table 45–235), the maximum PCS transmit path data delay is the sum of the values from these two sets of registers. If any of the two register sets are not valid, then the corresponding value is not included in the maximum PCS transmit path data delay.

The minimum PCS transmit path data delay value is given in two sets of registers. The first set (Registers 3.1803 and 3.1804, see Table 45–236) gives the integer nanoseconds portion of the minimum PCS transmit path data delay, in units of ns. The second set (Register 3.1810, see Table 45–236) gives the fractional nanoseconds portion of the minimum PCS transmit path data delay, in units of 2^{-16} ns. If both sets of registers are valid (see Table 45–235), the minimum PCS transmit path data delay is the sum of the values from these two sets of registers. If any of the two register sets are not valid, then the corresponding value is not included in the minimum PCS transmit path data delay.

Proposed Text (4/6)

- Add the following rows to Table 45-236 –TimeSync PCS transmit path data delay register

Bit(s)	Name	Description	R/W[a]
3.1809.15:0	Maximum fine resolution PCS transmit path data delay	PCS_fine_delay_TX_max[15:0]	RO, MW
3.1810.15:0	Minimum fine resolution PCS transmit path data delay	PCS_fine_delay_TX_min[15:0]	RO, MW

Proposed Text (5/6)

45.2.3.68 TimeSync PCS receive path data delay (Registers 3.1805, 3.1806, 3.1807, 3.1808, 3.1811, and 3.1812)

The TimeSync PCS receive path data delay and fine resolution receive path data delay registers contains the maximum ~~(Registers 3.1805, 3.1806, see Table 45–237)~~ and minimum ~~(Registers 3.1807, 3.1808, see Table 45–237)~~ values of the PCS receive path data delay. ~~The receive path data delay is expressed in units of ns.~~ The values contained in these registers are valid when the link is established, as indicated by bit 2 in Register 1.1 (see 45.2.1.2.4), and when the corresponding capability register bit (see Table 45–235) is asserted.

The maximum PCS receive path data delay value is given in two sets of registers. The first set (Registers 3.1805 and 3.1806, see Table 45–237) gives the integer nanoseconds portion of the maximum PCS receive path data delay, in units of ns. The second set (Register 3.1811, see Table 45–237) gives the fractional nanoseconds portion of the maximum PCS receive path data delay, in units of 2^{-16} ns. If both sets of registers are valid (see Table 45–235), the maximum PCS receive path data delay is the sum of the values from these two sets of registers. If any of the two register sets are not valid, then the corresponding value is not included in the maximum PCS receive path data delay.

The minimum PCS receive path data delay value is given in two sets of registers. The first set (Registers 3.1807 and 3.1808, see Table 45–237) gives the integer nanoseconds portion of the minimum PCS receive path data delay, in units of ns. The second set (Register 3.1812, see Table 45–237) gives the fractional nanoseconds portion of the minimum PCS receive path data delay, in units of 2^{-16} ns. If both sets of registers are valid (see Table 45–235), the minimum PCS receive path data delay is the sum of the values from these two sets of registers. If any of the two register sets are not valid, then the corresponding value is not included in the minimum PCS receive path data delay.

Proposed Text (6/6)

- Add the following rows to Table 45-237 –TimeSync PCS receive path data delay register

Bit(s)	Name	Description	R/W[a]
3.1811.15:0	Maximum fine resolution PCS receive path data delay	PCS_fine_delay_RX_max[15:0]	RO, MW
3.1812.15:0	Minimum fine resolution PCS receive path data delay	PCS_fine_delay_RX_min[15:0]	RO, MW

Thank you!

Any questions or comments?